

FPD93140

Small Format a-Si AMLCD Gate Driver with Integrated Power Supply

General Description

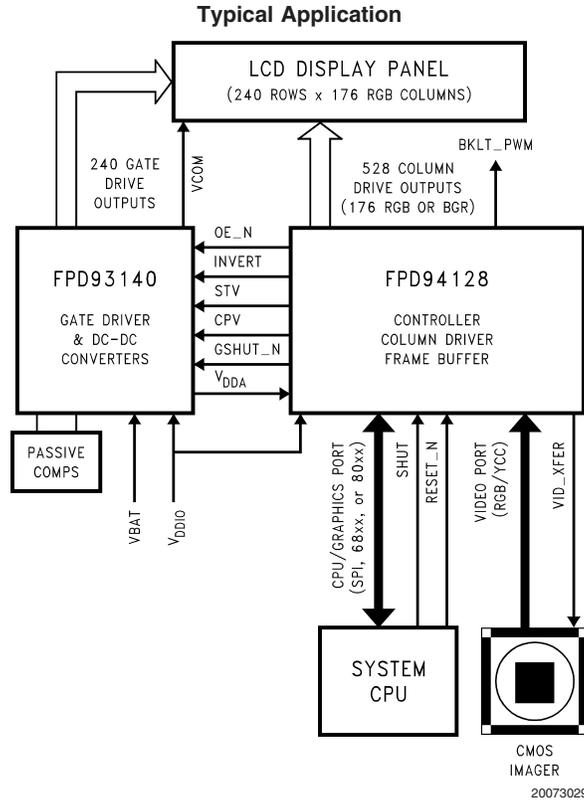
The FPD93140 is a Low Power Gate Driver with Power Supply for Small Format LCD Displays. The FPD93140 and the companion FPD94128 (Controller / Column Driver with Integrated Frame Buffer) form a complete 2-chip solution for driving TFT LCD panels containing up to 176RGB X 240 pixels with versatile mounting and scan options. Its function is to drive the gates of the LCD active matrix displays and to generate all the supply voltages necessary for display operation. A shift register activates rows sequentially in programmable sequences based on the external clock. On chip charge pumps require a minimum number of external capacitors to generate all the necessary voltages to power the FPD94128 Column Driver and drive the LCD rows.

Under command from the FPD94128 series Column Driver, the FPD93140 can drive from 2 to 240 rows. This allows the use of various display sizes and Partial Display modes to reduce power consumption.

Features

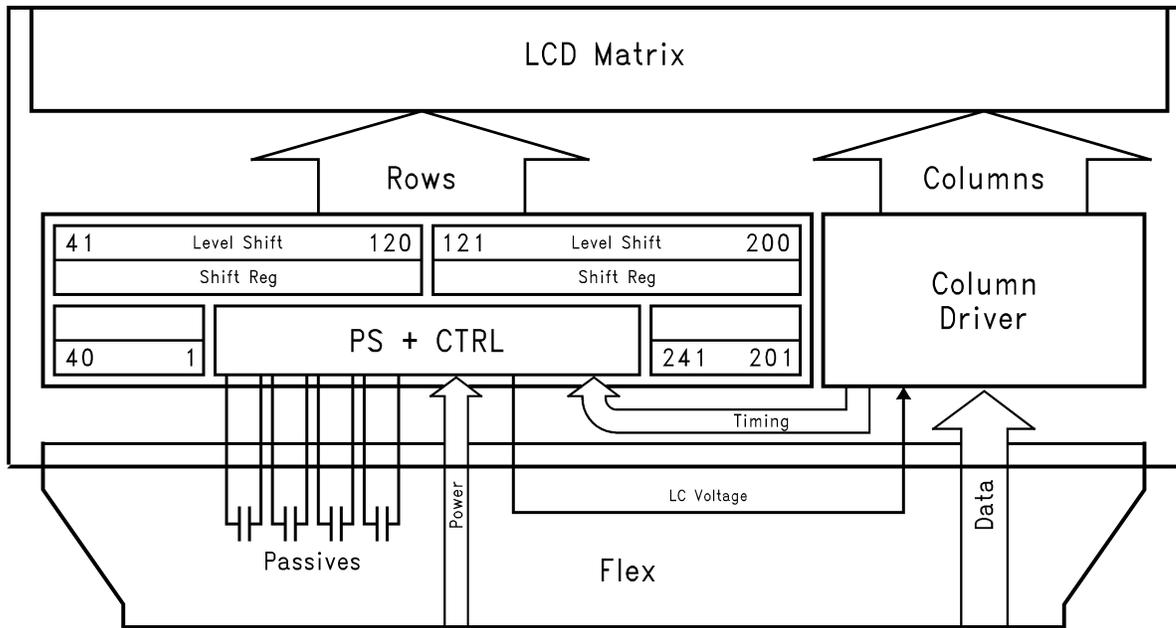
- 241 Outputs Accommodates from 2 to 240 Rows with a dummy row
- Bumped Flip Chip Packaging (45um Row Centers)
- 4 Flexible mounting/scan options provide for symmetric display layout
- Wide Supply input range of 2.85V to 5.5V for direct connection to Li-Ion battery
- Low Power < 100µA I_Q
- High Efficiency (80%)
- Onboard Charge Pump Power Supplies:
 - +9 to +18V @ 100µA
 - -6 to -12V @ 100µA or -9 to -18V @ 100µA
- 3 to 6V @ 1mA Adjustable LCD Voltage
- VCOM driver and adjustable LCD Voltage
- Optional "off-level" modulation in phase with VCOM

Block Diagrams



Block Diagrams (Continued)

FPD93140 Block Diagram



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Functional Description

Row Driver

Row output voltages are generated by on chip charge pumps or can be provided externally. Level Shifters change low voltage shift register outputs into drive voltages. A pre-charge scheme reduces power dissipation while driving the gate line capacitance.

Vertical Start (STV) is sampled on the Rising Edge of CPV and activates ROW1 immediately. Subsequent rising edges of CPV shift to the next ROW output. OE- enables each ROW going high. It can be used to blank ROW outputs while waiting for columns to settle. Unused rows are skipped by clocking the STV token through without enabling the Outputs (Burst Mode).

An optional Row Invert signal (RINV) can be used to modulate VN in conjunction with VCOM if the LCD storage capacitor is tied to an adjacent row. This allows the storage cap and LCD cap to track. RINV should be tied low to disable this behavior. An additional row output is provided to attach to a final dummy row if necessary.

Power Supply

A doubler charge pump creates 2xVDD. An externally adjustable LDO voltage regulator then creates a voltage VG that is

external adjustable from 3 to 6V. VG is then tripled and inverted to create VGH (3xVG) and VGL (-2 or -3xVG) high and low logic levels for the Row Driver Outputs.

An adjustable voltage regulator creates VLCD. VLCD is intended to provide the Column Driver (CD) with LCD bias voltage. VLCD is derived from the VDD or 2xVDD depending on their value relative to VLCD to optimize efficiency. During shutdown the VLCD output is internally switched to VDD to provide a standby voltage for the Column Driver.

An adjustable voltage regulator creates VCOMA, the VCOM amplitude voltage. Another adjustable regulator creates VCOMH the VCOM high level. When used with the AC Coupling Capacitor a Modulated VCOM voltage can be created swinging VCOM between VCOMH and VCOMH-VCOMA.

A 1X charge pump is used to translate the VCOMA voltage to the VGL voltage to create ROFFH (VCOMA-VGL) and ROFFL (VGL).

The Charge Pumps are clocked by the CPV signal so that quiescent current tracks frame rate.

Ordering Information

NSID	Function	Package
FPD93140	Gate Driver	COG
FPD94128	Column Driver (see Datasheet)	COG

Notes

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