

FPD87352CXA

+3.3V TFT-LCD Timing Controller with Single LVDS Input/Dual RSDS™ Outputs Including RTC (Response Time Compensation) for TFT-LCD Monitors and TV (XGA/WXGA/HDTV I,II,-)

General Description

The FPD87352CXA is an integrated FPD-Link™ + RSDS + TFT-LCD Timing Controller. The logic architecture is implemented using standard and default timing controller functionality based on an Embedded Gate Array. The device is reconfigurable to the needs of a specific application by providing user-defined specifications or customer supplied VHDL/Verilog code.

The FPD87352CXA is an ideal Timing Controller for LCD TV Applications. It has a unique feature, RTC that will improve the intra-gray level response time of a LCD TV panel. Improving the intra-gray level response time of the LCD panel will result in a dramatically improved Motion Picture Image Quality of video content that are displayed on the LCD panel. The RTC feature is accomplished through application of a Boost or Overdrive Voltage that will force the LC material to respond more rapidly. This Boost or Overdrive is accomplished through combination of an internal or external EEPROM LUT (Look Up Table), which contains the boost/overdrive levels, and external memory that acts as a Frame Buffer.

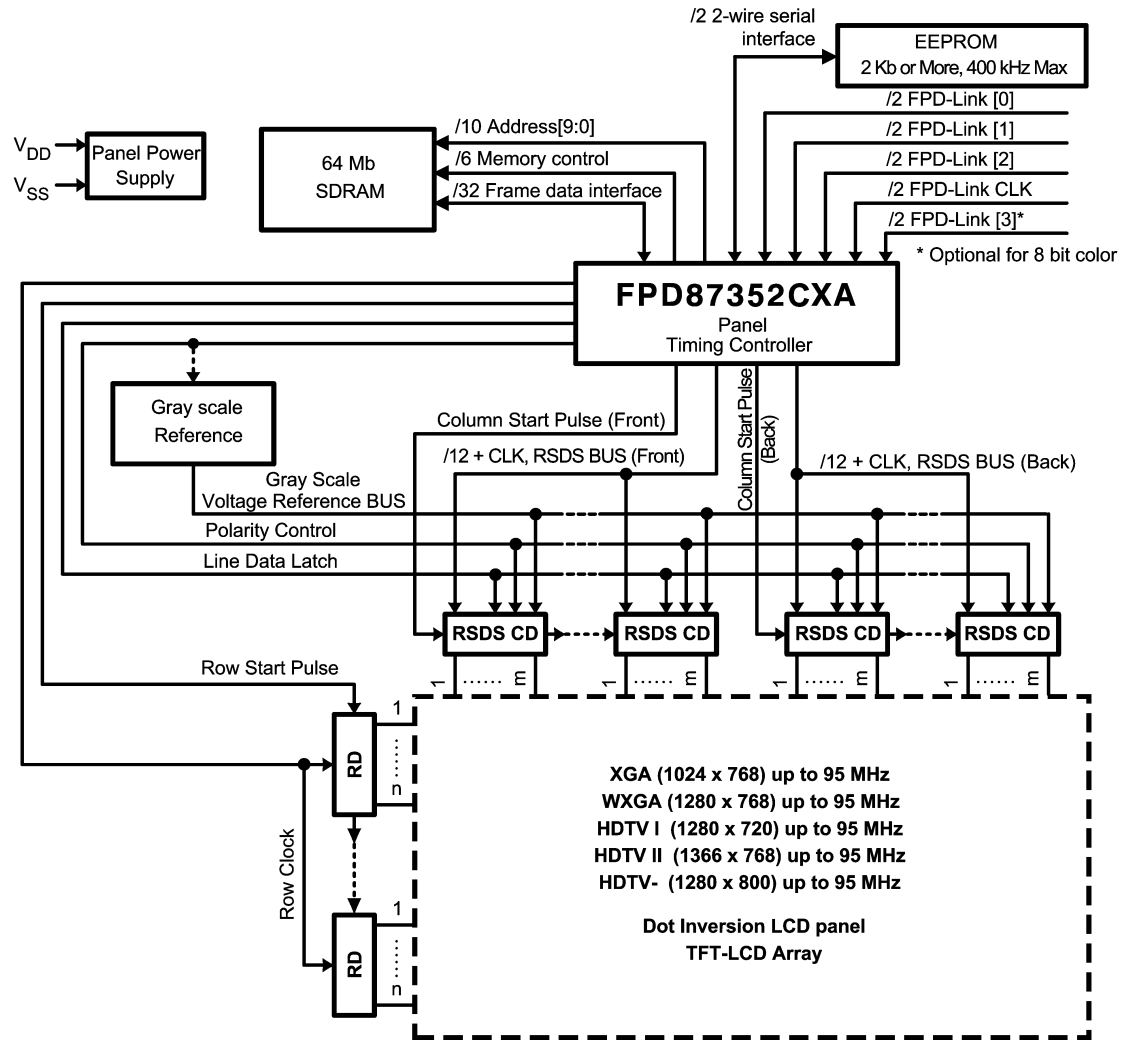
The FPD87352CXA is a timing controller that combines an LVDS single pixel input interface with National's Reduced Swing Differential Signaling (RSDS) output column driver interface for XGA/WXGA/HDTV I,II,- resolutions. It resides on the Flat Panel Display and provides the data buffering and control signal generation. FPD-Link, a lower dynamic power, low EMI (Electro Magnetic Interference) interface is used between this timing controller and the host system. A RSDS interface is used between the timing controller and the column drivers.

The dual 13/10 pair differential bus conveys up to 24-bit color data for XGA, WXGA and HDTV panels.

Features

- Input frequency range from 30 MHz to 95 MHz
- Support display resolutions XGA (1024x768), WXGA (1280x768), HDTV I (1280x768), HDTV II (1366x768) and HDTV - (1280x800)
- Embedded gate array for custom panel timing
- LVDS single pixel input (8-bit/6-bit) interface (FPD-Link)
- RSDS dual bus output (8-bit/6-bit)
- Drives RSDS column drivers up to 47.5 MHz clock
- Flexible RSDS data output mapping for Bottom or Top mount
- RTC (Response time compensation) function
- 2 Wired Serial EEPROM Interface support (RTC LUT)
- Interface with external frame memory
- Virtual 8-bit color depth in FRC/Dithering mode
- Supports Graphics Controllers with spread spectrum interface for lower EMI
- Supports external Spread Spectrum (SSCG)
- DE only mode
- CMOS circuitry operates from 3.0V–3.6V; 0°C–70°C
- 176 LQFP package with body size 24 mm x 24 mm x 1.4 mm, 0.5 mm pitch

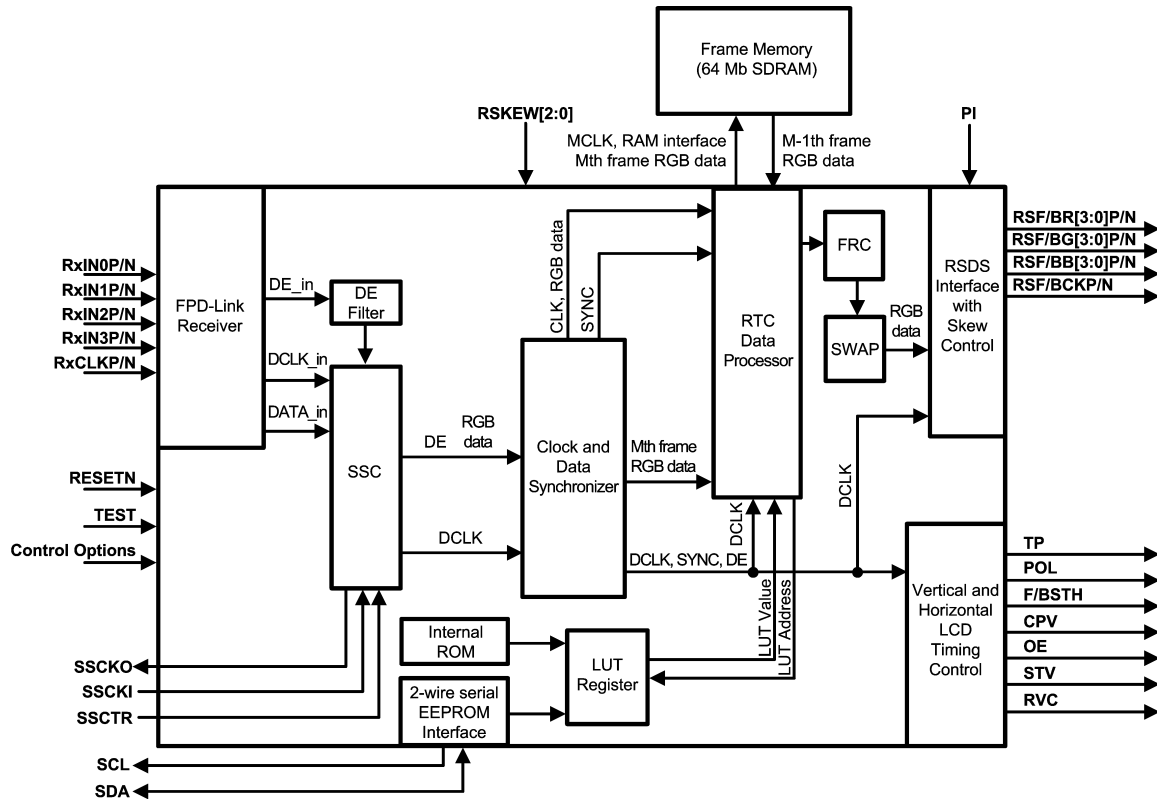
System Diagram



20116201

FIGURE 1. Block Diagram of the LCD Module

Block Diagram



20116202

FIGURE 2. Block Diagram

Function Description

FPD-LINK RECEIVER

The LVDS based FPD-Link Receiver receives input video data and control timing. Four LVDS channels plus clock provide 24-bit color.

RESETN initializes the chip with the default register values for the LUT values from internal ROM or external EEPROM.

SSC (SPREAD SPECTRUM CONTROL)

This SSC function provides a means for reducing EMI. This feature uses external SSC signal source that provides synchronized spread spectrum for RSDS and control signal outputs.

2-WIRE SERIAL EEPROM INTERFACE

The Serial EEPROM Interface controls the FPD87352CXA initialization of LUT register. If the EEPROM is not present, the LUT value is provided by internal ROM of FPD87352CXA.

CLK & DATA SYNCHRONIZER

This function delays and aligns data to match the internal data process which included RSDS skew control by RSKEW[2:0]. All the data processes are needed to be aligned each data path through RSDS output and LCD timing control signal.

LUT REGISTER

This block provides the RTC reference values to be processed on the RTC Data Processor Block. The setting of RTC reference values is provided by the external EEPROM in normal condition. If the external EEPROM is not present it will use the internal ROM's RTC reference values. The RTC reference values are the new gray values depending on the difference between the current frames' RGB gray data and the previous frame's RGB gray data of same pixel.

RTC DATA PROCESSOR

This function generates new gray values depending on the difference of the current RGB gray data and same pixel of the previous frame. The reference values fetch from the LUT (Look Up Table) values in the LUT Register.

RSDS INTERFACE WITH SKEW CONTROL

This functional block transforms CMOS level signal to RSDS for the system clock (DCLK) and RGB color data. The RSDS skew is controlled by RSKEW[2:0] with delay steps between the RSF/BCKP/N and RSF/BR/G/B[3:0]P/N which is implemented in CLK & Data synchronizer.

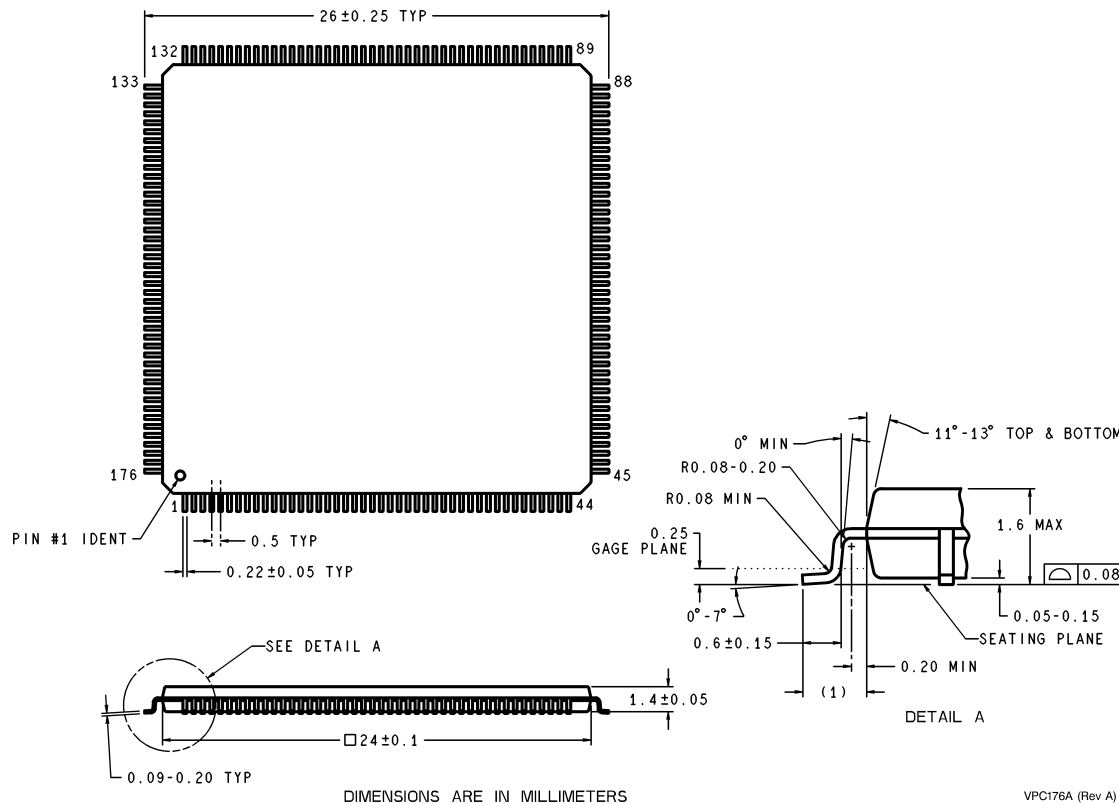
Function Description (Continued)

VERTICAL & HORIZONTAL LCD TIMING CONTROL

This function block generates the TTL(CMOS) level signal for the interface of column drivers and row drivers in the LCD

system. All signals are synchronized by RSF/BCKP/N which is RSDS data clock for the column drivers. The clock skew control must not change the typical timing of TTL(CMOS) level signals.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

- STANDARD LEAD FINISH:
7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15) THICKNESS ON COPPER.
- DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25 mm PER SIDE.
- REFERENCE JEDEC REGISTRATION MS-026, VARIATION BGA, DATED FEBRUARY 1999.

**Plastic Quad Flatpack, JEDEC
NS Package Number VPC176A**

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