National Semiconductor

PRELIMINARY
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FPD87346
Low EMI, Low Dynamic Power (SVGA) XGA/WXGA TFT-LCD Timing Controller with Reduced Swing Differential Signaling (RSDS™) Outputs

General Description

The FPD87346 is a timing controller that combines an LVDS single pixel input interface with National's Reduced Swing Differential Signaling (RSDS™) output driver interface for (SVGA) XGA and Wide XGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for (SVGA) XGA, and Wide XGA graphic modes. The RSDS™ path to the column driver contributes toward lowering radiated EMI and reducing system dynamic power consumption.

This single RSDS™ bus conveys the 8-bit color data for (SVGA) XGA, and Wide XGA panels at 170 Mb/s when using VESA 60 Hz standard timing.

Features

- Reduced Swing Differential Signalling (RSDS™) digital bus reduces dynamic power, EMI and bus width from the timing controller
- LVDS single pixel input interface system
- Input clock range from 40 MHz to 85 MHz
- Drives RSDS™ Column Drivers at 170 Mb/s with an 85 MHz clock (Max.)
- Virtual 8 bit color depth in FRC/Dithering mode
- Single narrow 9-bit differential Source Driver bus minimizes width of Source PCB
- Ability to drive (SVGA) XGA and Wide XGA TFT-LCD Systems
- Failure detect function in DE mode
- CMOS circuitry operates from a 3.0V–3.6V supply

System Diagram

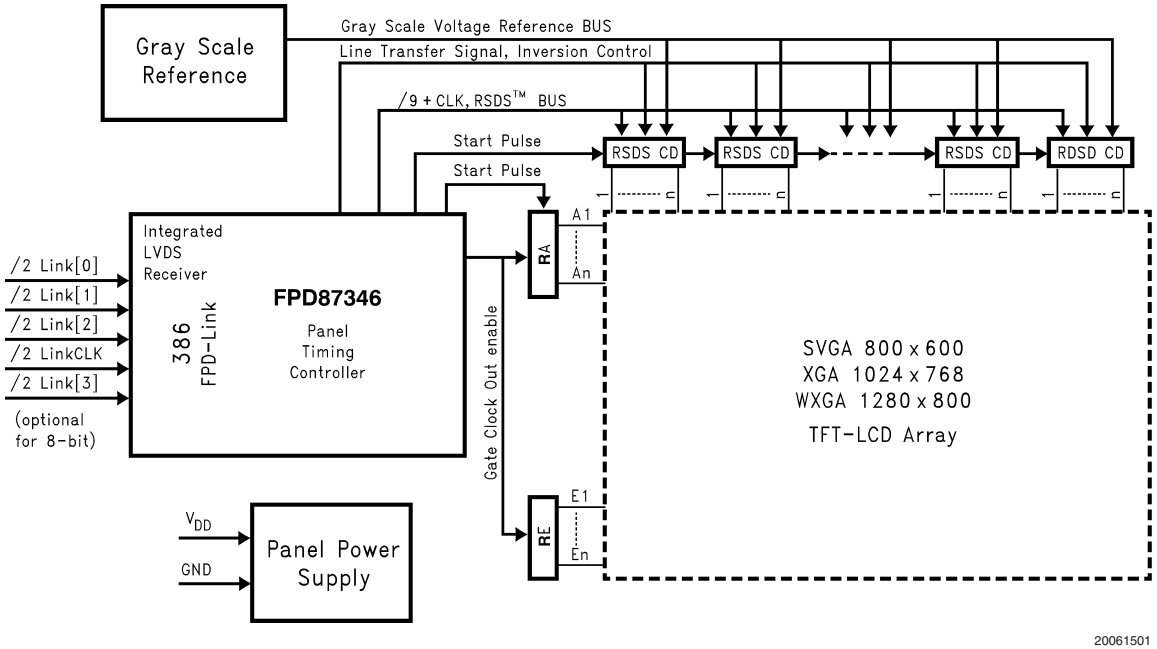


FIGURE 1. Block Diagram of the LCD Module

RSDS™ is a trademark of National Semiconductor Corporation

Block Diagram

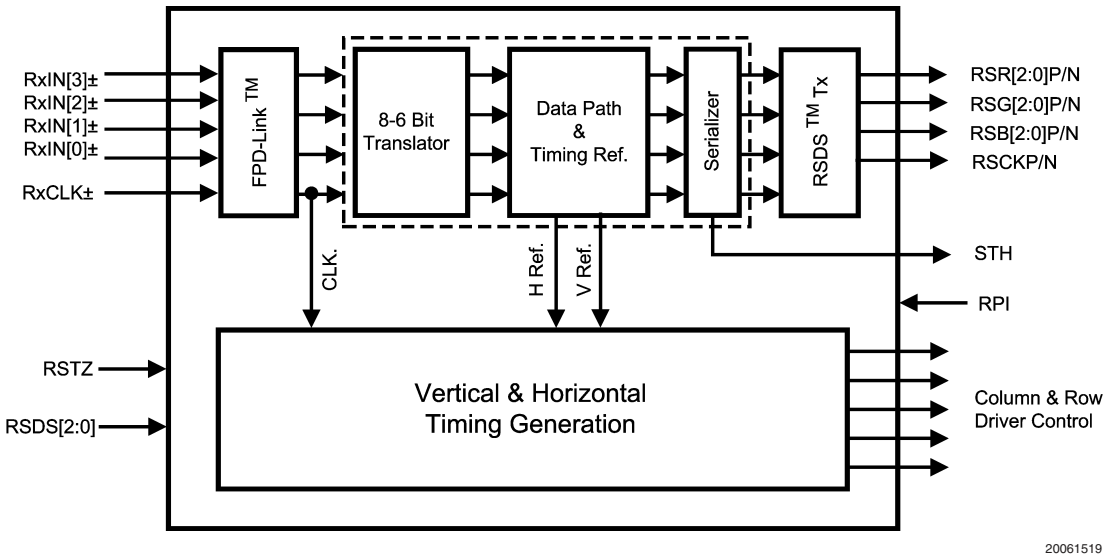


FIGURE 2. Block Diagram

Functional Description

FPD-LINK RECEIVER

The LVDS based FPD-Link Receiver inputs video data and control timing through 4-LVDS channels plus clock to provide 24-bit color or 3-LVDS channels can be used for 18-bit color. The video data is converted to a parallel data stream and routed to the 8-6 bit translator.

SPREAD SPECTRUM SUPPORT

The FPD-Link receiver supports graphics controllers with Spread Spectrum interfaces for reducing EMI. The Spread Spectrum methods supported are Center and Down Spread. A maximum of 2% total is supported at a frequency modulation of 100kHz maximum.

8-6 BIT TRANSLATOR

8-bit data is reduced to a 6-bit data path via a time multiplexed dithering technique or simple truncation of the LSBs. This function is enabled via the input control pins.

DATAPATH BLOCK AND RSDS TRANSMITTER

6(8)-bit video data (RGB) is input to the Datapath Block supports up to an 85 MHz pixel rate. The data is delayed to align the Column Driver Start Pulse (STH) with the Column Driver data. The data bus (RSR[2:0]P/N, RSG[2:0]P/N, RSB[2:0]P/N) outputs at a 170 MHz rate on 9 differential output channels. The clock is output on the RSCKP/N differential pair. The RSDS Column Drivers latch data on both positive and negative edges of the clock. The RSDS output setup/hold timings are also adjustable through the RSDS[2:0] input pins.

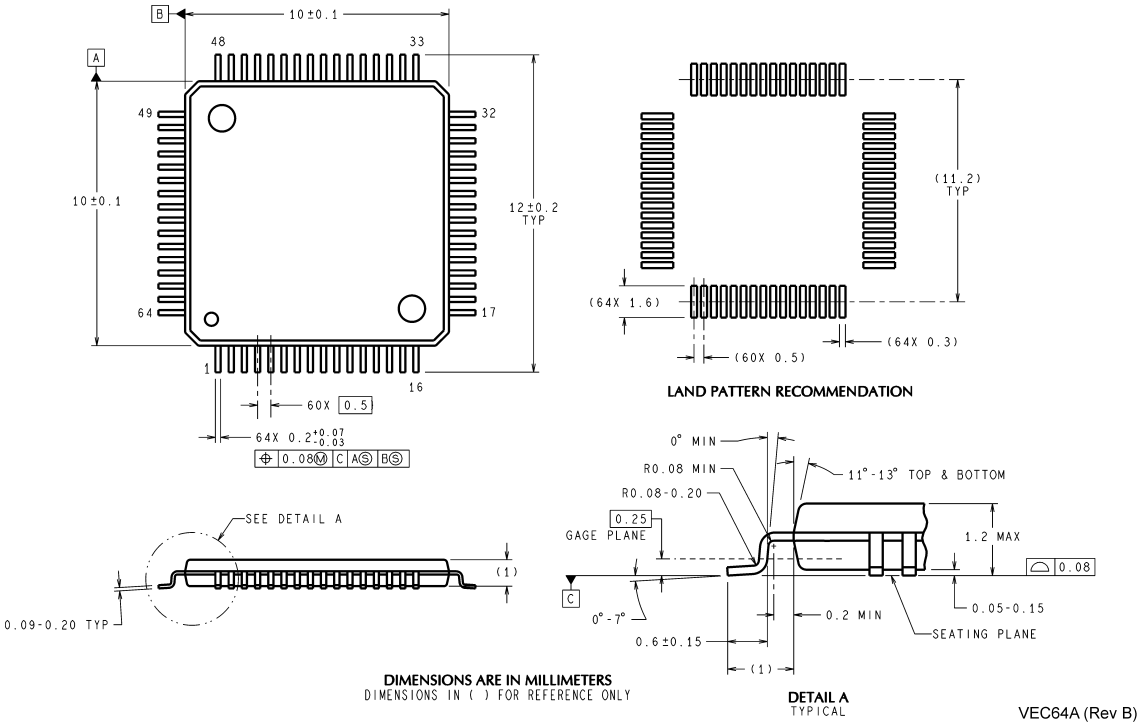
TIMING CONTROL FUNCTION

The Timing Control function generates control to Column Drivers, Row Drivers, and power supply. The GPOs (General Purpose Outputs) provide for CD latch pulse, REV, and Row Driver control generation. The General Purpose Outputs allow the user to generate control anywhere within the frame data. Standard Row Driver interface or Custom Row Driver interfaces can be implemented with the GPOs (General Purpose Outputs).

RSDS OUTPUT VOLTAGE CONTROL

The RSDS output voltage swing is controlled through an external load resistor connected to the R_{PI} pin. The RSDS output signal levels can be adjusted to suit the particular application. This is dependent on overall LCD module design characteristics such as trace impedance, termination, etc. The RSDS output voltage is inversely related to the R_{PI} value. Lower R_{PI} values will increase the RSDS output voltage swing and consequently overall power consumption will also increase.

Physical Dimensions inches (millimeters) unless otherwise noted



64-pin TQFP Package
Order Number FPD87346VS
NS Package Number VEC-64A

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