National Semiconductor™

ADVANCED INFORMATION
NOV, 1997

FPD63310
Universal Interface XGA Panel Timing Controller (UI-XPAT) Reduced Swing Differential Signaling (*RSDS)*

General Description

The FPD63310 is the first TFT-LCD timing controller that combines at TTL single pixel system interface with National's Reduced Swing Differential Signaling (RSDS) source driver interface. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for XGA and SVGA TFT-LCD panels.

The RSDS path to the source or column drivers contributes toward lowing radiated EMI, reducing system power consumption and eliminates one of the pixel busses used in typical XGA TFT-LCD panels today.

This single 9-bit differential bus conveys the 18-bit color data for XGA panels at 130Mb/s when using VESA 60Hz standard timing.

With the addition of a single National DS90CF364 or 564 FPD-LINK ™ chip, the entire data path is optimized for reduced EMI, power consumption and width..

Feature

- Reduced Swing Differential Signaling (RSDS)™ source driver bus for low power and reduced EMI
- Universal TTL single pixel system interface
- Drives National Semiconductor RSDS Column Drivers at 130Mb/s with a 65 MHz clock
- Optional EEPROM programming allows fine tuning in development and production environments.
- Ability to drive SVGA XGA TFT-LCD Systems
- Narrow 9-bit differential Source Driver bus minimizes width of Source PCB
- CMOS circuitry operates from a 3.3V supply.
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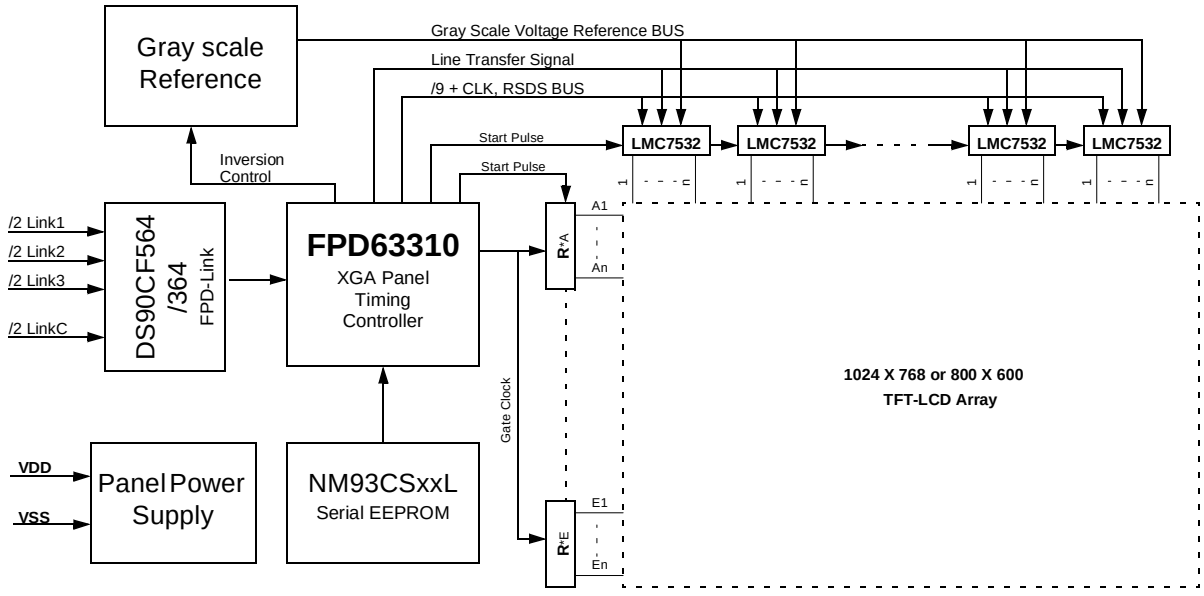
System Diagram

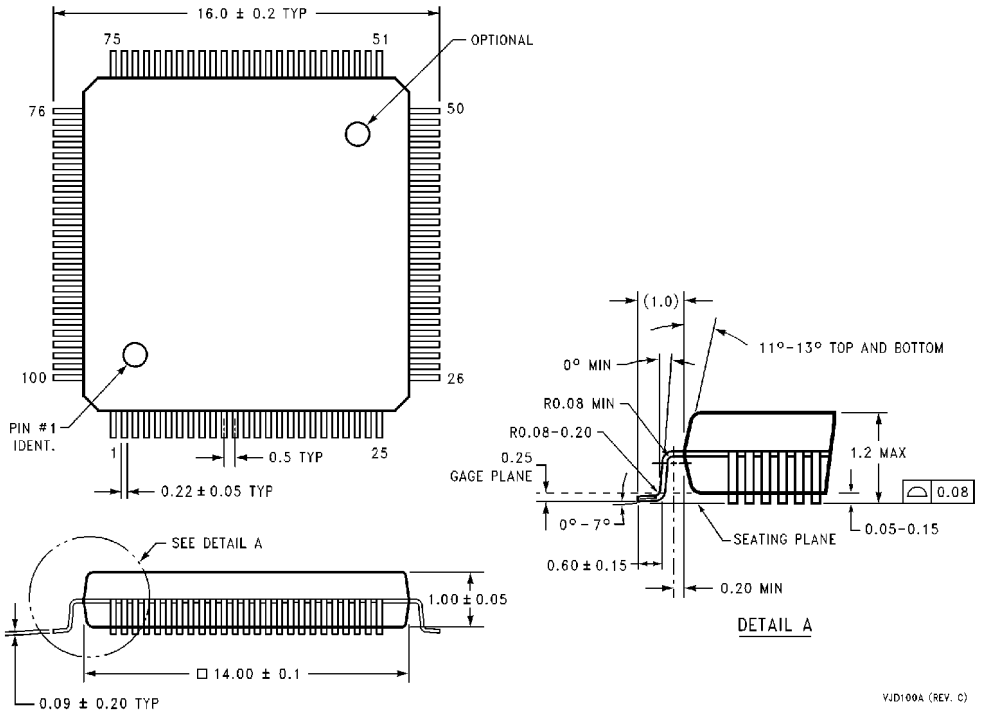


*: Row Driver; LM7403(National Semiconductor)
TMS57600, 1, 4(Texas Instrument)
uPD16650, 2, 4(NEC)

fFPD-LINK ™ is a trademark of National Semiconductor

Package information

Physical Dimension (millimeters)



ThinPlastic Quad Flatpac (JEDEC)(TQFP)
NS package Number VJD100A

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