

## FPD33680

# Low Power, Low EMI, TFT-LCD Column Driver with RSDS Inputs, 64 Grayshades, and 480 Outputs for SXGA/UXGA Applications

## General Description

The FPD33680 is a direct drive, 64 gray level, 480 output, TFT-LCD column driver with an RSDS™ data interface. It provides the capability to display 262,144 colors (18-bit color) with a large dynamic output range for twisted nematic applications. It is targeted to support SXGA applications up to a 75Hz refresh rate and UXGA applications up to a 60Hz refresh rate. Output voltages are gamma corrected to provide a direct mapping between digital video and LCD panel brightness.

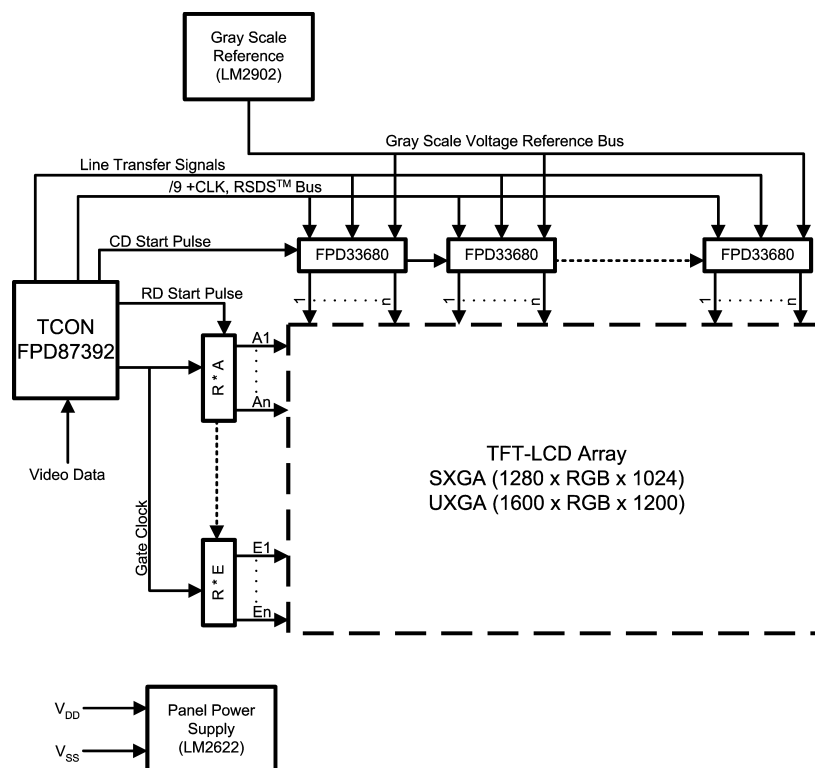
An RSDS (Reduced Swing Differential Signaling) interface is used between the timing controller and the column driver to minimize EMI and reduce power.

The column driver with its interface offers a low power, low EMI column driver solution with direct-drive dynamic range and dot-inversion addressing.

## Features

- RSDS (Reduced Swing Differential Signaling) data bus for low power, reduced EMI and small PCB foot print
- 85MHz maximum operating frequency at  $V_{DD1}=3.0V$
- RSDS pin location and RSDS Switch feature simplify PCB layout and improve EMI
- Ideal for UXGA notebook applications
- Smart Charge Conservation for low power consumption
- 64 Gray levels per color (18-bit color)
- Supports both Dot and N-Line inversion
- Four externally programmable gamma curves
- Very low offsets for artifact free images
- Optional, high current, repair amplifiers

## System Diagram



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## Absolute Maximum Ratings (Note 1)

|                                                                              |                                         |
|------------------------------------------------------------------------------|-----------------------------------------|
| Analog Supply, ( $V_{DD2}$ ) (Note 2)                                        | –0.3V to +11.5V                         |
| Logic Supply, ( $V_{DD1}$ ) (Note 2)                                         | –0.3V to +5.0V                          |
| Low-Polarity RDAC Reference Voltages, ( $V_{GMA6}$ to $V_{GMA10}$ ) (Note 2) | –0.3V to $0.5V_{DD2}$                   |
| High-Polarity RDAC Reference Voltages, ( $V_{GMA1}$ to $V_{GMA5}$ ) (Note 2) | $0.5V_{DD2} - 1.0V$ to $V_{DD2} + 0.3V$ |
| RDAC Current (All Gamma Voltage Taps), ( $I_{GMA}$ to $I_{GMA10}$ )          | –2.5mA to 2.5mA                         |
| Input Voltage (Digital Logic), ( $V_{IN}$ ) (Note 2)                         | –0.3V to $V_{DD1} + 0.3V$               |
| Output Voltage, ( $V_{OUT}$ ) (Note 2)                                       | –0.3V to $V_{DD2} + 0.3V$               |
| Output Current (Analog), ( $I_{OUT}$ )                                       | –7mA to +7mA                            |

Storage Temperature Range, ( $T_S$ ) –55°C to +125°C

**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

**Note 2:** Absolute voltages referenced to  $V_{SS1} = V_{SS2} = 0.0V$ .

## Recommended Operating Conditions

|                                    | Min | Typ | Max  | Units |
|------------------------------------|-----|-----|------|-------|
| Logic Supply Voltage ( $V_{DD1}$ ) | 3.0 | 3.3 | 3.6  | V     |
| Supply Voltage ( $V_{DD2}$ )       | 7.5 |     | 10.5 | V     |
| Operating Temperature ( $T_A$ )    | –10 | +25 | +70  | °C    |

## DC Electrical Characteristics

### Digital Electrical Characteristics

| Symbol    | Parameter                 | Conditions                         | Min             | Typ  | Max           | Units |
|-----------|---------------------------|------------------------------------|-----------------|------|---------------|-------|
| $V_{IH}$  | Logic Input High Voltage  |                                    | $0.7 V_{DD1}$   |      |               | V     |
| $V_{IL}$  | Logic Input Low Voltage   |                                    |                 |      | $0.3 V_{DD1}$ | V     |
| $V_{OH}$  | Logic Output High Voltage | $I_{OH} = -0.5mA$                  | $V_{DD1} - 0.5$ |      |               | V     |
| $V_{OL}$  | Logic Output Low Voltage  | $I_{OL} = 0.5mA$                   |                 |      | 0.5           | V     |
| $I_{DD1}$ | Logic Current             | (Note 3)                           |                 | 10.0 | 15.0          | mA    |
| $I_{IH}$  | Input Leakage             | $V_{DD1} = 3.6V$ , $V_{IN} = 3.6V$ | –1              |      | 1             | μA    |
| $I_{IL}$  | Input Leakage             | $V_{DD1} = 3.6V$ , $V_{IN} = 0V$   | –1              |      | 1             | μA    |
| $C_{IN}$  | Input Capacitance         | All logic pins                     |                 | 2    |               | pF    |

**Note 3:** CLK frequency = 81MHz,  $V_{DD1} = 3.3V$ ,  $V_{SS1} = V_{SS2} = 0.0V$ , line time = 13.3μs, data = all 1's for 4 lines followed by all 0's for 4 lines.

## RSDS Characteristics

| Symbol          | Parameter                            | Conditions                                                                       | Min             | Typ  | Max             | Units |
|-----------------|--------------------------------------|----------------------------------------------------------------------------------|-----------------|------|-----------------|-------|
| $V_{IH_{RSDS}}$ | RSDS High Input Voltage              | $V_{CM_{RSDS}} = 1.2V$ (Note 4) see <i>Figure 1</i>                              | 100             | 200  |                 | mV    |
| $V_{IL_{RSDS}}$ | RSDS Low Input Voltage               | $V_{CM_{RSDS}} = 1.2V$ (Note 4) see <i>Figure 1</i>                              |                 | –200 | –100            | mV    |
| $V_{CM_{RSDS}}$ | RSDS Common Mode Input Voltage Range | $V_{IH_{RSDS}} = +100mV$ , $V_{IL_{RSDS}} = -100mV$ (Note 5) see <i>Figure 1</i> | $V_{SS1} + 0.1$ |      | $V_{DD1} - 1.3$ | V     |
| IDL             | RSDS Input Leakage Current           | DxxP, DxxN, CLKP, CLKN                                                           | –10             |      | 10              | μA    |

**Note 4:**  $V_{CM_{RSDS}} = (V_{CLKP} + V_{CLKN})/2$  or  $(V_{DxxP} + V_{DxxN})/2$ .

**Note 5:**  $V_{IH_{RSDS}}$  and  $V_{IL_{RSDS}}$  are referenced to  $V_{CM_{RSDS}}$

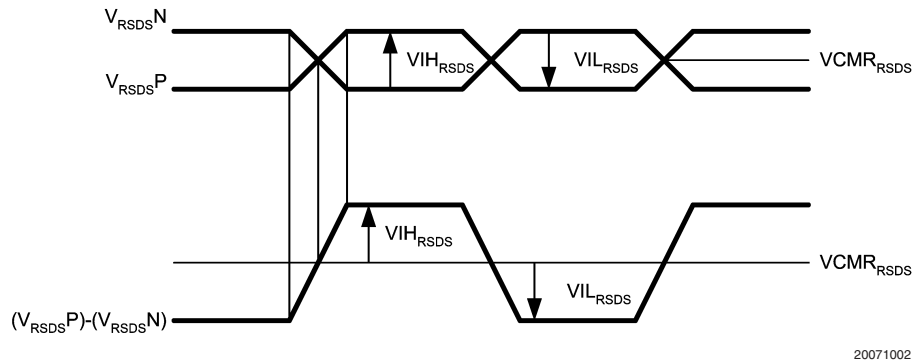


FIGURE 1. RSDS Signal Definition

## Analog Electrical Characteristics

| Symbol        | Parameter                                                                  | Conditions                                                  | Min               | Typ     | Max               | Units      |
|---------------|----------------------------------------------------------------------------|-------------------------------------------------------------|-------------------|---------|-------------------|------------|
| $I_{DD2}$     | Supply Current Consumption                                                 | (Note 6)                                                    |                   | 8.0     | 15.0              | mA         |
| $V_{GMA1}$    | Upper RDAC High Side Input                                                 | (Note 7)                                                    | $V_{DD2}/2 + 0.2$ |         | $V_{DD2} - 0.2$   | V          |
| $V_{GMA5}$    | Upper RDAC Low Side Input                                                  | (Note 7)                                                    | $V_{DD2}/2 + 0.2$ |         | $V_{DD2} - 0.2$   | V          |
| $V_{GMA6}$    | Lower RDAC High Side Input                                                 | (Note 7)                                                    | 0.2               |         | $V_{DD2}/2 - 0.2$ | V          |
| $V_{GMA10}$   | Lower RDAC Low Side Input                                                  | (Note 7)                                                    | 0.2               |         | $V_{DD2}/2 - 0.2$ | V          |
| $C_{LOAD}$    | Output Capacitive Load                                                     |                                                             | 30                |         | 150               | pF         |
| $V_{OUT}$     | Output Voltage Range                                                       |                                                             | $V_{SS2} + 0.2$   |         | $V_{DD2} - 0.2$   | V          |
| $R_{DAC}$     | RDAC References ( $V_{GMA1}$ to $V_{GMA5}$ and $V_{GMA6}$ to $V_{GMA10}$ ) | each                                                        | 12.0              | 15.0    | 18.0              | k $\Omega$ |
| $V_{pperr}$   | Output Peak to Peak Error (gray levels 0 through 58)                       | $V_{GMA1} = V_{DD2} - TBDV$<br>$V_{GMA10} = V_{SS2} + TBDV$ |                   | $\pm 3$ | $\pm 10$          | mV         |
|               | Output Peak to Peak Error (gray levels 59 through 63)                      | (Note 8)                                                    |                   | $\pm 5$ | $\pm 15$          | mV         |
| $V_{parterr}$ | Output Part to Part Error                                                  | (Note 9)                                                    |                   |         | $\pm 5$           | mV         |
| $I_{OUT RP}$  | Repair Buffer Output Current                                               | (Note 10)                                                   | $\pm 2$           | $\pm 3$ |                   | mA         |

**Note 6:**  $V_{DD2} = 10V$ ,  $V_{DD1} = 3.3V$ ,  $f_{CLK} = 81MHz$ , line time = 13.3 $\mu$ sec, data = maximum output swing (GMA1 to GMA10), [TIME1, TIME0] = [0,1] (charge sharing of 32 clock cycles)

**Note 7:** The following relationship must be maintained between the reference voltages:  $V_{DD2} > V_{GMA1} > V_{GMA2} > V_{GMA3} > V_{GMA4} > V_{GMA5} > V_{GMA6} > V_{GMA7} > V_{GMA8} > V_{GMA9} > V_{GMA10} > V_{SS2}$

**Note 8:**  $V_{pperr}$  is meant to reflect the error in peak-to-peak output voltage for each gray level when the output swings from the high value  $V_{Hxx}$  to the low value  $V_{Lxx}$ . This parameter applies to every output on the die. The typical value represents one standard deviation from ideal based on tester data. The maximum value is a constraint of the test environment, not the performance of the part.

**Note 9:**  $V_{parterr}$  is meant to guarantee the part-to-part output variation. The average of all outputs at gray level 32 is compared to a nominal gray level 32 value. The difference is  $V_{parterr}$ .

**Note 10:** Current into device pins is defined as positive. Current out of device pins is defined as negative.  $|V_{OUT} - V_{IN}| > 500mV$ .

## AC Electrical Characteristics

### Digital AC Characteristics

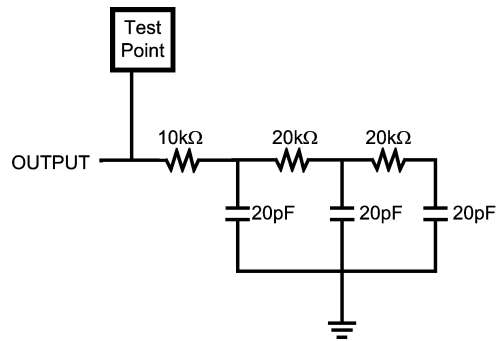
| Symbol         | Parameter                | Conditions                | Min         | Typ | Max      | Units      |
|----------------|--------------------------|---------------------------|-------------|-----|----------|------------|
| $PW_{CLK}$     | Clock Period             | $V_{DD1} = 3.0$ to $3.6V$ | 11.7        |     |          | ns         |
| $PW_{CLK(L)}$  | Low Clock Pulse Width    |                           | 40%         |     | 60%      | $PW_{CLK}$ |
| $PW_{CLK(H)}$  | High Clock Pulse Width   |                           | 40%         |     | 60%      | $PW_{CLK}$ |
| $t_{setup1}$   | RSDS Data Setup Time     |                           | 2           |     |          | ns         |
| $t_{hold1}$    | RSDS Data Hold Time      |                           | 0           |     |          | ns         |
| $t_{setup2}$   | ENIOx Setup Time         |                           | 2           |     |          | ns         |
| $t_{hold2}$    | ENIOx Hold Time          |                           | 4           |     |          | ns         |
| $t_{PLH1}$     | Start Pulse Fall Delay   | $C_{LINE} = 15$ pF        |             |     | 8        | ns         |
| $PW_{DIO}$     | ENIOx Pulse Width        |                           | 1           |     | 2        | $PW_{CLK}$ |
| $PW_{CLK1}$    | LOAD Pulse Width         |                           | $5 T_{CLK}$ |     | $5\mu s$ |            |
| $t_{LDT}$      | Last Clock to LOAD Delay |                           | 1           |     |          | $PW_{CLK}$ |
| $t_{DENSU}$    | LOAD to First ENIO Setup |                           | 2           |     |          | $PW_{CLK}$ |
| $t_{POL-CLK1}$ | POL-CLK1 Time            |                           | 14          |     |          | ns         |

### Analog AC Characteristics

Supplies:  $V_{SS1} = V_{SS2} = 0.0V$ ,  $V_{DD1} = 3.3V$ ,  $V_{DD2} = +10.0V$ .

| Symbol                | Parameter                                              | Conditions                     | Min | Typ | Max | Units   |
|-----------------------|--------------------------------------------------------|--------------------------------|-----|-----|-----|---------|
| $t_{settle\ 90\%}$    | Output Settling Time to 90% of Final Value             | Figure 2 (Note 11)             |     |     | 6   | $\mu s$ |
| $t_{6-bit\ accy}$     | Output Settling Time to 6-bit accuracy                 | (Note 11)                      |     |     | 10  | $\mu s$ |
| $t_{RP\ 90\%}$        | Repair Line Output Settling Time to 90% of Final Value | $C_{LOAD} = 150$ pF, (Note 11) |     |     | 6   | $\mu s$ |
| $t_{RP\ 6-bit\ accy}$ | Repair Line Output Settling Time to 6-bit accuracy     | $C_{LOAD} = 150$ pF, (Note 11) |     |     | 10  | $\mu s$ |

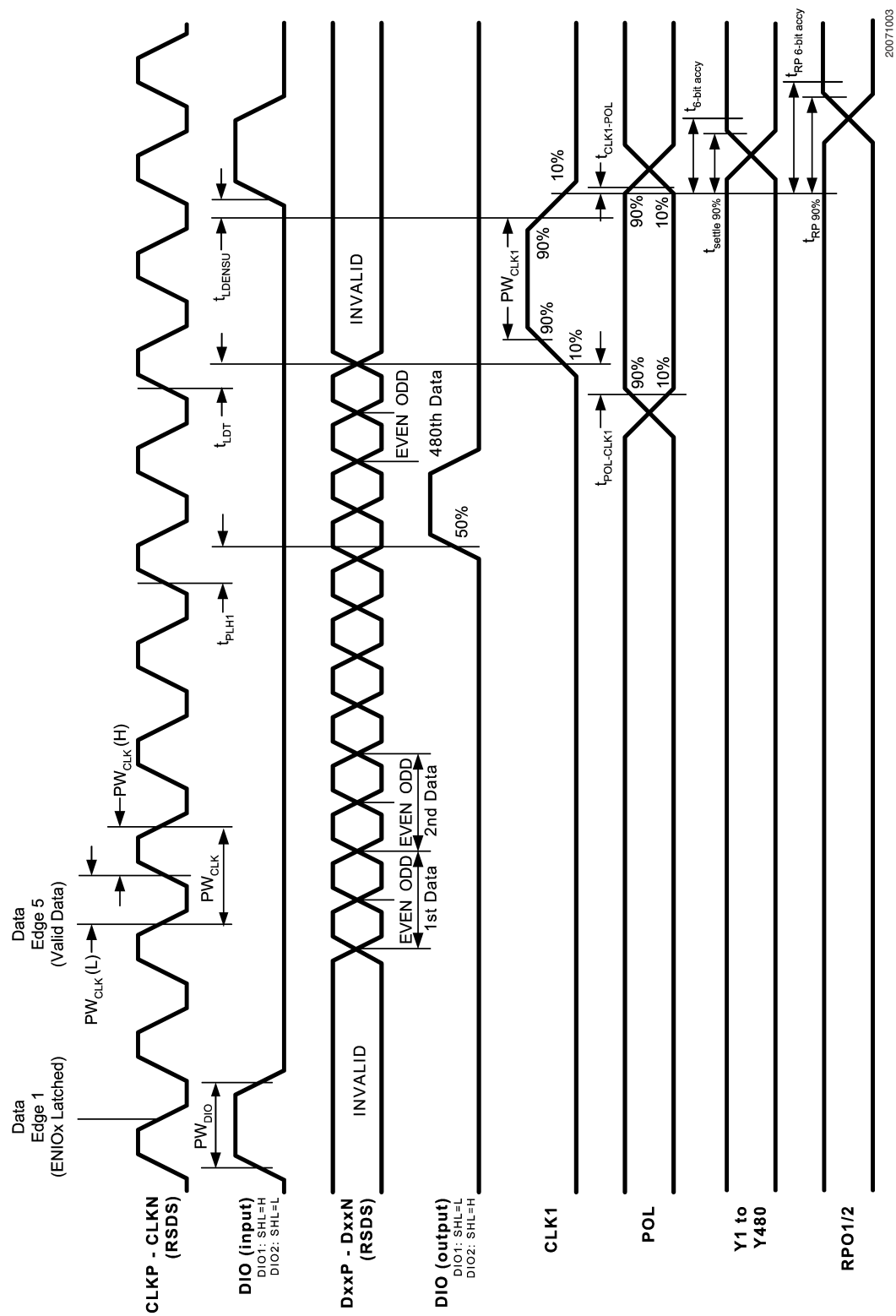
**Note 11:**  $V_{GMA1} = 9.8V$ ,  $V_{GMA10} = 0.2V$ ,  $V_{GMA5} = 5.2V$ ,  $V_{GMA6} = 4.8V$ , [TIME0, TIME1] = [0,1].



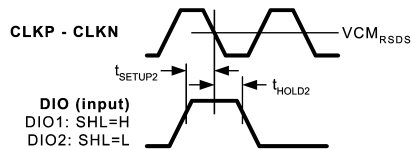
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**FIGURE 2. Test Circuit for Output Settling Time Measurements**

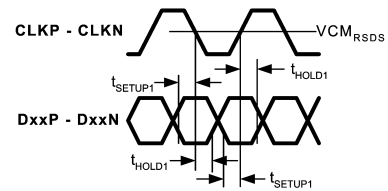
## Timing Diagrams



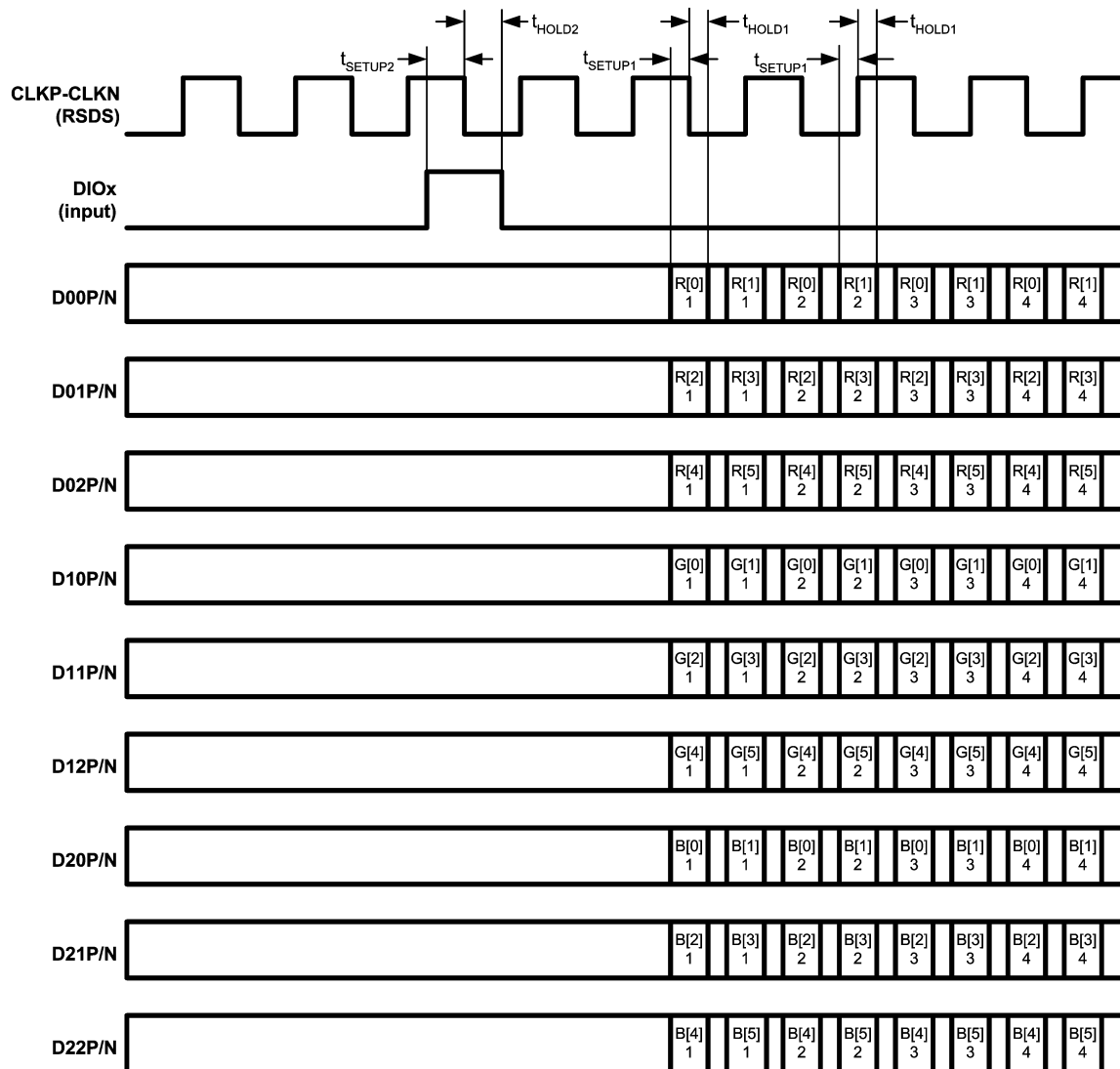
## Timing Diagrams (Continued)



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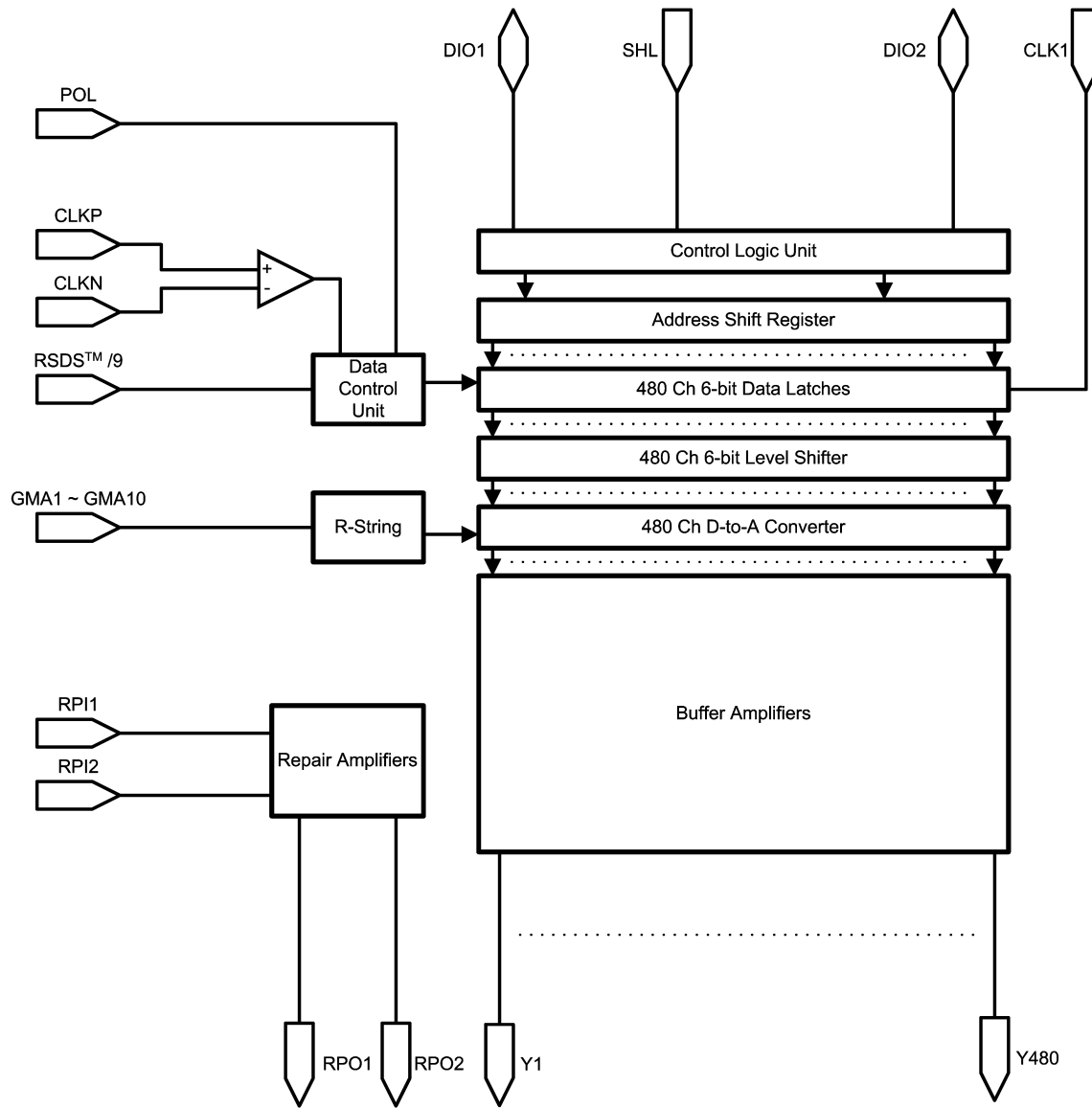


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## Block Diagram



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## Functional Description

### GENERAL OVERVIEW

The FPD33680 is a low power, low EMI, 480 output column driver with 64 gray level capability (6-bit). It provides direct drive for TFT-LCD displays, eliminating the need for  $V_{COM}$  modulation. Direct drive significantly reduces system power consumption and also reduces component count while providing superior image quality and cross-talk margin. The FPD33680 utilizes National's *Charge Conservation Technology* that recovers energy stored in the capacitance of the column lines to reduce power consumption further.

The FPD33680 is designed for use in systems using dot inversion. Column inversion and N-line inversion are also supported. Other modes of polarity inversion including line inversion and frame inversion are not supported.

Digital video data inputs to the FPD33680 are received using Reduced Swing Differential Signaling (RSDS™) receiver circuitry integrated into the column driver IC. The RSDS™ digital video commands one of 64 gray level voltages on

each output. Output voltages are driven with individual high drive, low offset, operational amplifiers. Data loading and line buffering is accomplished by means of an internal, bi-directional shift register.

### GAMMA CORRECTION

The FPD33680 is designed to offer compatibility with a wide range of panel gamma characteristics. The output voltage levels corresponding to each of the 64 gray level commands can be externally adjusted to match the desired gamma characteristics of the display by means of two internal resistor-string DACs (RDACs). One RDAC provides the high-polarity output voltages (voltages higher than  $V_{com}$ ) and the other provides the low-polarity output voltages (voltages lower than  $V_{com}$ ).

The FPD33680 R-DAC resistance curve has been carefully designed to accurately match the natural, inverse gamma of a twisted nematic (TN) display with a 2.2 gamma transfer

## Functional Description (Continued)

characteristic. Additional, custom gamma curves can be requested through your National Semiconductor representative. A typical TN display, when operated with the FPD33680 drivers will produce a luminance with grayscale characteristic typical of CRT monitors. The resistor values for the R-DAC are shown in Figure 7. The individual R-DAC characteristics can be found in Figure 4, Figure 5, and Figure 6.

Most applications will only need to provide references for each of the two ends of the two R-DACs (GMA1, GMA5, GMA6, and GMA10). Six additional, intermediate R-DAC tap points are available for further customization.

### CHARGE CONSERVATION TECHNOLOGY

National Semiconductor's proprietary charge conservation technology significantly reduces power consumption. Charge conservation works by briefly switching all of the columns to a common node at the start of each line. This has the effect of redistributing the charge stored in the capacitance of the panel columns. Because half the columns are at voltages more positive than  $V_{com}$  and half are more negative, this redistribution of charge or "charge-sharing" has the effect of pulling all of the columns to a neutral voltage near the middle of the driver's dynamic range. Thus, the voltages on all the columns are driven approximately halfway toward their next value with no power expended. This dramatically reduces panel power dissipation (up to a theoretical limit of 50%) compared to conventional drivers which must drive each column through the entire voltage swing every time polarity is reversed.

'Smart' charge sharing is used to further optimize this feature. Data inversion is monitored and charge shared only across data ranges (i.e. when output polarity changes between adjacent lines). This is useful during n-line inversion when polarity changes do not occur at every line transition.

As shown in Figure 3, charge sharing begins at the falling edge of CLK1 and continues for the number of RSDS clock cycles shown in Table 1. For more information on National's proprietary Smart Charge Sharing technology, please see application note *AN1235 Using Smart Charge Sharing to Reduce Power and Boost Column Driver Performance*, which is available on the National Semiconductor website or through your National Semiconductor representative.

The amount of charge share time is determined by 2 pins: TIME0 and TIME1. Both TIME0 and TIME1 pins default to a low state, so if both pins are left floating, the charge share time will be 16 RSDS clock cycles. The average panel should set charge sharing at either 32 RSDS clocks or 64 RSDS clocks, depending on the data rate and the panel load. Panels with much larger RC loads may need to increase the charge share time to get the maximum benefit and panels with a smaller load can realize power savings with a shorter charge share time. Please contact National Semiconductor if you need further assistance in selecting a charge share time.

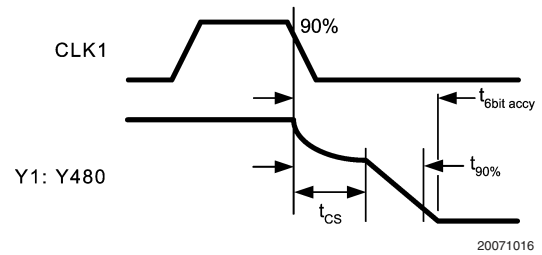


FIGURE 3. FPD33680 Charge Share Timing

TABLE 1. Charge Sharing Definition

| TIME0 | TIME1 | Charge Share Time                    |
|-------|-------|--------------------------------------|
| 0     | 0     | 16 RSDS CLKs (approx. 250ns @ 65MHz) |
| 0     | 1     | 32 RSDS CLKs (approx. 500ns @ 65MHz) |
| 1     | 0     | 64 RSDS CLKs (approx. 1μs @ 65MHz)   |
| 1     | 1     | 128 RSDS CLKs (approx. 2μs @ 65MHz)  |

### RSDS DATA CHANNEL

The RSDS data bus is comprised of nine channels and a common clock. Each channel consists of a two wire differential pair. The nine channels carry digital video data organized as three busses of three channels. Each three channel bus corresponds on one of the three video colors, red, green and blue. The three video busses are comprised of a most, middle and least significant bit. The six bit video word is carried on the three wires of each video bus in two consecutive half words. The even fields of the word are transmitted-received on a first clock and are followed by the odd fields on the following clock transition. Clocking is dual edge and the clock signal is also carried on a two wire, differential pair.

### PIN SWAP AND PIN ORDER

The FPD33680 comes with advanced features to simplify the PCB routing and reduce EMI. The first improvement is the organization of the input pins. In the industry standard RSDS pinout, the RSDS bus is split into 3 sections across the inputs and is interrupted by power and ground signals as well as TTL level signals. The FPD33680 groups all of the RSDS signals together. The power and gamma inputs are grouped together and the low speed TTL signals are grouped together. This makes PCB routing easier. The second feature is the RSDS Swap. This allows the number of corners in the RSDS bus to be cut in half. From one column driver to the next, the order of the RSDS input pins is reversed, allowing the RSDS bus to be routed more efficiently. The pin definitions are shown in Table 2.

### OPTIONAL REPAIR AMPLIFIERS

The FPD33680 provides two general purpose, unity gain output buffers, one located at each end of the input bank of the die. These buffers may be used to repair an open in a column line. The drive signal from the output of the faulted line can be stitched to the input of the repair buffer during the repair process. The output of the repair buffer is then routed to the other side of the column line making it possible to maintain fast rise and fall times on both ends of the afflicted column line.



## Functional Description (Continued)

### PIN DESCRIPTIONS

The pin order configuration for the FPD33680 is shown in *Figure 8*.

#### CLKP and CLKN — Data Clock (input)

Differential clock input for RSDS™ data loading. Note that when RSDS\_SW is tied to  $V_{SS1}$ , the polarity of CLKP and CLKN is reversed (i.e. the CLKP input should be connected to the TCON CLKN output and the CLKN input should be connected to the TCON CLKP output).

#### RSDS\_SW — RSDS Swap (Input)

The RSDS\_SW pin controls the definition of the RSDS data input pins to provide for optimal PCB routing. When tied to  $V_{DD1}$  or left floating, the RSDS input pins are in their default state. When the RSDS\_SW pin is tied to  $V_{SS2}$ , the input pins are in their alternate configuration as shown in *Table 2*

#### DxxP/N — RSDS Data Bus (input)

RSDS™ data input pins. The definitions are controlled by the state of the RSDS\_SW pin as shown in *Table 2*. Note that the polarity of the RSDS signals also reverses (i.e. CLKP—CLKN).

**TABLE 2. RSDS Input Pin Configuration**

| RSDS™ Input | RSDS_SW = NC or $V_{DD1}$ | RSDS_SW = $V_{SS}$ |
|-------------|---------------------------|--------------------|
| RSDS0P      | BLUE[2]P                  | NC                 |
| RSDS0N      | BLUE[2]N                  | NC                 |
| RSDS1P      | BLUE[1]P                  | NC                 |
| RSDS1N      | BLUE[1]N                  | NC                 |
| RSDS2P      | BLUE[0]P                  | NC                 |
| RSDS2N      | BLUE[0]N                  | NC                 |
| RSDS3P      | GREEN[2]P                 | RED[0]N            |
| RSDS3N      | GREEN[2]N                 | RED[0]P            |
| RSDS4P      | GREEN[1]P                 | RED[1]N            |
| RSDS4N      | GREEN[1]N                 | RED[1]P            |
| RSDS5P      | GREEN[0]P                 | RED[2]N            |
| RSDS5N      | GREEN[0]N                 | RED[2]P            |
| CLKP        | CLKP                      | CLKN               |
| CLKN        | CLKN                      | CLKP               |
| RSDS6P      | RED[2]P                   | GREEN[0]N          |
| RSDS6N      | RED[2]N                   | GREEN[0]P          |
| RSDS7P      | RED[1]P                   | GREEN[1]N          |
| RSDS7N      | RED[1]N                   | GREEN[1]P          |
| RSDS8P      | RED[0]P                   | GREEN[2]N          |
| RSDS8N      | RED[0]N                   | GREEN[2]P          |
| RSDS9P      | NC                        | BLUE[0]N           |
| RSDS9N      | NC                        | BLUE[0]P           |
| RSDS10P     | NC                        | BLUE[1]N           |
| RSDS10N     | NC                        | BLUE[1]P           |
| RSDS11P     | NC                        | BLUE[2]N           |
| RSDS11N     | NC                        | BLUE[2]P           |

#### CLK1 — Data Load (input)

The rising edge of CLK1 copies the digital video buffered by the shift register into a second latch for conversion to analog. The falling edge of CLK1 begins charge sharing.

#### POL — Polarity (input)

When POL is low, odd numbered outputs (1, 3, 5, . . . 383) are controlled by VGMA6 through VGMA10 and even numbered outputs are controlled by VGMA1 through VGMA5. When POL is high, odd numbered outputs are controlled by VGMA1 through VGMA5 and even numbered outputs are controlled by VGMA6 through VGMA10. The POL signal for line #n is sampled at the rising edge of CLK1 on line # n–1.

#### DIO1/DIO2 — Data Loading Enable 1 and 2 (I/O)

The DIO1 and DIO2 pins allow several FPD33680 column drivers to be daisy chained together. The start pulse (SP or STH) from the timing controller is connected to the input DIOx pin on the first column driver in the chain. The input DIO for the remaining column drivers in the chain are connected to the output DIO from the preceding column driver. The SHL pin controls whether DIO1 or DIO2 is configured as the input.

If SHL is high, then the DIO1 pin is configured as an input and the DIO2 pin as an output. If SHL is low, the DIO2 pin is configured as an input and the DIO1 pin as an output.

The input DIOx pin is latched on the falling edge of the CLKP signal.

#### DATPOL — Digital Data Invert (input)

When DATPOL is high, RSDS data is inverted. The DATPOL pin can be tied either high or low through connection to a neighboring pin on a custom package eliminating the need to connect the pin to the PCB.

#### SHL — Data Shift Direction (input)

The SHL pin controls the data load direction. When SHL is high, the data is loaded from output 1 to output 480, DIO1 is configured as an input, and DIO2 is configured as an output. When SHL is low, the data is loaded from output 480 to output 1, DIO2 is configured as an input, and DIO1 is configured as an output. The SHL pin can be tied off in the custom package, eliminating the need to connect it to the PCB.

#### RPI1/ RPI2 — Repair Amp Input 1 and 2 (input)

The input signal for the repair line buffers. These buffers are optional and when not used, the input should be tied to ground. RPI1 and RPI2 can be tied to ground with a connection in the package, eliminating the need to connect them to the PCB.

#### RPO1/ RPO2 — Repair Amp Output 1 and 2 (output)

The output of the repair line buffers. These outputs are current buffered copies of their respective inputs. When not in use, RPO1 and RPO2 can be left unconnected.

#### TIME0/ TIME1 — Charge Share Time Select Pins (input)

The TIME0 and TIME1 pins define the length of charge share time. *Table 1* lists the charge share time options defined by TIME0 and TIME1. Both of these pins have internal pull-down resistors and default to a logic low state. They can also be tied high in the package, eliminating the need to connect them to the PCB.

#### $V_{GMA1}$ – $V_{GMA10}$ — RDAC References (input)

The reference voltages to the upper and lower RDACs used to control the inverse gamma transfer function of the driver. Option - Any or all of the inputs  $V_{GMA2}$  through  $V_{GMA4}$  and  $V_{GMA7}$  through  $V_{GMA9}$  can be left undriven (floating).

#### $V_{DD1}$ — Digital Voltage Supply (power)

Positive supply voltage for the digital logic functions of the driver. Nominally 3.3V.

#### $V_{DD2}$ — Analog Voltage Supply (power)

**Functional Description** (Continued)

Positive supply voltage for the analog functions of the driver.  
Nominally between 8.0 and 10.0V

**V<sub>SS1</sub>** — *Digital Ground (power)*

Digital ground reference voltage. Typically tied to V<sub>SS2</sub> on the PCB.

**V<sub>SS2</sub>** — *Analog Ground (power)*

Analog ground reference voltage. Typically tied to V<sub>SS1</sub> on the PCB

# Functional Description (Continued)

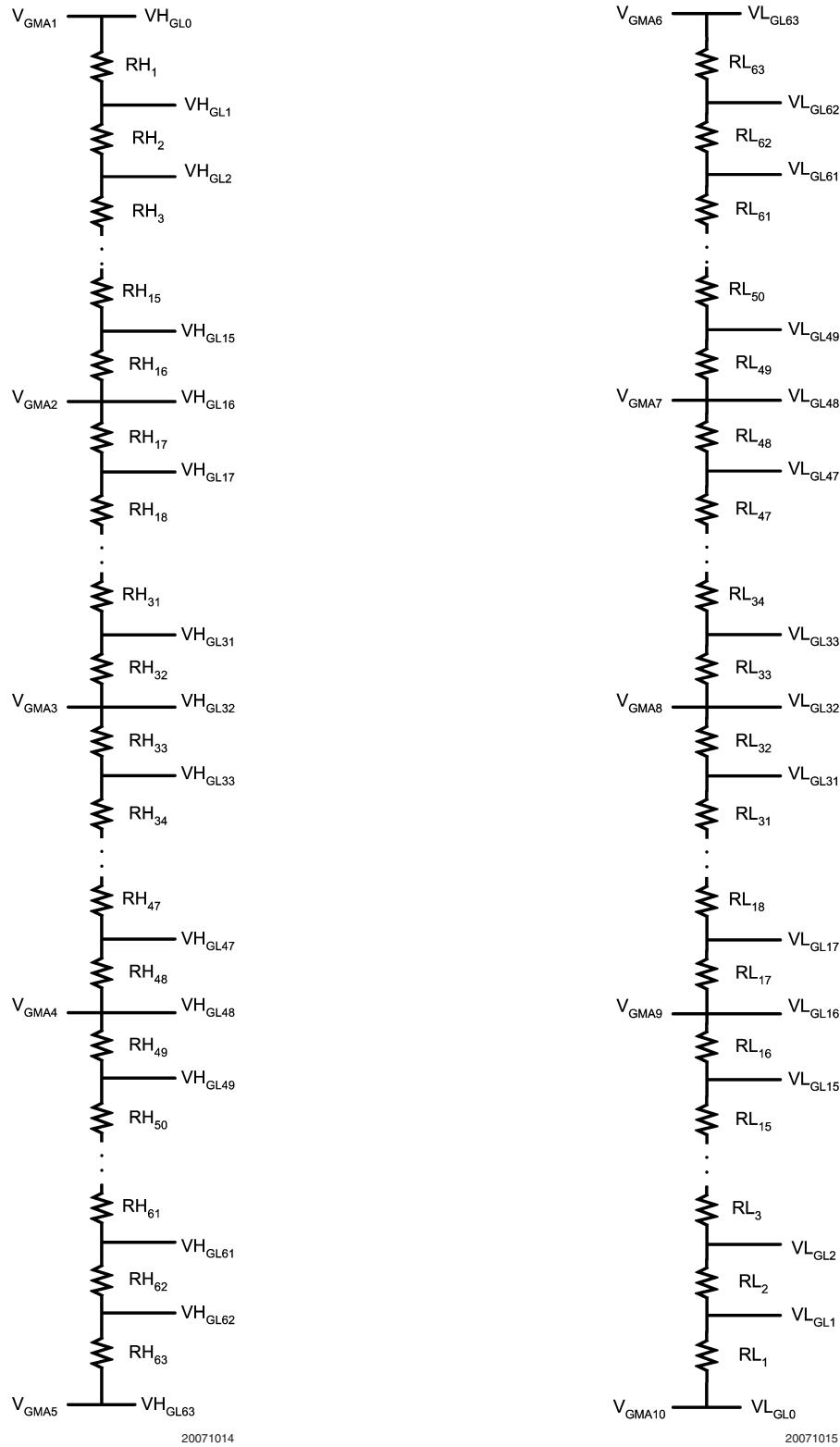


FIGURE 4. FPD33680F R-DAC Configuration

# Functional Description (Continued)

| Data            | Output Voltage (gamma F) |                       |           | Data            | Output Voltage (gamma F) |                      |           |
|-----------------|--------------------------|-----------------------|-----------|-----------------|--------------------------|----------------------|-----------|
| 00 <sub>H</sub> | VL0                      | VGMA10                |           | 20 <sub>H</sub> | VL32                     | VGMA8                |           |
| 01 <sub>H</sub> | VL1                      | VGMA9–(VGMA9–VGMA10)x | 5536/6459 | 21 <sub>H</sub> | VL33                     | VGMA7–(VGMA7–VGMA8)x | 1710/1829 |
| 02 <sub>H</sub> | VL2                      | VGMA9–(VGMA9–VGMA10)x | 4762/6459 | 22 <sub>H</sub> | VL34                     | VGMA7–(VGMA7–VGMA8)x | 1591/1829 |
| 03 <sub>H</sub> | VL3                      | VGMA9–(VGMA9–VGMA10)x | 4152/6459 | 23 <sub>H</sub> | VL35                     | VGMA7–(VGMA7–VGMA8)x | 1472/1829 |
| 04 <sub>H</sub> | VL4                      | VGMA9–(VGMA9–VGMA10)x | 3542/6459 | 24 <sub>H</sub> | VL36                     | VGMA7–(VGMA7–VGMA8)x | 1353/1829 |
| 05 <sub>H</sub> | VL5                      | VGMA9–(VGMA9–VGMA10)x | 3081/6459 | 25 <sub>H</sub> | VL37                     | VGMA7–(VGMA7–VGMA8)x | 1249/1829 |
| 06 <sub>H</sub> | VL6                      | VGMA9–(VGMA9–VGMA10)x | 2620/6459 | 26 <sub>H</sub> | VL38                     | VGMA7–(VGMA7–VGMA8)x | 1145/1829 |
| 07 <sub>H</sub> | VL7                      | VGMA9–(VGMA9–VGMA10)x | 2159/6459 | 27 <sub>H</sub> | VL39                     | VGMA7–(VGMA7–VGMA8)x | 1041/1829 |
| 08 <sub>H</sub> | VL8                      | VGMA9–(VGMA9–VGMA10)x | 1846/6459 | 28 <sub>H</sub> | VL40                     | VGMA7–(VGMA7–VGMA8)x | 937/1829  |
| 09 <sub>H</sub> | VL9                      | VGMA9–(VGMA9–VGMA10)x | 1533/6459 | 29 <sub>H</sub> | VL41                     | VGMA7–(VGMA7–VGMA8)x | 833/1829  |
| 0A <sub>H</sub> | VL10                     | VGMA9–(VGMA9–VGMA10)x | 1265/6459 | 2A <sub>H</sub> | VL42                     | VGMA7–(VGMA7–VGMA8)x | 714/1829  |
| 0B <sub>H</sub> | VL11                     | VGMA9–(VGMA9–VGMA10)x | 997/6459  | 2B <sub>H</sub> | VL43                     | VGMA7–(VGMA7–VGMA8)x | 595/1829  |
| 0C <sub>H</sub> | VL12                     | VGMA9–(VGMA9–VGMA10)x | 774/6459  | 2C <sub>H</sub> | VL44                     | VGMA7–(VGMA7–VGMA8)x | 476/1829  |
| 0D <sub>H</sub> | VL13                     | VGMA9–(VGMA9–VGMA10)x | 551/6459  | 2D <sub>H</sub> | VL45                     | VGMA7–(VGMA7–VGMA8)x | 357/1829  |
| 0E <sub>H</sub> | VL14                     | VGMA9–(VGMA9–VGMA10)x | 358/6459  | 2E <sub>H</sub> | VL46                     | VGMA7–(VGMA7–VGMA8)x | 238/1829  |
| 0F <sub>H</sub> | VL15                     | VGMA9–(VGMA9–VGMA10)x | 179/6459  | 2F <sub>H</sub> | VL47                     | VGMA7–(VGMA7–VGMA8)x | 119/1829  |
| 10 <sub>H</sub> | VL16                     | VGMA9                 |           | 30 <sub>H</sub> | VL48                     | VGMA7                |           |
| 11 <sub>H</sub> | VL17                     | VGMA8–(VGMA8–VGMA9)x  | 1950/2114 | 31 <sub>H</sub> | VL49                     | VGMA6–(VGMA6–VGMA7)x | 4481/4600 |
| 12 <sub>H</sub> | VL18                     | VGMA8–(VGMA8–VGMA9)x  | 1801/2114 | 32 <sub>H</sub> | VL50                     | VGMA6–(VGMA6–VGMA7)x | 4347/4600 |
| 13 <sub>H</sub> | VL19                     | VGMA8–(VGMA8–VGMA9)x  | 1652/2114 | 33 <sub>H</sub> | VL51                     | VGMA6–(VGMA6–VGMA7)x | 4198/4600 |
| 14 <sub>H</sub> | VL20                     | VGMA8–(VGMA8–VGMA9)x  | 1503/2114 | 34 <sub>H</sub> | VL52                     | VGMA6–(VGMA6–VGMA7)x | 4049/4600 |
| 15 <sub>H</sub> | VL21                     | VGMA8–(VGMA8–VGMA9)x  | 1369/2114 | 35 <sub>H</sub> | VL53                     | VGMA6–(VGMA6–VGMA7)x | 3885/4600 |
| 16 <sub>H</sub> | VL22                     | VGMA8–(VGMA8–VGMA9)x  | 1235/2114 | 36 <sub>H</sub> | VL54                     | VGMA6–(VGMA6–VGMA7)x | 3706/4600 |
| 17 <sub>H</sub> | VL23                     | VGMA8–(VGMA8–VGMA9)x  | 1101/2114 | 37 <sub>H</sub> | VL55                     | VGMA6–(VGMA6–VGMA7)x | 3527/4600 |
| 18 <sub>H</sub> | VL24                     | VGMA8–(VGMA8–VGMA9)x  | 967/2114  | 38 <sub>H</sub> | VL56                     | VGMA6–(VGMA6–VGMA7)x | 3348/4600 |
| 19 <sub>H</sub> | VL25                     | VGMA8–(VGMA8–VGMA9)x  | 833/2114  | 39 <sub>H</sub> | VL57                     | VGMA6–(VGMA6–VGMA7)x | 3125/4600 |
| 1A <sub>H</sub> | VL26                     | VGMA8–(VGMA8–VGMA9)x  | 714/2114  | 3A <sub>H</sub> | VL58                     | VGMA6–(VGMA6–VGMA7)x | 2887/4600 |
| 1B <sub>H</sub> | VL27                     | VGMA8–(VGMA8–VGMA9)x  | 595/2114  | 3B <sub>H</sub> | VL59                     | VGMA6–(VGMA6–VGMA7)x | 2619/4600 |
| 1C <sub>H</sub> | VL28                     | VGMA8–(VGMA8–VGMA9)x  | 476/2114  | 3C <sub>H</sub> | VL60                     | VGMA6–(VGMA6–VGMA7)x | 2306/4600 |
| 1D <sub>H</sub> | VL29                     | VGMA8–(VGMA8–VGMA9)x  | 357/2114  | 3D <sub>H</sub> | VL61                     | VGMA6–(VGMA6–VGMA7)x | 1845/2600 |
| 1E <sub>H</sub> | VL30                     | VGMA8–(VGMA8–VGMA9)x  | 238/2114  | 3E <sub>H</sub> | VL62                     | VGMA6–(VGMA6–VGMA7)x | 1235/4600 |
| 1F <sub>H</sub> | VL31                     | VGMA8–(VGMA8–VGMA9)x  | 119/2114  | 3F <sub>H</sub> | VL63                     | VGMA6                |           |

FIGURE 5. FPD33680F Lower Gamma Voltages

# Functional Description (Continued)

| Data            | Output Voltage (gamma F) |                      |           | Data            | Output Voltage (gamma F) |                      |           |
|-----------------|--------------------------|----------------------|-----------|-----------------|--------------------------|----------------------|-----------|
| 00 <sub>H</sub> | VH0                      | VGMA1                |           | 20 <sub>H</sub> | VH32                     | VGMA3                |           |
| 01 <sub>H</sub> | VH1                      | VGMA2+(VGMA1-VGMA2)x | 5536/6459 | 21 <sub>H</sub> | VH33                     | VGMA4+(VGMA3-VGMA4)x | 1710/1829 |
| 02 <sub>H</sub> | VH2                      | VGMA2+(VGMA1-VGMA2)x | 4762/6459 | 22 <sub>H</sub> | VH34                     | VGMA4+(VGMA3-VGMA4)x | 1591/1829 |
| 03 <sub>H</sub> | VH3                      | VGMA2+(VGMA1-VGMA2)x | 4152/6459 | 23 <sub>H</sub> | VH35                     | VGMA4+(VGMA3-VGMA4)x | 1472/1829 |
| 04 <sub>H</sub> | VH4                      | VGMA2+(VGMA1-VGMA2)x | 3542/6459 | 24 <sub>H</sub> | VH36                     | VGMA4+(VGMA3-VGMA4)x | 1353/1829 |
| 05 <sub>H</sub> | VH5                      | VGMA2+(VGMA1-VGMA2)x | 3081/6459 | 25 <sub>H</sub> | VH37                     | VGMA4+(VGMA3-VGMA4)x | 1249/1829 |
| 06 <sub>H</sub> | VH6                      | VGMA2+(VGMA1-VGMA2)x | 2620/6459 | 26 <sub>H</sub> | VH38                     | VGMA4+(VGMA3-VGMA4)x | 1145/1829 |
| 07 <sub>H</sub> | VH7                      | VGMA2+(VGMA1-VGMA2)x | 2159/6459 | 27 <sub>H</sub> | VH39                     | VGMA4+(VGMA3-VGMA4)x | 1041/1829 |
| 08 <sub>H</sub> | VH8                      | VGMA2+(VGMA1-VGMA2)x | 1846/6459 | 28 <sub>H</sub> | VH40                     | VGMA4+(VGMA3-VGMA4)x | 937/1829  |
| 09 <sub>H</sub> | VH9                      | VGMA2+(VGMA1-VGMA2)x | 1533/6459 | 29 <sub>H</sub> | VH41                     | VGMA4+(VGMA3-VGMA4)x | 833/1829  |
| 0A <sub>H</sub> | VH10                     | VGMA2+(VGMA1-VGMA2)x | 1265/6459 | 2A <sub>H</sub> | VH42                     | VGMA4+(VGMA3-VGMA4)x | 714/1829  |
| 0B <sub>H</sub> | VH11                     | VGMA2+(VGMA1-VGMA2)x | 997/6459  | 2B <sub>H</sub> | VH43                     | VGMA4+(VGMA3-VGMA4)x | 595/1829  |
| 0C <sub>H</sub> | VH12                     | VGMA2+(VGMA1-VGMA2)x | 774/6459  | 2C <sub>H</sub> | VH44                     | VGMA4+(VGMA3-VGMA4)x | 476/1829  |
| 0D <sub>H</sub> | VH13                     | VGMA2+(VGMA1-VGMA2)x | 551/6459  | 2D <sub>H</sub> | VH45                     | VGMA4+(VGMA3-VGMA4)x | 357/1829  |
| 0E <sub>H</sub> | VH14                     | VGMA2+(VGMA1-VGMA2)x | 358/6459  | 2E <sub>H</sub> | VH46                     | VGMA4+(VGMA3-VGMA4)x | 238/1829  |
| 0F <sub>H</sub> | VH15                     | VGMA2+(VGMA1-VGMA2)x | 179/6459  | 2F <sub>H</sub> | VH47                     | VGMA4+(VGMA3-VGMA4)x | 119/1829  |
| 10 <sub>H</sub> | VH16                     | VGMA2                |           | 30 <sub>H</sub> | VH48                     | VGMA4                |           |
| 11 <sub>H</sub> | VH17                     | VGMA3+(VGMA2-VGMA3)x | 1950/2114 | 31 <sub>H</sub> | VH49                     | VGMA5+(VGMA4-VGMA5)x | 4481/4600 |
| 12 <sub>H</sub> | VH18                     | VGMA3+(VGMA2-VGMA3)x | 1801/2114 | 32 <sub>H</sub> | VH50                     | VGMA5+(VGMA4-VGMA5)x | 4347/4600 |
| 13 <sub>H</sub> | VH19                     | VGMA3+(VGMA2-VGMA3)x | 1652/2114 | 33 <sub>H</sub> | VH51                     | VGMA5+(VGMA4-VGMA5)x | 4198/4600 |
| 14 <sub>H</sub> | VH20                     | VGMA3+(VGMA2-VGMA3)x | 1503/2114 | 34 <sub>H</sub> | VH52                     | VGMA5+(VGMA4-VGMA5)x | 4049/4600 |
| 15 <sub>H</sub> | VH21                     | VGMA3+(VGMA2-VGMA3)x | 1369/2114 | 35 <sub>H</sub> | VH53                     | VGMA5+(VGMA4-VGMA5)x | 3885/4600 |
| 16 <sub>H</sub> | VH22                     | VGMA3+(VGMA2-VGMA3)x | 1235/2114 | 36 <sub>H</sub> | VH54                     | VGMA5+(VGMA4-VGMA5)x | 3706/4600 |
| 17 <sub>H</sub> | VH23                     | VGMA3+(VGMA2-VGMA3)x | 1101/2114 | 37 <sub>H</sub> | VH55                     | VGMA5+(VGMA4-VGMA5)x | 3527/4600 |
| 18 <sub>H</sub> | VH24                     | VGMA3+(VGMA2-VGMA3)x | 967/2114  | 38 <sub>H</sub> | VH56                     | VGMA5+(VGMA4-VGMA5)x | 3348/4600 |
| 19 <sub>H</sub> | VH25                     | VGMA3+(VGMA2-VGMA3)x | 833/2114  | 39 <sub>H</sub> | VH57                     | VGMA5+(VGMA4-VGMA5)x | 3125/4600 |
| 1A <sub>H</sub> | VH26                     | VGMA3+(VGMA2-VGMA3)x | 714/2114  | 3A <sub>H</sub> | VH58                     | VGMA5+(VGMA4-VGMA5)x | 2887/4600 |
| 1B <sub>H</sub> | VH27                     | VGMA3+(VGMA2-VGMA3)x | 595/2114  | 3B <sub>H</sub> | VH59                     | VGMA5+(VGMA4-VGMA5)x | 2619/4600 |
| 1C <sub>H</sub> | VH28                     | VGMA3+(VGMA2-VGMA3)x | 476/2114  | 3C <sub>H</sub> | VH60                     | VGMA5+(VGMA4-VGMA5)x | 2306/4600 |
| 1D <sub>H</sub> | VH29                     | VGMA3+(VGMA2-VGMA3)x | 357/2114  | 3D <sub>H</sub> | VH61                     | VGMA5+(VGMA4-VGMA5)x | 1845/4600 |
| 1E <sub>H</sub> | VH30                     | VGMA3+(VGMA2-VGMA3)x | 238/2114  | 3E <sub>H</sub> | VH62                     | VGMA5+(VGMA4-VGMA5)x | 1235/4600 |
| 1F <sub>H</sub> | VH31                     | VGMA3+(VGMA2-VGMA3)x | 119/2114  | 3F <sub>H</sub> | VH63                     | VGMA5                |           |

FIGURE 6. FPD33680F Upper Gamma Voltages

## Functional Description (Continued)

| R    | F ( $\Omega$ ) | R                  | F ( $\Omega$ ) |
|------|----------------|--------------------|----------------|
| Rx1  | 923            | Rx33               | 119            |
| Rx2  | 774            | Rx34               | 119            |
| Rx3  | 610            | Rx35               | 119            |
| Rx4  | 610            | Rx36               | 119            |
| Rx5  | 461            | Rx37               | 104            |
| Rx6  | 461            | Rx38               | 104            |
| Rx7  | 461            | Rx39               | 104            |
| Rx8  | 313            | Rx40               | 104            |
| Rx9  | 313            | Rx41               | 104            |
| Rx10 | 268            | Rx42               | 119            |
| Rx11 | 268            | Rx43               | 119            |
| Rx12 | 223            | Rx44               | 119            |
| Rx13 | 223            | Rx45               | 119            |
| Rx14 | 193            | Rx46               | 119            |
| Rx15 | 179            | Rx47               | 119            |
| Rx16 | 179            | Rx48               | 119            |
| Rx17 | 164            | Rx49               | 119            |
| Rx18 | 149            | Rx50               | 134            |
| Rx19 | 149            | Rx51               | 149            |
| Rx20 | 149            | Rx52               | 149            |
| Rx21 | 134            | Rx53               | 164            |
| Rx22 | 134            | Rx54               | 179            |
| Rx23 | 134            | Rx55               | 179            |
| Rx24 | 134            | Rx56               | 179            |
| Rx25 | 134            | Rx57               | 223            |
| Rx26 | 119            | Rx58               | 238            |
| Rx27 | 119            | Rx59               | 268            |
| Rx28 | 119            | Rx60               | 313            |
| Rx29 | 119            | Rx61               | 461            |
| Rx30 | 119            | Rx62               | 610            |
| Rx31 | 119            | Rx63               | 1235           |
| Rx32 | 119            | R <sup>total</sup> | 15000          |

FIGURE 7. FPD33680 R-DAC Resistance Values

# Functional Description (Continued)

| INPUTS   |         | OUTPUTS |      |
|----------|---------|---------|------|
| optional | RPI2    |         | Y480 |
| optional | RPIO2   |         | Y479 |
|          | VDD2    |         | Y478 |
|          | VSS2    |         |      |
|          | DIO2    |         |      |
|          | RSDS0P  |         |      |
|          | RSDS0N  |         | .    |
|          | RSDS1P  |         | .    |
|          | RSDS1N  |         | .    |
|          | RSDS2P  |         | .    |
|          | RSDS2N  |         | .    |
|          | RSDS3P  |         | .    |
|          | RSDS3N  |         | .    |
|          | RSDS4P  |         | .    |
|          | RSDS4N  |         | .    |
|          | RSDS5P  |         | .    |
|          | RSDS5N  |         | .    |
|          | CLKP    |         | .    |
|          | CLKN    |         | .    |
|          | RSDS6P  |         | .    |
|          | RSDS6N  |         | .    |
|          | RSDS7P  |         | .    |
|          | RSDS7N  |         | .    |
|          | RSDS8P  |         | .    |
|          | RSDS8N  |         | .    |
|          | RSDS9P  |         | .    |
|          | RSDS9N  |         | .    |
|          | RSDS10P |         | .    |
|          | RSDS10N |         | .    |
|          | RSDS11P |         | .    |
|          | RSDS11N |         | .    |
|          | GMA10   |         | .    |
| optional | GMA9    |         | .    |
| optional | GMA8    |         | .    |
| optional | GMA7    |         | .    |
|          | GMA6    |         | .    |
|          | GMA5    |         | .    |
| optional | GMA4    |         | .    |
| optional | GMA3    |         | .    |
| optional | GMA2    |         | .    |
|          | GMA1    |         | .    |
|          | VSS1    |         | .    |
|          | VDD1    |         |      |
|          | CLK1    |         |      |
|          | POL     |         |      |
| optional | RSDS_SW |         |      |
| optional | SHL     |         |      |
| optional | DATPOL  |         |      |
|          | DIO1    |         | .    |
|          | VDD2    |         |      |
|          | VSS2    |         | Y3   |
| optional | RPO1    |         | Y2   |
| optional | RPI1    |         | Y1   |

**Note:** This figure represents a FPD33680 die oriented pad side up.

**FIGURE 8. FPD33680 I/O Configuration**

## Ordering Information

| Part Number | Gamma Curve | Custom Package # | Package Suffix | Package Type |
|-------------|-------------|------------------|----------------|--------------|
| FPD33680    | F           | XX               | CT             | TCP          |
| FPD33680    | F           | XX               | CF             | COF          |

**Note 12:** Custom Package # is assigned by National Semiconductor for each custom TCP or COF design

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