National Semiconductor

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FPD03784
Low Power, Low EMI, TFT-LCD Column Driver with Dual, TTL Bus Inputs, 64 Grayshades, and 384 Outputs for XGA/SXGA Applications

General Description

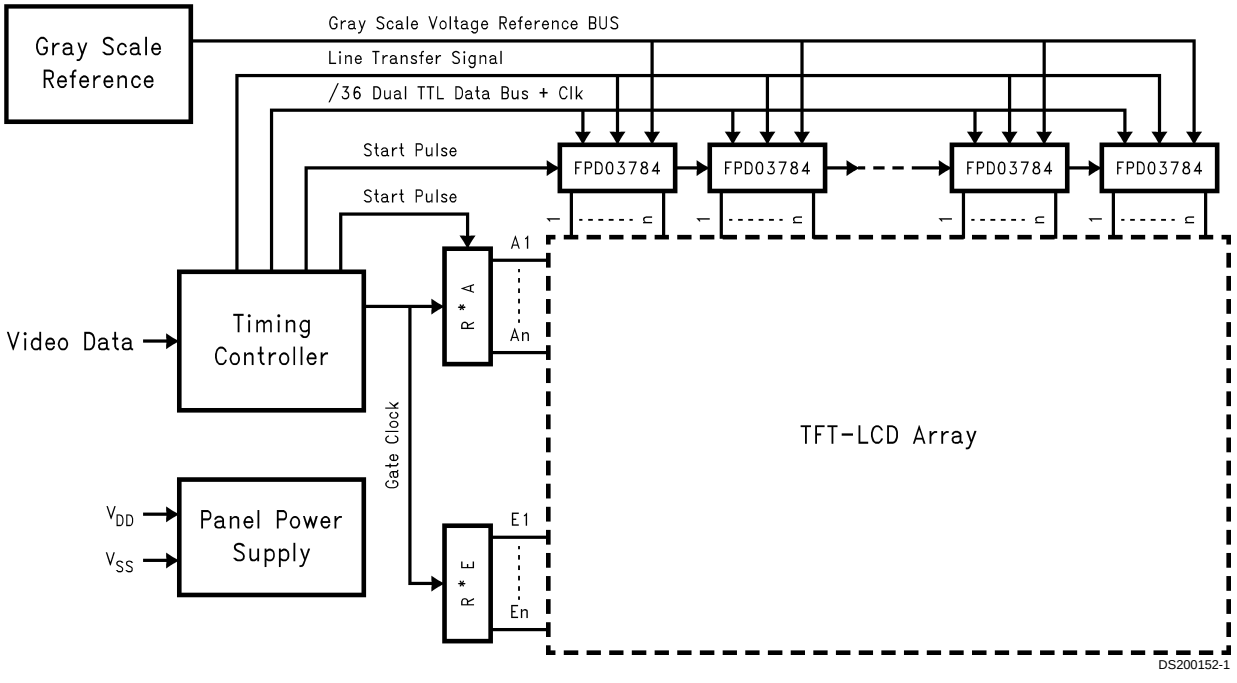
The FPD03784 Column Driver is a direct drive, 64 gray level, 384 output, TFT-LCD column driver with a dual bus, TTL data interface. It provides the capability to display 262,144 colors (18-bit color) with a large dynamic output range for twisted nematic applications. When used in a bank with other FPD03784 column drivers, the FPD03784 can support both XGA (8 drivers) or SXGA (10 drivers) applications. Output voltages are gamma corrected programmably to provide a direct mapping between digital video and LCD panel brightness.

The FPD03784 offers a low power, low EMI column driver solution with programmable output drive current and direct-drive dynamic range, and dot-inversion addressing.

Features

- Up to 65 MHz clock
- Supports both XGA and SXGA timing
- Supports notebook and monitor applications
- Charge Conservation for low power consumption
- 64 Gray levels per color (18-bit color)
- Externally programmable 2.2 gamma characteristic
- Supports both Dot and N-Line inversion
- Externally programmable gamma characteristic
- Programmable drivability allows optimization for small or large panel applications
- Very low offsets for artifact-free images
- High voltage outputs for high contrast in a large range of display panel applications

System Diagram



Absolute Maximum Ratings (Note 1)

Analog Supply, (V_{DD2}) (Note 2)	−0.3V to +10.5V
Logic Supply, (V_{DD1}) (Note 2)	−0.3V to +5.0V
High Bias Supply, (V_{HBIAS}) (Note 2)	−0.3V to +12.0V
Low-Polarity RDAC Reference Voltages, (V_{GMA7} to V_{GMA12}) (Note 2)	−0.3V to 0.5V_{DD2}
High-Polarity RDAC Reference Voltages, (V_{GMA1} to V_{GMA6}) (Note 2)	0.5V_{DD2} − 1.0V to V_{DD2} + 0.3V
RDAC Current (All Gamma Voltage Taps), (I_{GMA} to I_{GMA12})	−2.5mA to 2.5mA
Input Voltage (Digital Logic), (V_{IN}) (Note 2)	−0.3V to V_{DD1} + 0.3V
Output Voltage, (V_{OUT}) (Note 2)	−0.3V to V_{DD2} + 0.3V
Output Current (Analog), (I_{OUT})	−7mA to +7mA
Input Current Source, (I_{SIN})	−200µA to +200µA
Output Current Source, (I_{SOUT})	−200µA to +200µA
IREF Current, (I_{REF})	−1mA to +0.2mA
Storage Temperature Range, (T_S)	−55˚C to +125˚C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Absolute voltages referenced to V_{SS1} = V_{SS2} = 0.0V.

Recommended Operating Conditions

	Min	Typ	Max	Units
Logic Supply Voltage (V_{DD1}) (3.3V OR 2.5V)	3.0 2.25	3.3 2.5	3.6 2.75	V V
Supply Voltage (V_{DD2})	7.5		9.5	V
Operating Temperature (T_A)	−10	+25	+70	˚C

DC Electrical Characteristics

Digital Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		0.7 V_{DD1}			V
V_{IL}	Input Low Voltage				0.3 V_{DD1}	V
V_{OH}	Output High Voltage	I_{OH} = −0.5mA	V_{DD1} − 0.5			V
V_{OL}	Output Low Voltage	I_{OL} = 0.5mA			0.5	V
I_{DD1}	Logic Current	(Note 3)		0.6		mA
I_{DD1}	Logic Current	(Note 4)		0.36		mA
I_{IH}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 3.6V			1	µA
I_{IL}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 0V			1	µA
C_{IN}	Input Capacitance			2		pF

Note 3: CLK frequency = 32.5 MHz, V_{DD1} = 3.3V, V_{SS1} = V_{SS2} = 0.0V, R_{IREF} = 220 kΩ, charge share time = 1.5µs, line time = 22µs.

Note 4: CLK frequency = 32.5 MHz, V_{DD1} = 2.5V, V_{SS1} = V_{SS2} = 0.0V, R_{IREF} = 220 kΩ, charge share time = 1.5µs, line time = 22µs.

Analog Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD2}	Supply Current Consumption	(Note 5)		4.0		mA
PD	Power Dissipation	(Note 5)		40		mW
V_{GMA1}	Upper RDAC High Side Input	(Note 6)	V_{DD2}/2 + 0.2		V_{DD2} − 0.2	V
V_{GMA6}	Upper RDAC Low Side Input	(Note 6)	V_{DD2}/2 + 0.2		V_{DD2} − 0.2	V
V_{GMA7}	Lower RDAC High Side Input	VDD2 ≥ 8.5V(Note 6)	0.2		V_{DD2}/2 − 0.2	V
		VDD2 < 8.5V	0.2		V_{DD2}/2 − 0.4	V
V_{GMA12}	Lower RDAC Low Side Input	(Note 6)	0.2		V_{DD2}/2 − 0.2	V
V_{HBIAS}	Voltage of High Bias Current Supply:	V_{HBIAS} = V_{DD2}	V_{DD2}		V_{DD2}	
		Separate V_{HBIAS} Supply	≥ V_{GMA1} + 1.5V and ≥ 8.5V		V_{DD2} + 2.0	V
V_{CS}	Charge Share Voltage		The Greater of V_{DD1} or V_{GMA7}		V_{GMA6}	V
C_{LOAD}	Output Capacitive Load		30		80	pF
V_{OUT}	Output Voltage Range		V_{SS2} + 0.2		V_{DD2} − 0.2	V
A_{IREF}	I_{REF} to I_{MAX} Gain Factor	(Note 7)	8	10	12	

Analog Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_{IHBIAS}	I_{SIN} to I_{HBIAS} Gain Factor			22.5		
R_{CSTIME}	CSTIME resistance		5	12		kΩ
C_{CSTIME}	CSTIME capacitance			100	150	pF
I_{SIN}	Input Current Source		16	40	100	µA
I_{REF}	Amplifier Reference Current		10		75	µA
R_{DAC}	RDAC References (V_{GMA1} to V_{GMA6} and V_{GMA7} to V_{GMA12})	each	12.0	15.0	18.0	kΩ
V_{pperr}	Output Peak to Peak Error (gray levels 0 through 58)	$V_{GMA1} = V_{DD2} - 0.2V$ $V_{GMA12} = V_{SS2} + 0.2V$ (Note 8)		±3	±12	mV
	Output Peak to Peak Error (gray levels 59 through 63)			±5	±25	mV

Note 5: V_{DD2} = 9.5V, V_{HBIAS} = 9.5V, R_{IREF} = 220 kΩ, R_{ISIN} = 470 kΩ, V_{DD1} = 3.3V, DCLK = 65 MHz, R_{LOAD} = 5 kΩ, C_{LOAD} = 50 pF, charge share time = 1.5 µs, all other swinging between V_{GMA1} (= 8.0V) and V_{GMA12} (= 0.5V) with a line time = 22 µs.

Note 6: The following relationship must be maintained between the reference voltages: $V_{DD2} > V_{GMA1} > V_{GMA2} > V_{GMA3} > V_{GMA4} > V_{GMA5} > V_{GMA6} > V_{GMA7} > V_{GMA8} > V_{GMA9} > V_{GMA10} > V_{GMA11} > V_{GMA12} > V_{SS2}$

Note 7: I_{MAX} is the current delivered into a potential of 0.2V when the output is commanded to a potential of V_{DD2} − 0.2V or the current into the output from a potential of V_{DD2} − 0.2V when the output is commanded to 0.2V (V_{SS2} = 0V).

Note 8: This parameter reflects the error in peak-to-peak output voltage for each gray-level when the output swings from the gray-level high value, VHxx, to its low value, VLxx. This parameter applies to every output on the die. The **Typical** value represents one standard deviation from ideal based on tester data. The **Maximum** value is a constraint of the test environment, not the performance of the part.

Note 9: Current into device pins is defined as positive. Current out of device pins is defined as negative.

AC Electrical Characteristics

Digital AC Characteristics (3.3V Logic)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLK	Data Clock Frequency	SINGLE = 1 (Note 10)			65.0	MHz
		SINGLE = 0 (Note 10)			27.5	MHz
t_{WDCP}	CLK Clock Pulse Width	SINGLE = 1 (Note 10)	5			ns
		SINGLE = 0 (Note 10)	10			ns
t_{DSU}	Data Setup DX[5:0], POL, INVTxxx		4			ns
t_{DHLD}	Data Hold DX[5:0], POL, INVTxxx		4			ns
t_{TWP}	$\overline{LOAD}$ Pulse Width		50			ns
t_{LDENSU}	$\overline{LOAD}$ to First ENIO Setup	(Note 11)	200			ns
t_{ENDCSU}	ENIOx Input to CLK Setup		2.5			ns
t_{WEN}	ENIOx Input Pulse Width		10			ns
t_{ENPR}	ENIOx Output Prop Delay	Load = 20pF			12	ns
t_{LDLY}	Delay to $\overline{LOAD}$ Pulse		3			CLKs

Digital AC Characteristics (2.5V Logic)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLK	Data Clock Frequency	SINGLE = 1 (Note 10)			40.0	MHz
		SINGLE = 0 (Note 10)			17.5	MHz
t_{WDCP}	CLK Clock Pulse Width	SINGLE = 1 (Note 10)	10			ns
		SINGLE = 0(Note 10)	25			ns
t_{DSU}	Data Setup DX[5:0], POL, INVTxxx		4			ns
t_{DHLD}	Data Hold DX[5:0], POL, INVTxxx		6			ns
t_{TWP}	$\overline{LOAD}$ Pulse Width		50			ns
t_{LDENSU}	$\overline{LOAD}$ to First ENIO Setup	(Note 11)	200			ns
t_{ENDCSU}	ENIOx Input to CLK Setup		4			ns

Digital AC Characteristics (2.5V Logic) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WEN}	ENIOx Input Pulse Width		12			ns
t_{ENPR}	ENIOx Output Prop Delay	Load = 20pF			19	ns
t_{LDLY}	Delay to $\overline{LOAD}$ Pulse		3			CLKs

Note 10: Rise/Fall = 2.0ns max (10% to 90%)

Note 11: Does not need to be synchronous to clock.

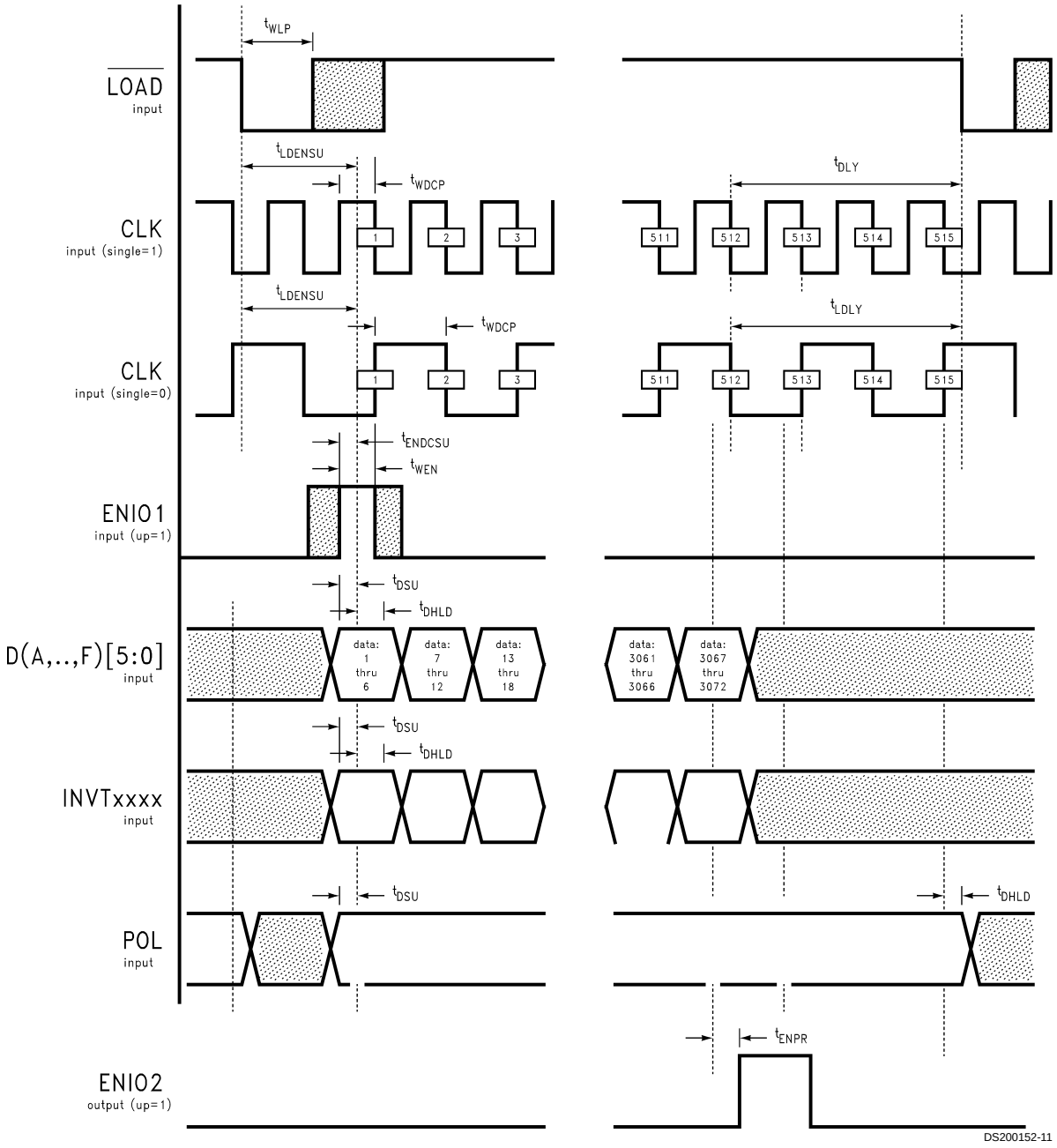
Analog AC Characteristics

Supplies: $V_{SS1} = V_{SS2} = 0.0V$, $V_{DD1} = 3.3V$, $V_{DD2} = +9.5V$, $V_{HBIAS} = 11.0V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{settle\ 90\%}$	Output Settling Time to 90% of Final Value	$R_{LOAD} = 5k\Omega$, $C_{LOAD} = 40$ pF (Note 12)		2.4		µs
$t_{settle\ 99\%}$	Output Settling Time to 99% of Final Value	$R_{LOAD} = 5k\Omega$, $C_{LOAD} = 40$ pF (Note 12)		2.8		µs

Note 12: $I_{SIN} = 40\mu A$, $I_{REF} = 45\mu A$, Charge Share Time = 400ns, $V_{GMA1} = 9.3V$, $V_{GMA10} = 0.2V$, $V_{GMA5} = 5.2V$, $V_{GMA6} = 4.8V$.

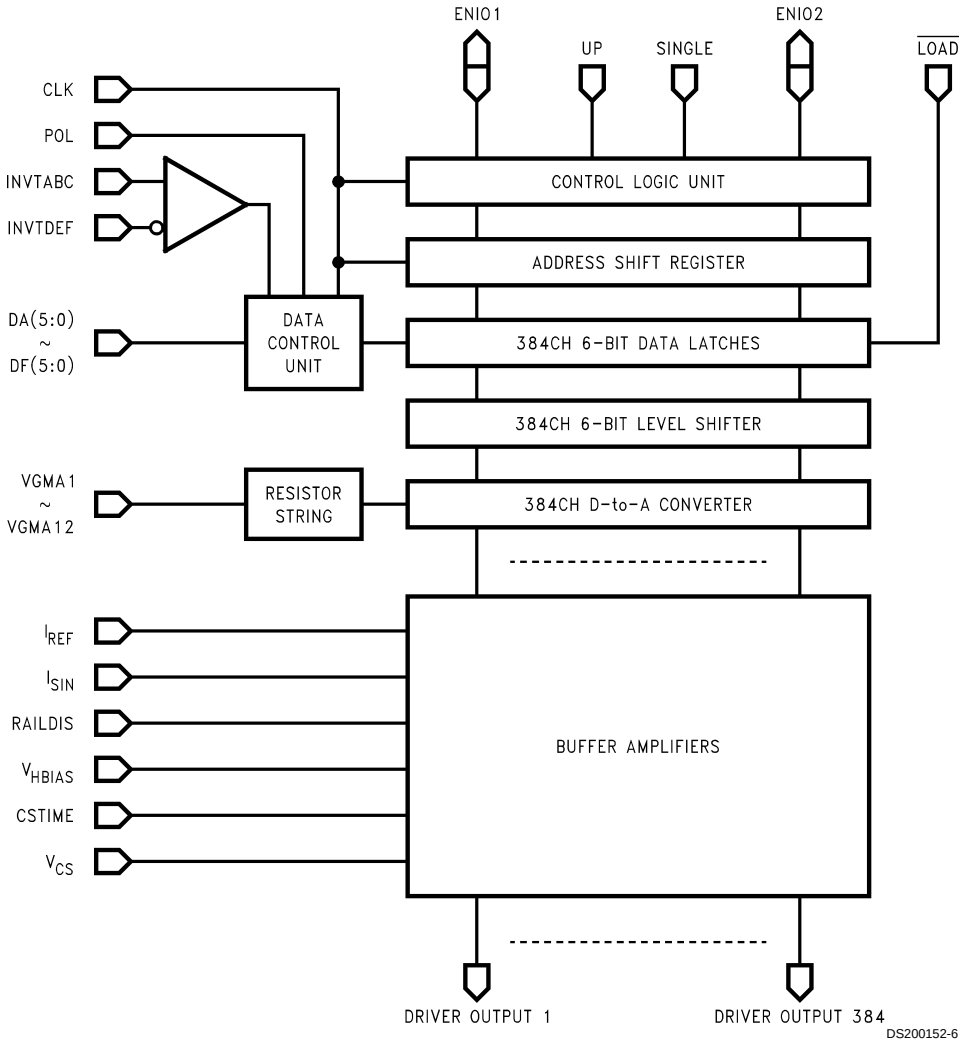
Timing Diagrams



Note 13: $\overline{\text{LOAD}}$ pulse is asynchronous to CLK. It must meet minimum pulse-width, t_{LDENSU} and t_{LDLY}.

Note 14: A minimum of 3 CLK cycles are required from the falling edge of CLK (on last data input to last chip) to the falling edge of the $\overline{\text{LOAD}}$ pulse. After these 3 CLK cycles, CLK may be disabled.

Block Diagram



DS200152-6

Functional Description

GENERAL OVERVIEW

The FPD03784 is a low power, low EMI, 384 output column driver with 64 gray level capability (6-bit). It provides direct drive for TFT-LCD displays, eliminating the need for V_{com} modulation. Direct drive significantly reduces system power consumption and also reduces component count while providing superior image quality and cross-talk margin. The FPD03784 utilizes National's *Charge Conservation Technology* that recovers energy stored in the capacitance of the column lines to reduce power consumption further.

The FPD03784 is designed for use in systems using dot inversion as the method of polarity inversion. Column inversion and N-line inversion are also supported. Other modes of polarity inversion including line inversion and frame inversion are not supported.

Digital video data inputs to the FPD03784 are received on six, six bit wide busses (dual bank, RGB busses) using TTL signaling. The digital video commands one of 64 gray level voltages on each output. Output voltages are driven with individual high drive, low offset, programmable-slew-rate, operational amplifiers. Data loading and line buffering is accomplished by means of an internal, bi-directional shift register.

GAMMA CORRECTION

The FPD03784 is designed to offer compatibility with a wide range of panel gamma characteristics. The output voltage levels corresponding to each of the 64 gray level commands can be externally adjusted to match the desired gamma characteristics of the display by means of two internal resistor-string DACs (RDACs). One RDAC provides the high-polarity output voltages (voltages higher than V_{com}) and the other provides the low-polarity output voltages (voltages lower than V_{com}).

The default RDAC resistance values have been carefully designed to provide a smooth 2.2 gamma characteristic in a twisted nematic (TN) display. This is especially useful for monitor applications. Consequently, most application designs will only need to provide references for each of the two ends of the two RDACs (four gamma references). Additional, intermediate taps to the RDAC are also provided for optional customization of the display gamma for contrast control as an example.

CHARGE CONSERVATION TECHNOLOGY

National Semiconductor's proprietary charge conservation technology significantly reduces power consumption. Charge conservation works by briefly switching all of the columns at the start of each line to a common node. This has

Functional Description (Continued)

the effect of redistributing the charge stored in the capacitance of the panel columns. Since half the columns are at voltages more positive than V_{com} and half are more negative, this redistribution of charge or "charge-sharing" has the effect of pulling all of the columns to a neutral voltage near the middle of the driver's dynamic range. Thus, the voltages on all the columns are driven approximately halfway toward their next value with no power expended. This dramatically reduces panel power dissipation (up to a theoretical limit of 50%) compared to conventional drivers which must drive each column through the entire voltage swing every time polarity is reversed.

PIN DESCRIPTIONS

The pin order configuration for the FPD03784 is shown in fig. 3. Optional pins do not need to be carried off a custom TCP or COP package but may require a connection to a neighboring pad on the die by a tie on the tape. The following paragraphs describe the function of the FPD03784 pins.

CSTIME — *CHARGE SHARE TIME (INPUT)*

The input controls how long the outputs are in charge share mode following each $\overline{LOAD}$ signal. The CSTIME input from all of the column drivers should be tied together and connected to VSS1 through a parallel combination of RC. The charge time is determined by the equation:

$$T_{charge\ share} = 0.69\ RC$$

A typical capacitance of 100pF should be chosen to swamp parasitic board and I/O pin effects. See *Figure 1*.

CLK — *DATA CLOCK (INPUT)*

Clock input for data on Dx[0:5].

DX[5:0] — *DATA BUS (INPUT)*

DA[5:0] — Data Input Pins for OUTPUTS 1, 7...379

DB[5:0] — Data Input Pins for OUTPUTS 2, 8...380

DC[5:0] — Data Input Pins for OUTPUTS 3, 9...381

DD[5:0] — Data Input Pins for OUTPUTS 4, 10...382

DE[5:0] — Data Input Pins for OUTPUTS 5, 11...383

DF[5:0] — Data Input Pins for OUTPUTS 6, 12...384

ENIO1/ENIO2 — *DATA LOADING ENABLE 1 AND 2 (I/O)*

If UP = H, then the ENIO1 pin is configured as an input and the ENIO2 pin is configured as an output. If UP = L, then the ENIO2 pin is configured as an input and the ENIO1 pin is configured as an output.

INVTABC — *DIGITAL DATA INVERT (INPUT)*

When INVERT = L, input data from DA[0:5], DB[0:5] and DC[0:5] is inverted. The INVTABC pin can be tied to INVTDEF on the TCP to form a single INVERT pin, or operated independently from each other.

INVTDEF — *DIGITAL DATA INVERT (INPUT)*

When INVERT = H, input data from DD[0:5], DE[0:5] and DF[0:5] is inverted. The INVTABC pin can be tied to INVTDEF on the TCP to form a single INVERT pin, or operated independently from each other.

I_{REF} — ***REF****ERENCE CURRENT FOR OUTPUT DRIVE (INPUT)*

The I_{REF} input allows the designer to set the maximum output drive current (I_{MAX}) of the FPD03784 suitable for the column line, RC network load. Current flow out of the I_{REF} pin is used to set the rise and fall slew rate of the output waveform. This current is supplied through an external resistor (R_{IREF}) tied between the I_{REF} pin (held by the FPD03784 at V_{DD1}) and V_{SS1}. Each driver IC must have a separate R_{IREF} resistor (see *Figure 1*).

I_{SIN} — *CURRENT SOURCE INPUT (INPUT)*

The I_{SIN} current controls the bandwidth and settling performance of the FPD03784 output-stage amplifiers. Increasing I_{SIN} increases the amplifier bandwidth and reduces settling time but also increases power consumption. Normally, I_{SIN} is set to 40µA, which provides a good balance between power consumption and amplifier bandwidth. The flexibility to adjust I_{SIN} accommodates very fast rise times ($I_{SIN} > 40\mu A$) or applications where low power is of extreme interest ($I_{SIN} < 40\mu A$).

The I_{SIN} current is supplied through an external resistor (R_{ISIN}) connected between the I_{SIN} pin and V_{DD2}. R_{ISIN} can be computed as follows:

$$R_{ISIN} = \frac{V_{DD2} - 2}{I_{SIN}}$$

(I_{SIN} normally = 40µA)

One resistor (R_{ISIN}) is needed for the entire display. This resistor is connected to the I_{SIN} input of the first driver, and the current going into this pin is copied to the I_{SOUT} output pin for cascading to the next driver. See *Figure 1*. Note that I_{HBIAS} varies linearly with I_{SIN}.

I_{SOUT} — *CURRENT **S**OURCE **O**UTPUT (OUTPUT)*

This output pin supplies the I_{SIN} current to the I_{SIN} input pin of the next driver in the row (see *Figure 1*). The I_{SOUT} pin of the last driver should be left floating. Optionally, this pin can be left floating on each driver if the designer wishes to provide a separate I_{SIN} source to each driver. While this adds resistor component count, it reduces input lead count.

$\overline{LOAD}$ — *DATA **LOAD** (INPUT)*

The falling edge of $\overline{LOAD}$ copies the digital video buffered by the shift register into a second latch beginning the D to A conversion. Immediately following the fall of $\overline{LOAD}$, the outputs are forced into charge share mode for the time set by the CSTIME input. The outputs then drive the D to A converted voltages following the CSTIME.

POL — ***POL****ARITY (INPUT)*

When POL = L, odd numbered outputs (1, 3, 5, ...383) are controlled by VGMA7 through VGMA12 and even numbered outputs are controlled by VGMA1 through VGMA6. When POL = H, odd numbered outputs are controlled by VGMA1 through VGMA6 and even numbered outputs are controlled by VGMA7 through VGMA12.

SINGLE — ***SINGLE****/DUAL-EDGE CLOCK ENABLE (INPUT)*

This pin controls single/dual-edge clocking. When SINGLE is high, single-edge clocking is enabled, and input data is latched only on the falling edge of CLK. When SINGLE is low, dual-edge clocking is enabled, and input data is latched on both the rising and falling edges of CLK.

Optional — The SINGLE die pad is bounded on each side by a logic High and a logic Low pad. This allows the state of SINGLE to be chosen on the TCP to eliminate an input pin.

UP — *DATA SHIFT DIRECTION — **UP** OR DOWN (INPUT)*

The UP pin controls the data shift direction. If UP is high then data is shifted "up" from output 1 to output 384, ENIO1 is configured as an input, and ENIO2 is an output. If UP is low then data is shifted "down" from output 384 to output 1, ENIO2 is an input, and ENIO1 is an output.

Functional Description (Continued)

Optional — The UP die pad is bounded on each side by a logic High and a logic Low pad. This allows the state of UP to be chosen on the TCP to eliminate an input pin.

V_{CS} — ***C**HARGE **S**HARE **V**OLTAGE REFERENCE*

This input provides the reference for the common node voltage during charge share time.

V_{DD1} — *DIGITAL **V**OLTAGE SUPPLY*

Positive supply voltage for the digital logic functions of the driver.

V_{DD2} — *ANALOG **V**OLTAGE SUPPLY*

Positive supply voltage for the analog functions of the driver.

V_{GMA1}–V_{GMA12} — *RDAC REFERENCES (INPUTS)*

The reference voltages to the upper and lower RDACs used to control the inverse gamma transfer function of the driver.

Option – Any or all of the inputs V_{GMA2} through V_{GMA5} and V_{GMA8} through V_{GMA11} can be left undriven (floating) at the designer's option to eliminate input pins and/or external reference circuitry.

V_{HBIAS} — ***H**IGH **BIAS** CURRENT **V**OLTAGE SUPPLY*

Optional positive supply voltage that provides a constant bias current to the output amplifiers to extend dynamic range. When separately provided, V_{HBIAS} must be 1.5V greater than V_{GMA1} (see Table iii for limits). When not separately provided, V_{HBIAS} must be supplied by V_{DD2}. In this configuration, V_{GMA1} must be held at or below V_{DD2} − 1.5V (see table iii for limits).

V_{SS1} — ***DIGITAL G**ROU**ND***

Digital ground reference voltage.

V_{SS2} — *ANALOG GROU**ND***

Analog ground reference voltage.

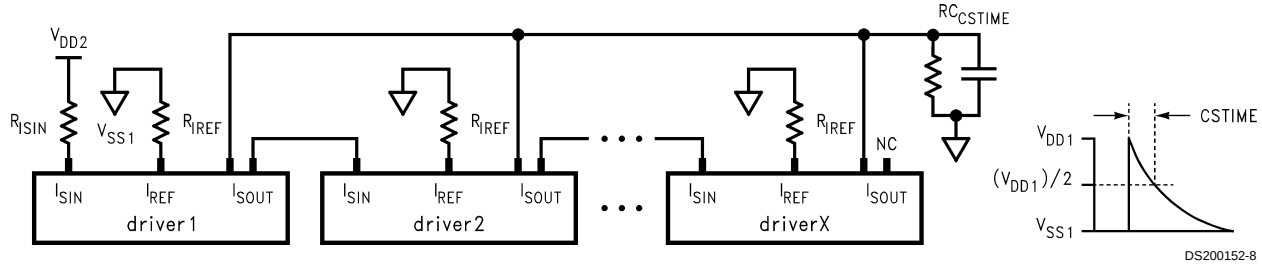
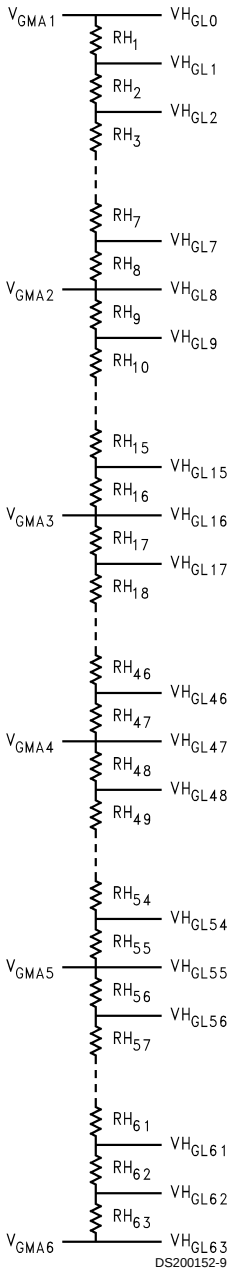


FIGURE 1. External Components and Connections for the I_{REF}, I_{SIN} and I_{SOUT}Pins

Functional Description (Continued)

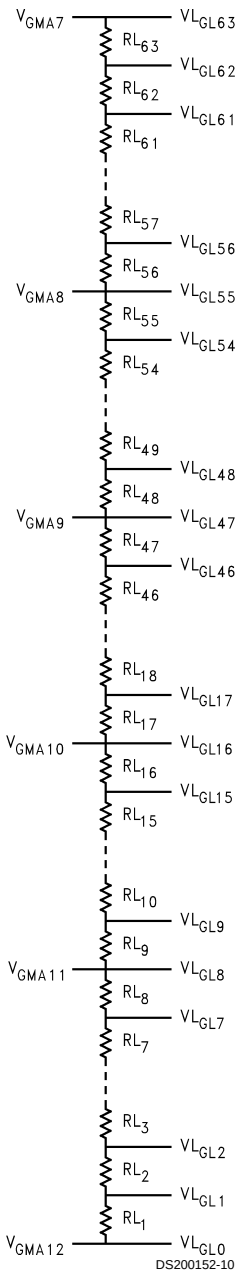


RH1	RDAC x 46/1008
RH2	RDAC x 40/1008
RH3	RDAC x 39/1008
RH4	RDAC x 38/1008
RH5	RDAC x 37/1008
RH6	RDAC x 32/1008
RH7	RDAC x 30/1008
RH8	RDAC x 29/1008
RH9	RDAC x 29/1008
RH10	RDAC x 26/1008
RH11	RDAC x 21/1008
RH12	RDAC x 19/1008
RH13	RDAC x 17/1008
RH14	RDAC x 17/1008
RH15	RDAC x 15/1008
RH16	RDAC x 14/1008
RH17	RDAC x 13/1008
RH18	RDAC x 13/1008
RH19	RDAC x 11/1008
RH20	RDAC x 10/1008
RH21	RDAC x 10/1008
RH22	RDAC x 9/1008
RH23	RDAC x 9/1008
RH24	RDAC x 9/1008
RH25	RDAC x 9/1008
RH26	RDAC x 8/1008
RH27	RDAC x 8/1008
RH28	RDAC x 7/1008
RH29	RDAC x 7/1008
RH30	RDAC x 7/1008
RH31	RDAC x 7/1008

RH32	RDAC x 7/1008
RH33	RDAC x 7/1008
RH34	RDAC x 7/1008
RH35	RDAC x 6/1008
RH36	RDAC x 6/1008
RH37	RDAC x 6/1008
RH38	RDAC x 7/1008
RH39	RDAC x 7/1008
RH40	RDAC x 6/1008
RH41	RDAC x 7/1008
RH42	RDAC x 6/1008
RH43	RDAC x 7/1008
RH44	RDAC x 6/1008
RH45	RDAC x 7/1008
RH46	RDAC x 8/1008
RH47	RDAC x 7/1008
RH48	RDAC x 7/1008
RH49	RDAC x 7/1008
RH50	RDAC x 8/1008
RH51	RDAC x 8/1008
RH52	RDAC x 8/1008
RH53	RDAC x 9/1008
RH54	RDAC x 9/1008
RH55	RDAC x 8/1008
RH56	RDAC x 10/1008
RH57	RDAC x 12/1008
RH58	RDAC x 13/1008
RH59	RDAC x 14/1008
RH60	RDAC x 15/1008
RH61	RDAC x 23/1008
RH62	RDAC x 36/1008
RH63	RDAC x 128/1008

FIGURE 2. FPD03784 R-DAC Transfer Characteristic

Functional Description (Continued)

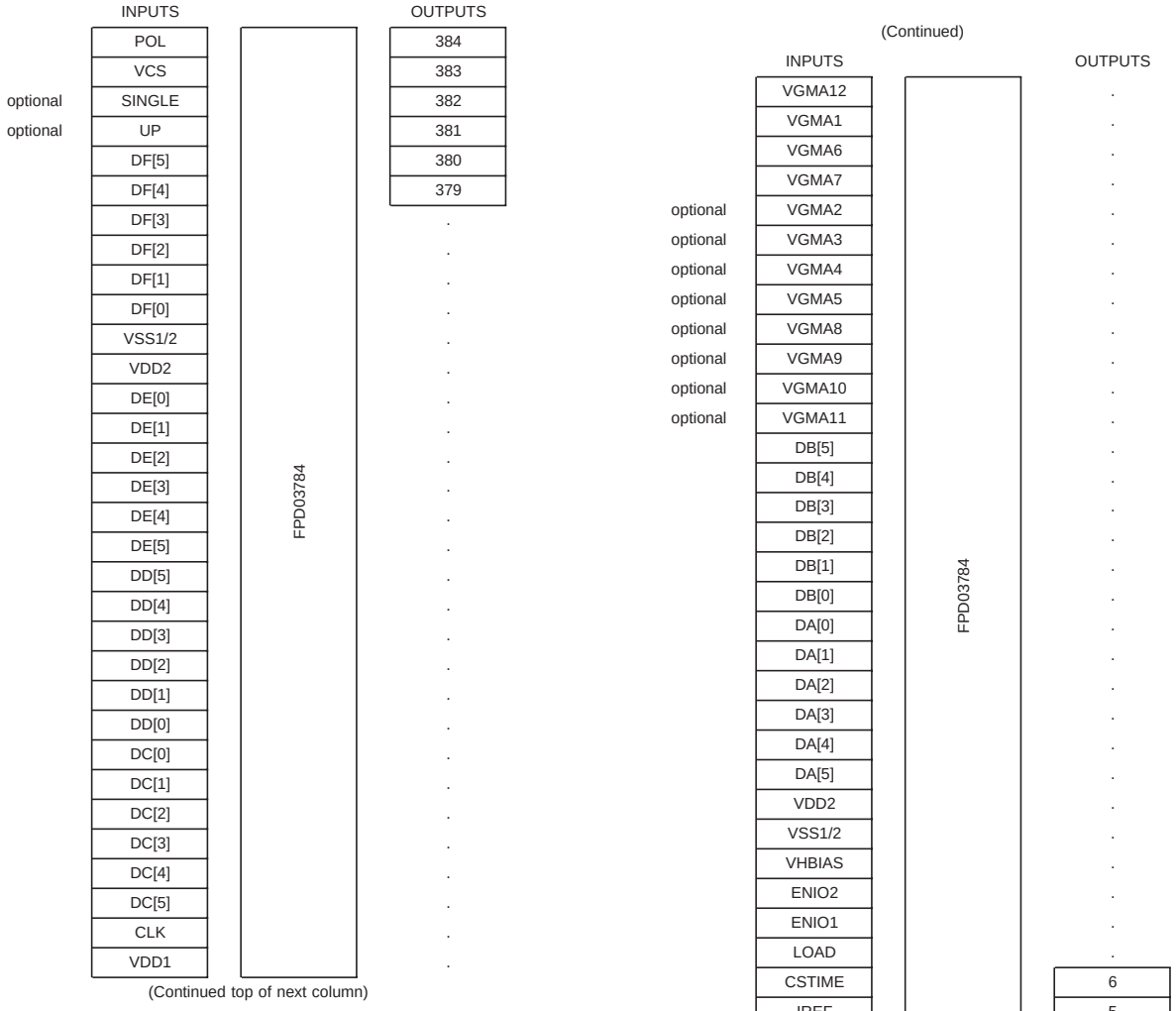


RL1	RDAC x 46/1008
RL2	RDAC x 40/1008
RL3	RDAC x 39/1008
RL4	RDAC x 38/1008
RL5	RDAC x 37/1008
RL6	RDAC x 32/1008
RL7	RDAC x 30/1008
RL8	RDAC x 29/1008
RL9	RDAC x 29/1008
RL10	RDAC x 26/1008
RL11	RDAC x 21/1008
RL12	RDAC x 19/1008
RL13	RDAC x 17/1008
RL14	RDAC x 17/1008
RL15	RDAC x 15/1008
RL16	RDAC x 14/1008
RL17	RDAC x 13/1008
RL18	RDAC x 13/1008
RL19	RDAC x 11/1008
RL20	RDAC x 10/1008
RL21	RDAC x 10/1008
RL22	RDAC x 9/1008
RL23	RDAC x 9/1008
RL24	RDAC x 9/1008
RL25	RDAC x 9/1008
RL26	RDAC x 8/1008
RL27	RDAC x 8/1008
RL28	RDAC x 7/1008
RL29	RDAC x 7/1008
RL30	RDAC x 7/1008
RL31	RDAC x 7/1008

RL32	RDAC x 7/1008
RL33	RDAC x 7/1008
RL34	RDAC x 7/1008
RL35	RDAC x 6/1008
RL36	RDAC x 6/1008
RL37	RDAC x 6/1008
RL38	RDAC x 7/1008
RL39	RDAC x 7/1008
RL40	RDAC x 6/1008
RL41	RDAC x 7/1008
RL42	RDAC x 6/1008
RL43	RDAC x 7/1008
RL44	RDAC x 6/1008
RL45	RDAC x 7/1008
RL46	RDAC x 8/1008
RL47	RDAC x 7/1008
RL48	RDAC x 7/1008
RL49	RDAC x 7/1008
RL50	RDAC x 8/1008
RL51	RDAC x 8/1008
RL52	RDAC x 8/1008
RL53	RDAC x 9/1008
RL54	RDAC x 9/1008
RL55	RDAC x 8/1008
RL56	RDAC x 10/1008
RL57	RDAC x 12/1008
RL58	RDAC x 13/1008
RL59	RDAC x 14/1008
RL60	RDAC x 15/1008
RL61	RDAC x 23/1008
RL62	RDAC x 36/1008
RL63	RDAC x 128/1008

FIGURE 3. FPD03784 R-DAC Transfer Characteristic (continued)

FPD03784 I/O Configuration



Note: This figure represents an FPD03784 die oriented pad side up.

Packaging

The FPD03784 is available as singulated die.

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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