September 2005

National Semiconductor

DS90LV804
4-Channel 800 Mbps LVDS Buffer/Repeater

General Description

The DS90LV804 is a four channel 800 Mbps LVDS buffer/repeater. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV804, available in the LLP (Leadless Leadframe Package) package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

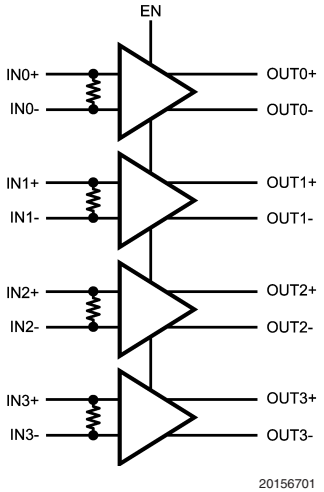
An output enable pin is provided, which allows the user to place the LVDS outputs and internal biasing generators in TRI-STATE.

The differential inputs interface to LVDS, and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals over lossy cables and backplanes, or in stub hider applications.

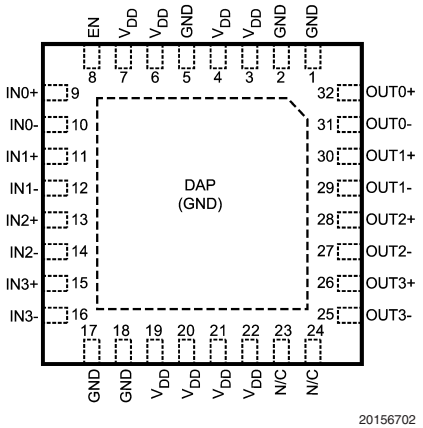
Features

- 800 Mbps data rate per channel
- Low output skew and jitter
- Hot plug protection
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100Ω input termination
- 15 kV ESD protection
- Single 3.3V supply
- Very low power consumption
- Industrial -40 to +85˚C temperature range
- Small LLP Package Footprint

Block and Connection Diagrams



DS90LV804 Block Diagram



DS90LV804 LLP Pinout
(Top View)

Pin Descriptions

Pin Name	LLP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS			
IN0+ IN0–	9 10	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1–	11 12	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2–	13 14	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3–	15 16	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS			
OUT0+ OUT0–	32 31	O, LVDS	Channel 0 inverting and non-inverting differential outputs. (Note 2)
OUT1+ OUT1–	30 29	O, LVDS	Channel 1 inverting and non-inverting differential outputs. (Note 2)
OUT2+ OUT2–	28 27	O, LVDS	Channel 2 inverting and non-inverting differential outputs. (Note 2)
OUT3+ OUT3-	26 25	O, LVDS	Channel 3 inverting and non-inverting differential outputs. (Note 2)
DIGITAL CONTROL INTERFACE			
EN	8	I, LVTTL	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL level input.
POWER			
V_{DD}	3, 4, 6, 7, 19, 20, 21, 22	I, Power	V_{DD} = 3.3V, ±5%
GND	1, 2, 5, 17, 18 (Note 1)	I, Power	Ground reference for LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the LLP-32 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance. The pin numbers listed should also be tied to ground for proper biasing.
N/C	23, 24		No Connect

Note 1: Note that for the LLP package the GND is connected thru the DAP on the back side of the LLP package in addition to grounding actual pins on the package as listed.

Note 2: The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS90LV804 device have been optimized for point-to-point backplane and cable applications.

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage (EN)	−0.3V to (V_{DD}+0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current	+90 mA
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Solder, 4sec)	260˚C
Max Pkg Power Capacity @ 25˚C	4.16W
Thermal Resistance (θ_{JA})	30˚C/W
Package Derating above +25˚C	33.3mW/˚C
ESD Last Passing Voltage	
HBM, 1.5kΩ, 100pF	15 kV
EIAJ, 0Ω, 200pF	250V
Charged Device Model	1000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.15V to 3.45V
Input Voltage (V_I) (Note 4)	0V to V_{DD}
Output Voltage (V_O)	0V to V_{DD}
Operating Temperature (T_A)	
Industrial	−40˚C to +85˚C

Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of products outside of recommended operation conditions.

Note 4: V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
LVTTL DC SPECIFICATIONS (EN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold (Note 6)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V		0	100	mV
V_{TL}	Differential Input Low Threshold (Note 6)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.45V	0.05		3.40	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 3.45V, $V_{DD} = V_{DDMAX}$	−10		+10	µA
		V_{IN} = 0V, $V_{DD} = V_{DDMAX}$	−10		+10	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage (Note 6)	R_L = 100Ω between OUT+ and OUT–	250	500	600	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		–35		35	mV
V_{OS}	Offset Voltage (Note 7)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		–35		35	mV
I_{OS}	Output Short Circuit Current	OUT+ or OUT– Short to GND		–60	–90	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT– to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I_{CC}	Total Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-.		117	140	mA
I_{CCZ}	TRI-STATE Supply Current	EN = 0V		2.7	6	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD}.		210	300	ps
t_{HLT}	Differential High to Low Transition Time			210	300	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output.		2.0	3.2	ns
t_{PHLD}	Differential High to Low Propagation Delay			2.0	3.2	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$		25	80	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.		50	125	ps
t_{JIT}	Jitter (Note 8)	RJ - Alternating 1 and 0 at 400 MHz (Note 9)		1.1	1.5	psrms
		DJ - K28.5 Pattern, 800 Mbps (Note 10)		15	35	psp-p
		TJ - PRBS 2^{23}-1 Pattern, 800 Mbps (Note 11)		30	55	psp-p
t_{ON}	LVDS Output Enable Time	Time from EN to OUT± change from TRI-STATE to active.			300	ns
t_{OFF}	LVDS Output Disable Time	Time from EN to OUT± change from active to TRI-STATE.			12	ns

Note 5: Typical parameters are measured at V_{DD} = 3.3V, T_A = 25˚C. They are for reference purposes, and are not production-tested.

Note 6: Differential output voltage V_{OD} is defined as ABS(OUT+–OUT–). Differential input voltage V_{ID} is defined as ABS(IN+–IN–).

Note 7: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 8: Jitter is not production tested, but guaranteed through characterization on a sample basis.

Note 9: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 400 MHz, t_r = t_f = 50ps (20% to 80%).

Note 10: Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 800 Mbps, t_r = t_f = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

Note 11: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 800 Mbps, t_r = t_f = 50ps (20% to 80%).

Feature Descriptions

OUTPUT CHARACTERISTICS

The output characteristics of the DS90LV804 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

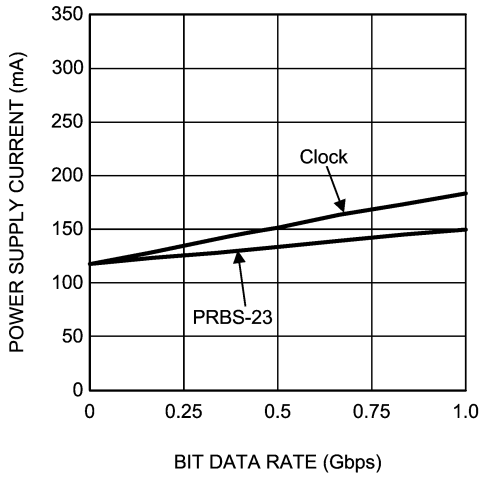
TRI-STATE MODE

The EN input activates a hardware TRI-STATE mode. When the TRI-STATE mode is active (EN=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in TRI-STATE mode. When exiting TRI-STATE mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194 “Failsafe Biasing of LVDS Interfaces” for more information.

TYPICAL PERFORMANCE CHARACTERISTICS



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Dynamic power supply current was measured while running a clock or PRBS 2^{23}-1 pattern with all 4 channels active. V_{CC} = 3.3V, T_A = +25˚C, V_{ID} = 0.5V, V_{CM} = 1.2V

Power Supply Current vs. Bit Data Rate

Packaging Information

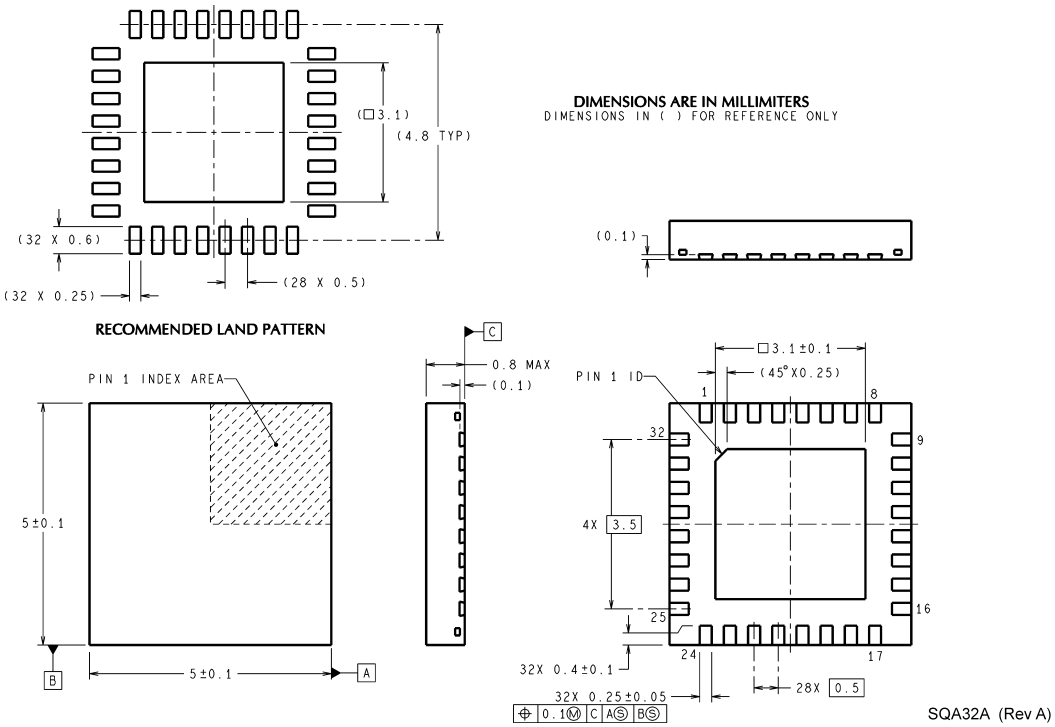
The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP package is offered in the no Pullback configuration. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

For more details about LLP packaging technology, refer to applications note AN-1187, "Leadless Leadframe Package"

Physical Dimensions inches (millimeters) unless otherwise noted



32-LLP, Plastic, Quad
Order Number DS90LV804TSQ (1000 piece Tape and Reel)
DS90LV804TSQX (4500 piece Tape and Reel)
NS Package Number SQA32A

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