National Semiconductor

May 2002

DS90CR218
+3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link Receiver - 75 MHz

General Description

The DS90CR217 (see DS90CR217/218A datasheet) transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR218 receiver converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75 MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/sec).

Complete specifications for the DS90CR217 are located in the DS90CR217/DS90CR218A datasheet. The DS90CR217 supports clock rates from 20 to 85 MHz.

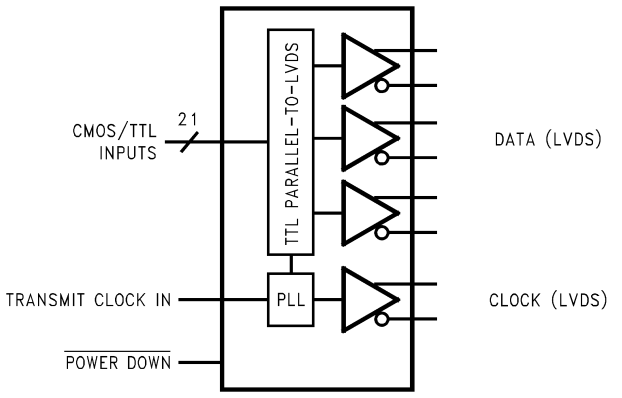
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 75 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on TxINPUTs and RxOUTPUTs
- Low power consumption
- Tx + Rx Powerdown mode <400µW (max)
- ±1V common-mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Mbytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 48-lead TSSOP package

Block Diagrams

DS90CR217



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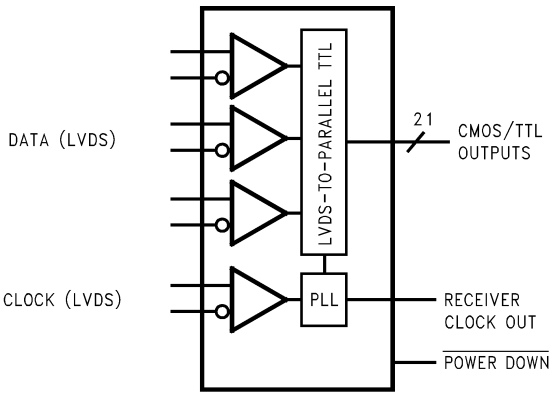
Order Number DS90CR217MTD
See NS Package Number MTD48
(See DS90CR217/DS90CR218A Datasheet)

DS90CR218



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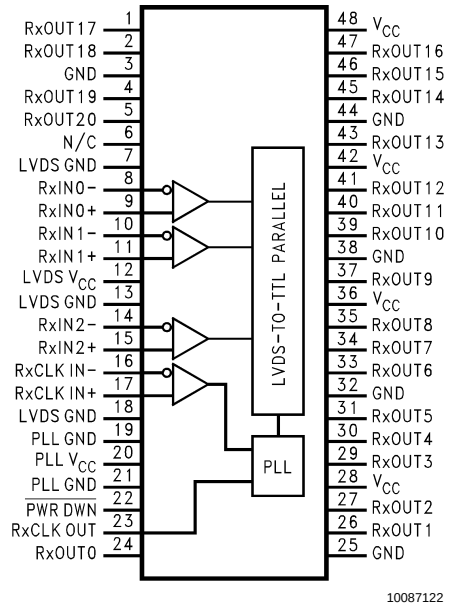
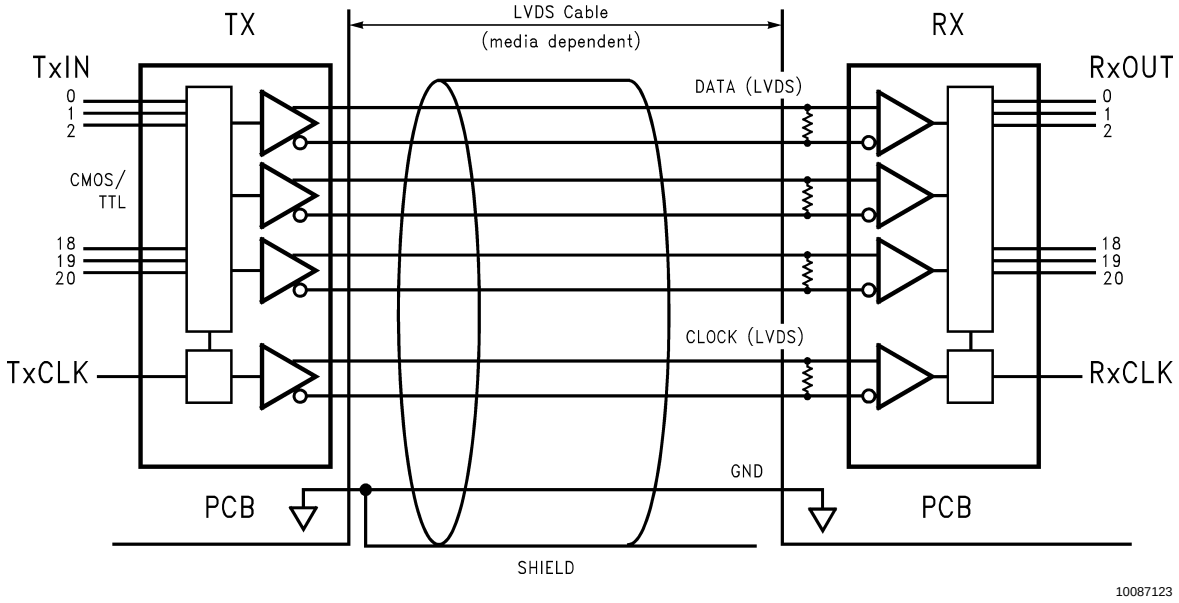
Order Number DS90CR218MTD
See NS Package Number MTD48

Pin Diagram



DS90CR218

Typical Application



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.5V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature	
(Soldering, 4 sec.)	+260˚C
Maximum Package Power Dissipation @ +25˚C	
MTD48 (TSSOP) Package:	
DS90CR218	1.89 W
Package Derating	
DS90CR218	15 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5kΩ, 100pF)	> 7kV
(EIAJ, 0Ω, 200pF)	> 700V
Latch Up Tolerance @ 25˚C	> ±300mA

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−60	−120	mA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern (*Figures 1, 2*)	f = 33 MHz		49	60	mA
			f = 40 MHz		53	65	mA
			f = 66 MHz		78	95	mA
			f = 75 MHz		90	105	mA
I_{CCRZ}	Receiver Supply Current Power Down	$\overline{PWR\ DWN}$ = Low Receiver Outputs Stay Low during Powerdown Mode			15	55	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{TH} and V_{TL}).

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (*Figure 2*)			2.0	3.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (*Figure 2*)			1.8	3.5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (*Figure 8*)	f = 75 MHz	0.58	0.95	1.32	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.49	2.86	3.23	ns
RSPos2	Receiver Input Strobe Position for Bit 2		4.39	4.76	5.13	ns
RSPos3	Receiver Input Strobe Position for Bit 3		6.30	6.67	7.04	ns
RSPos4	Receiver Input Strobe Position for Bit 4		8.20	8.57	8.94	ns
RSPos5	Receiver Input Strobe Position for Bit 5		10.11	10.48	10.85	ns
RSPos6	Receiver Input Strobe Position for Bit 6		12.01	12.38	12.75	ns
RSKM	Receiver Skew Margin (when used with DS90CR217)(Note 4) (*Figure 9*)	f = 75 MHz	380			ps
RCOP	RxCLK OUT Period (*Figure 3*)		13.33	T	50	ns
RCOH	RxCLK OUT High Time (*Figure 3*)	f = 75 MHz	3.6	5	6.0	ns
RCOL	RxCLK OUT Low Time (*Figure 3*)		3.6	5	6.0	ns
RSRC	RxOUT Setup to RxCLK OUT (*Figure 3*)		3.5			ns
RHRC	RxOUT Hold to RxCLK OUT (*Figure 3*)		3.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25˚C, V_{CC} = 3.3V (Note 5)(*Figure 4*)		3.4	5.0	7.3	ns
RPLLS	Receiver Phase Lock Loop Set (*Figure 5*)				10	ms
RPDD	Receiver Powerdown Delay (*Figure 7*)				1	µs

Note 4: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock jitter less than 250 ps.

Note 5: Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 217/287 transmitter and 218/288 receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period. See also DS90CR217 datasheet.

AC Timing Diagrams

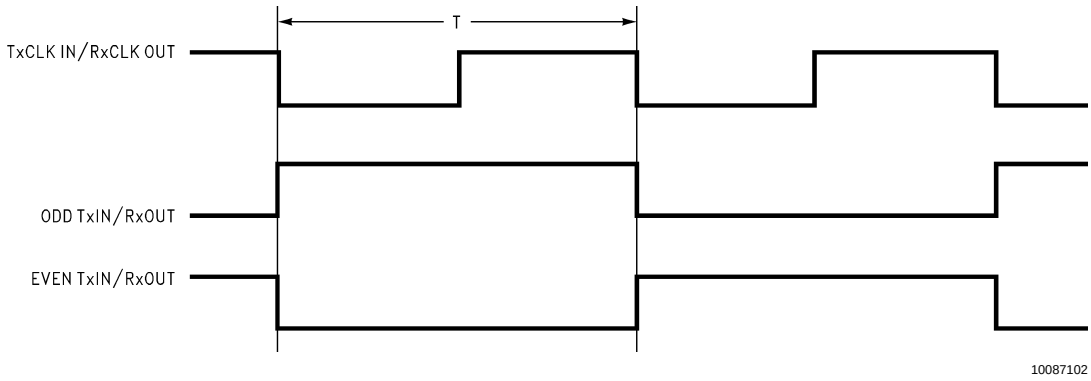


FIGURE 1. “Worst Case” Test Pattern

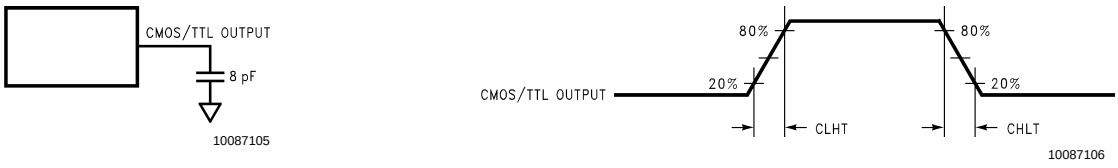


FIGURE 2. DS90CR218 (Receiver) CMOS/TTL Output Load and Transition Times

AC Timing Diagrams (Continued)

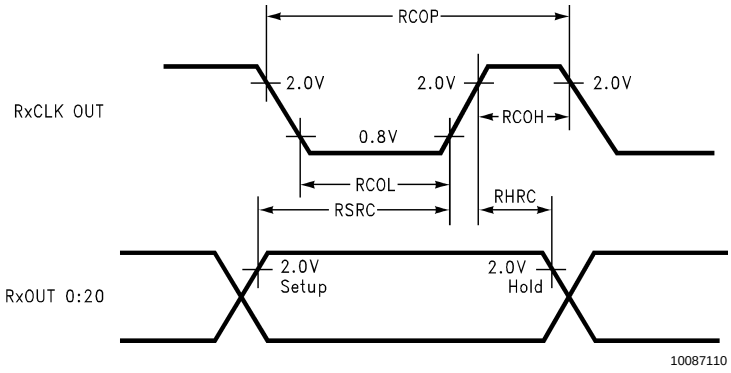


FIGURE 3. DS90CR218 (Receiver) Setup/Hold and High/Low Times

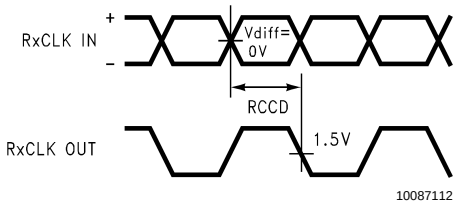


FIGURE 4. DS90CR218 (Receiver) Clock In to Clock Out Delay

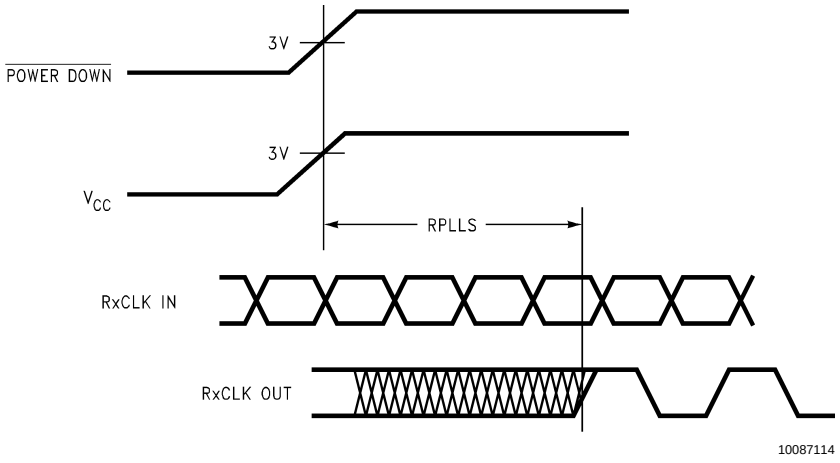


FIGURE 5. DS9OCR218 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

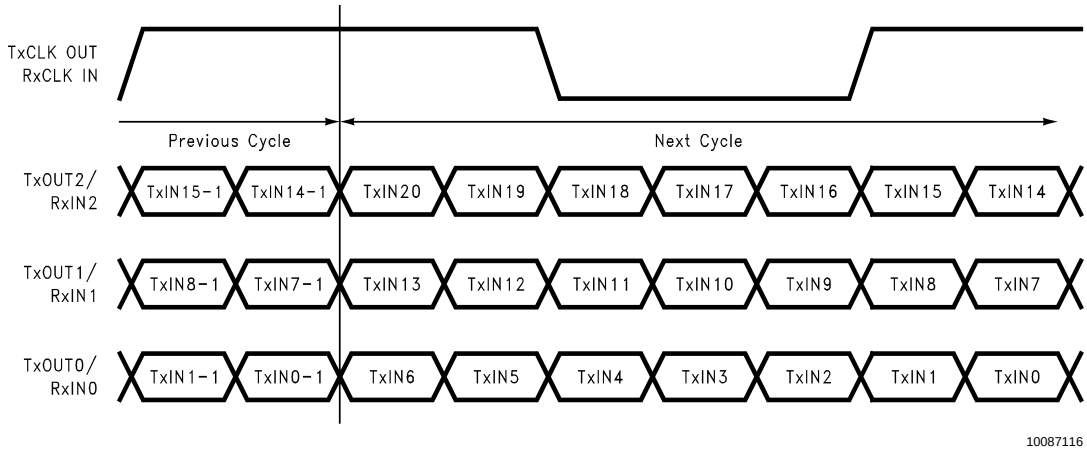


FIGURE 6. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR217)

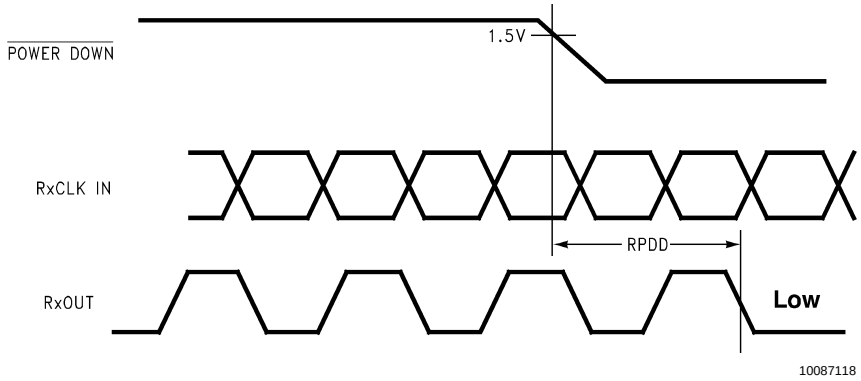


FIGURE 7. Receiver Powerdown Delay

AC Timing Diagrams (Continued)

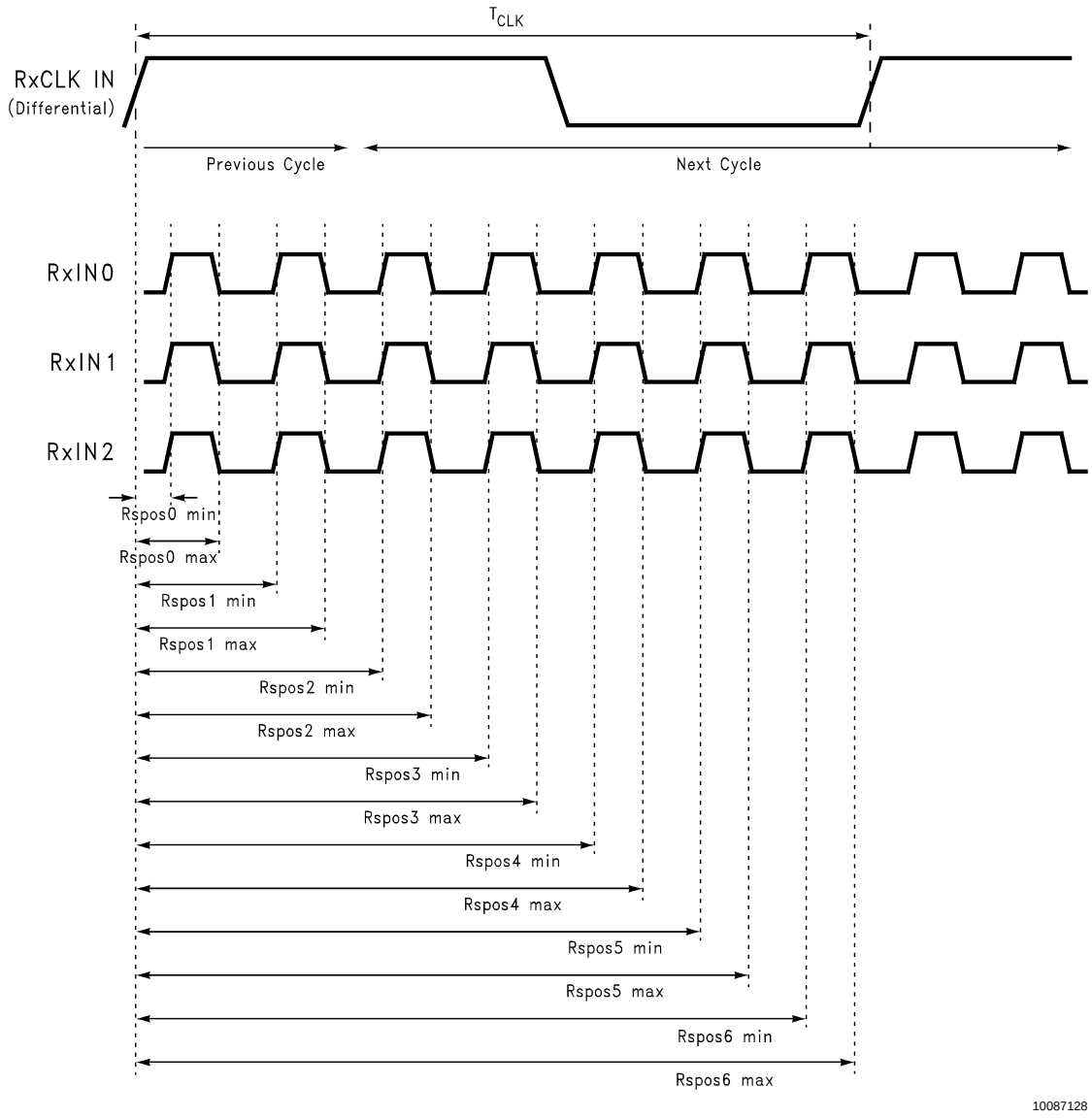
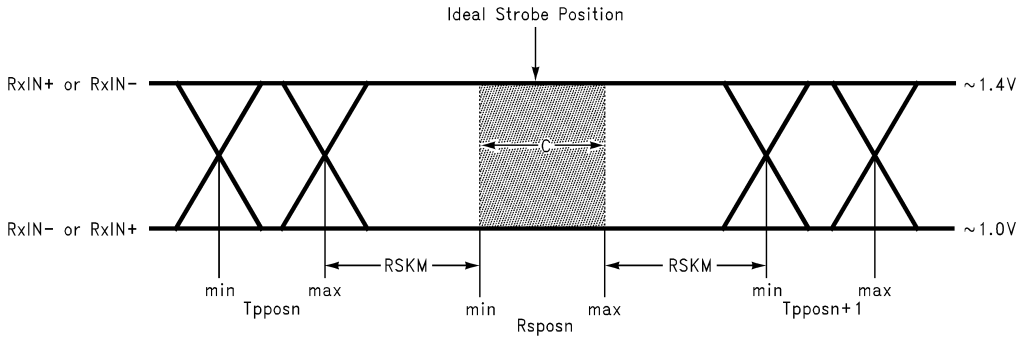


FIGURE 8. Receiver LVDS Input Strobe Position

AC Timing Diagrams (Continued)



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos — Transmitter output pulse position (min and max)

RSKM ≥ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 6) + ISI (Inter-symbol interference) (Note 7)

Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 6: Cycle-to-cycle jitter is less than 250 ps at 75MHz

Note 7: ISI is dependent on interconnect length; may be zero

FIGURE 9. Receiver LVDS Input Skew Margin (DS90CR217/DS90CR218)

DS90CR218 Pin Description—Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs. (Note 8)
RxIN−	I	3	Negative LVDS differential data inputs. (Note 8)
RxOUT	O	21	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	1	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Note 8: These receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

Applications Information

The DS90CR217 and DS90CR218 are backward compatible with the existing 5V Channel Link transmitter/receiver pair (DS90CR213, DS90CR214). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC}.
2. Transmitter input and control inputs except 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. The receiver powerdown feature when enabled will lock receiver output to a logic low. However, the 5V/66 MHz receiver maintain the outputs in the previous state when powerdown occurred.

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths ($<$ 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of 1.58 Gbit/s. Additional applications information can be found in the following National Interface Application Notes:

AN = ####	Topic
AN-1041	Introduction to Channel Link
AN-1108	PCB Design Guidelines for LVDS and Link Devices
AN-806	Transmission Line Theory
AN-905	Transmission Line Calculations and Differential Impedance
AN-916	Cable Information

CABLES: A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR217/218) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR287/288) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 130ps (@ 75 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common-mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

BOARD LAYOUT: To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high-speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

TERMINATION: Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. *Figure 10* shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

Applications Information (Continued)

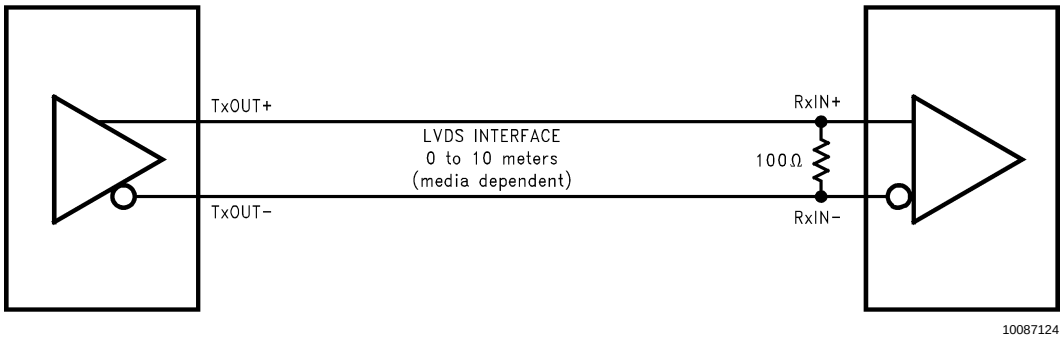


FIGURE 10. LVDS Serialized Link Termination

DECOUPLING CAPACITORS: Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01 µF and 0.001 µF. An example is shown in *Figure 11*. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

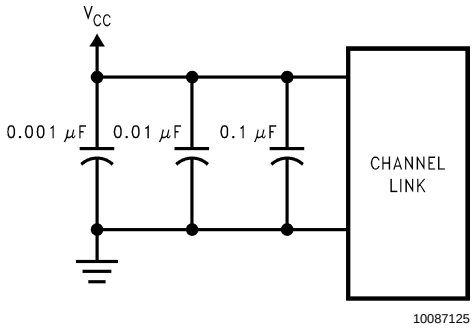


FIGURE 11. CHANNEL LINK Decoupling Configuration

CLOCK JITTER: The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 75 MHz clock has a period of 13.33 ns which results in a data bit width of 1.90 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

COMMON-MODE vs. DIFFERENTIAL MODE NOISE MARGIN: The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common-mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a ±1.0V shifting of the center point due to ground potential differences and common-mode noise.

TRANSMITTER INPUT CLOCK: The transmitter input clock must always be present when the device is enabled ($\overline{\text{PWR DWN}}$ = HIGH). If the clock is stopped, the $\overline{\text{PWR DWN}}$ pin must be used to disable the PLL. The $\overline{\text{PWR DWN}}$ pin must be held low until after the input clock signal has been reapplied. This will ensure a proper device reset and PLL lock to occur.

POWER SEQUENCING AND POWERDOWN MODE: Outputs of the CHANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The transmitter input clock may be applied prior to powering up and enabling the transmitter. The transmitter input clock may also be applied after power up; however, the use of the $\overline{\text{PWR DWN}}$ pin is required as described in the Transmitter Input Clock section. Do not power up and enable ($\overline{\text{PWR DWN}}$ = HIGH) the transmitter without a valid clock signal applied to the TxCLK IN pin.

Applications Information (Continued)

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

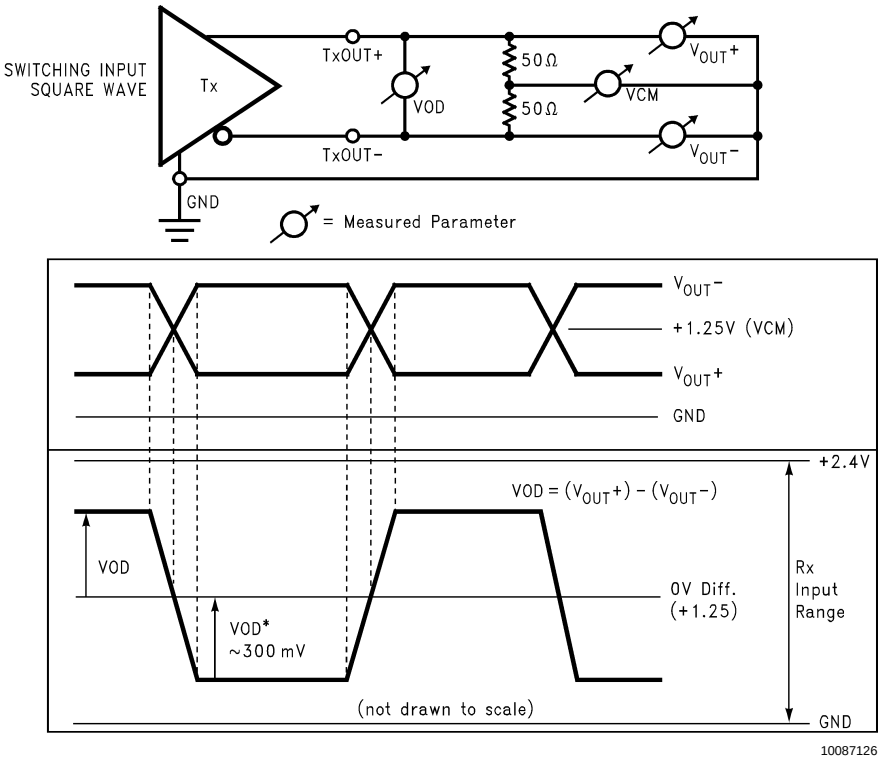
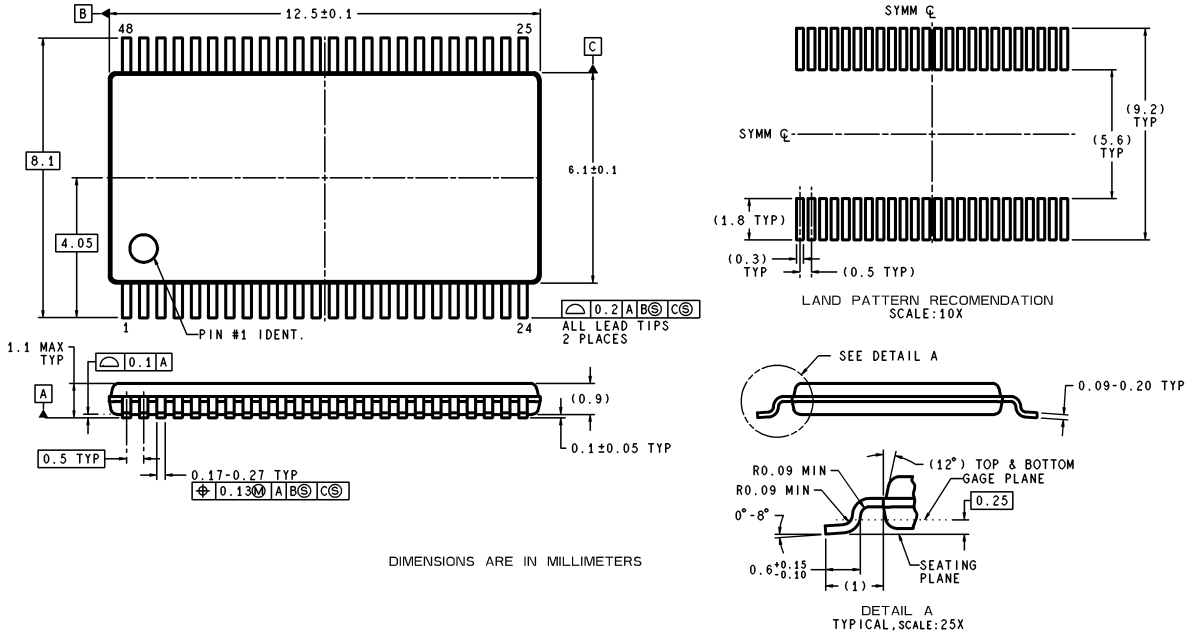


FIGURE 12. Single-Ended and Differential Waveforms

Physical Dimensions inches (millimeters)

unless otherwise noted



Order Number DS90CR218MTD
Dimensions in millimeters only
NS Package Number MTD48

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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