National Semiconductor

ADVANCE INFORMATION
April 2005

DS90C3202
3.3V 8 MHz to 135 MHz Dual FPD-Link Receiver

General Description

The DS90C3202 is a 3.3V single/dual FPD-Link 10-bit color receiver is designed to be used in Liquid Crystal Display TVs, LCD Monitors, Digital TVs, and Plasma Display Panel TVs. The DS90C3202 is designed to interface between the digital video processor and the display device using the low-power, low-EMI LVDS (Low Voltage Differential Signaling) interface. The DS90C3202 converts up to ten LVDS data streams back into 70 bits of parallel LVCMOS/LVTTL data. The receiver can be programmed with rising edge or falling edge clock. Optional two-wire serial programming allows fine tuning in development and production environments. With an input clock at 135 MHz, the maximum transmission rate of each LVDS line is 945 Mbps, for an aggregate throughput rate of 9.45 Gbps (945 Mbytes/s). This allows the dual 10-bit LVDS Receiver to support resolutions up to HDTV.

Features

- Up to 9.45 Gbit/s data throughput
- 8 MHz to 135 MHz input clock support
- Supports up to QXGA panel resolutions
- Supports HDTV panel resolutions and frame rates up to 1920 x 1080p
- LVDS 30-bit, 24-bit or 18-bit color data inputs
- Supports single pixel and dual pixel interfaces
- Supports spread spectrum clocking
- Two-wire serial communication interface
- Programmable clock edge and control strobe select
- Power down mode
- +3.3V supply voltage
- 128-pin TQFP Package
- Compliant to TIA/EIA-644-A-2001 LVDS Standard
- Backward compatible configuration with FPD-Link

Block Diagram

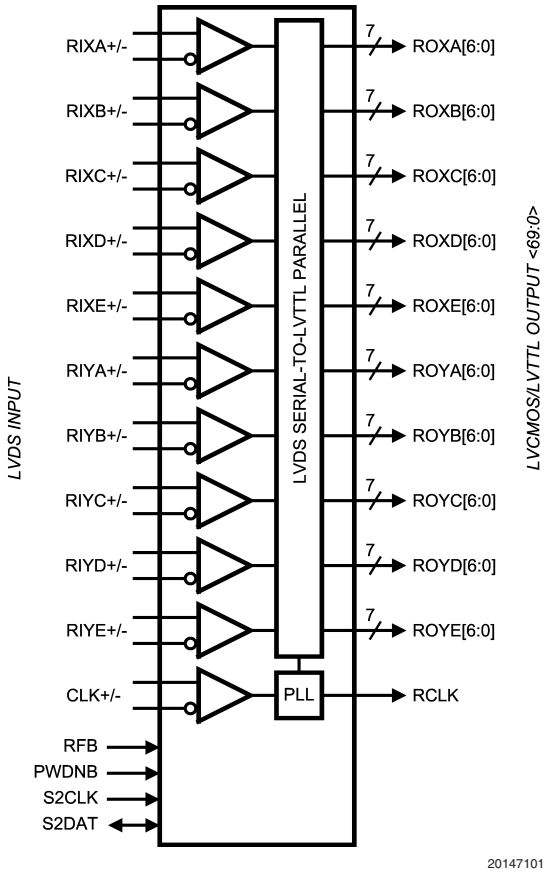


FIGURE 1. Receiver Block Diagram

Typical Application Diagram

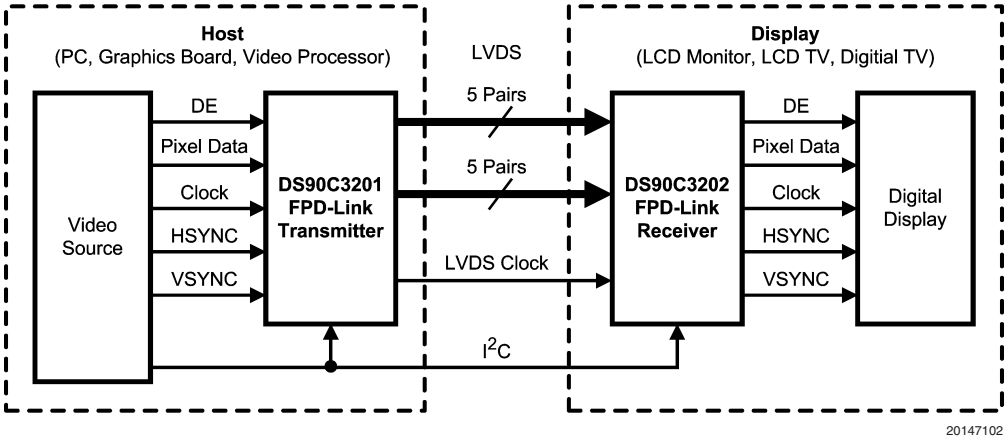


FIGURE 2. LCD Panel Application Diagram

Functional Description

The DS90C3201 and DS90C3202 are a dual 10-bit color Transmitter and Receiver FPD-Link chipset designed to transmit data at clocks speeds from 8 to 135 MHz. DS90C3201 and DS90C3202 are designed to interface between the digital video processor and the display using a LVDS interface. The DS90C3201 transmitter serializes 2 channels of video data (10-bit each for RGB for each channel, totaling 60 bits) and control signals (HSYNC, VSYNC, DE and two user-defined signals) along with clock signal to 10 channels of LVDS signals and transmits them. The DS90C3202 receiver converts 10 channels of LVDS signals into parallel signals and outputs 2 channels of video data (10-bit each for RGB for each channel, totaling 60 bits) and control signals (HSYNC, VSYNC, DE and two user-defined signals) along with clock signal. The dual high speed LVDS channels supports single pixel in-single pixel out and dual pixel in-dual pixel out transmission modes. The FPD-Link chipset is suitable for a variety of display applications including LCD Monitors, LCD TV, Digital TV, and DLP TV, and Plasma Display Panels.

Using a true 10-bit color depth system, the 30-bit RGB color produces over 1.07 billion colors to represent High Definition (HD) displays in their most natural color, surpassing the maximum 16.7 million colors achieved by 6/8-bit color conventionally used for large-scale LCD televisions and LCD monitors.

LVDS RECEIVER

The LVDS Receiver receives input RGB video data and control signal timing.

SELECTABLE OUTPUT DATA STROBE

The Receiver output data edge strobe can be latched on the rising or falling edges of clock signal. The dedicated RFB pin is used to program output strobe select on the rising edge of RCLK or the falling edge of RCLK.

2-WIRE SERIAL COMMUNICATION INTERFACE

Optional I2C programming allows fine tuning in development and production environments. The I2C interface provides several capabilities to reduce EMI and to customize output timing. These capabilities are selectable/programmable via I2C: Programmable Skew Rates, Progress Turn On Function, Input/Output Channel Control.

PROGRAMMABLE SKEW RATES

Programmable edge rates allow the LVCMOS/LVTTL Data and Clock outputs to be adjusted for better impedance matching for noise and EMI reduction. The individual output drive control registers for ROX[A-E], ROY[A-E], and RCLK are programmable via I2C.

PROGRESS TURN ON FUNCTION

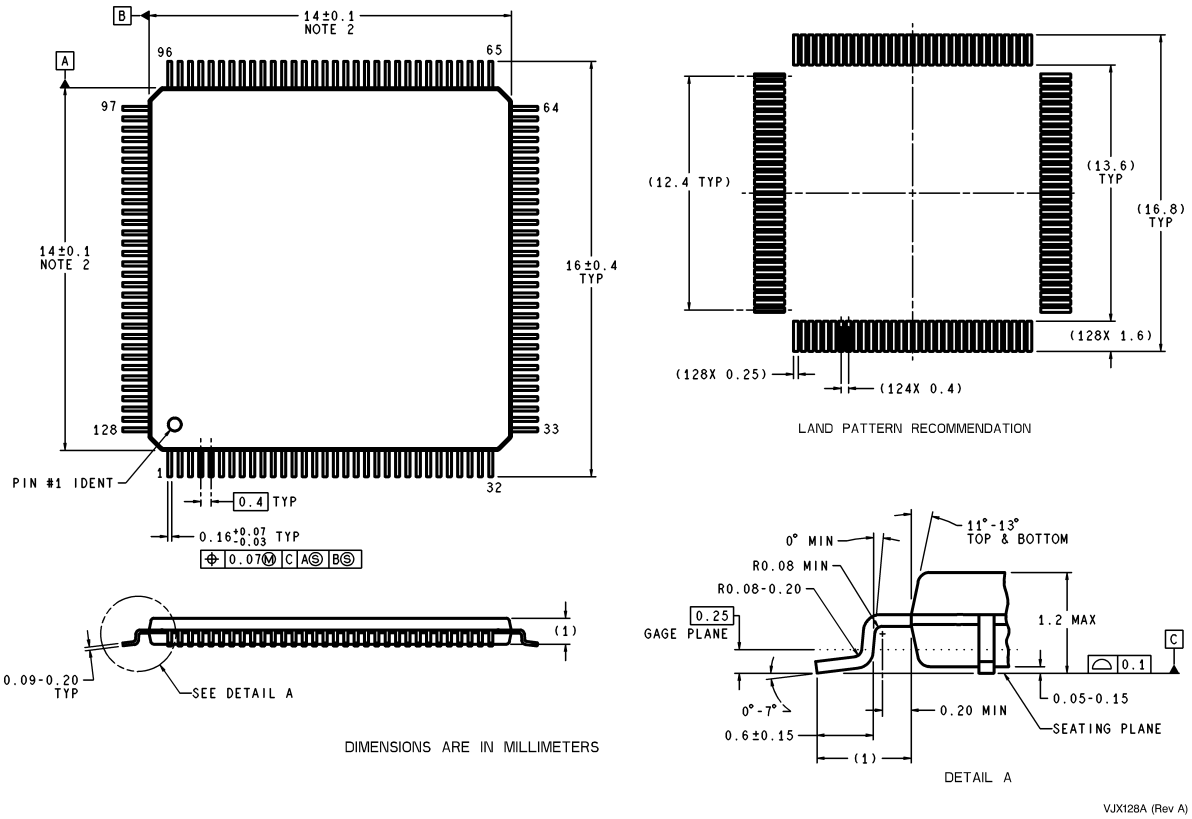
Progress Turn On (PTO) function aligns the two output channels of LVCMOS/LVTLL in either a non-skew data format (simultaneous switching) or a skewed data format (staggered). The skewed format delays the selected channel data and staggers the outputs. This reduces the number of outputs switching simultaneously, which lowers EMI radiation and minimizes ground bounce. Feature is controlled via I2C.

INPUT/OUTPUT CHANNEL CONTROL

Full independent control for input/output channels can be disabled to minimize power supply line noise and overall power dissipation. Feature is configured via I2C.

Physical Dimensions inches (millimeters)

unless otherwise noted



128-Pin TQFP Package
Order Number DS90C3202VS
NS Package Number VJX128A

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