National Semiconductor

September 2005

DS16F95QML
EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA standard RS-485 as well as RS-422A.

The DS16F95 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS16F95QML features lower power, extended temperature range and improved specifications.

The DS16F95 combines a TRI-STATE® differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

The DS16F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Radiation features DS16F95 guaranteed to 300k rd(Si)
- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHZ) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DISCRIPTION
DS16F95E/883	5962–89615012A	E20A	20LD LCC
DS16F95J/883	5962–8961501PA	J08A	8LD CERDIP
DS16F95J-QMLV	5962–8961501VPA	J08A	8LD CERDIP
DS16F95JFQML	5962F8961501QPA 300k rd(Si)	J08A	8LD CERDIP
DS16F95JFQMLV	5962F8961501VPA 300k rd(Si)	J08A	8LDS CERDIP
DS16F95W-SMD	5962–8961501HA	W10A	10LD CERPACK
DS16F95W/883		W10A	10LD CERPACK
DS16F95W-QMLV	5962–8961501VHA	W10A	10LD CERPACK
DS16F95WFQML	5962F8961501QHA 300k rd(Si)	W10A	10LD CERPACK
DS16F95WFQMLV	5962F8961501VHA 300k rd(Si)	W10A	10LD CERPACK
DS16F95WG/883	5962–8961501QXA	WG10A	10LD Ceramic SOIC
DS16F95WG-QMLV	5962–8961501VXA	WG10A	10LD Ceramic SOIC
DS16F95WGFQML	5962F8961501QXA 300k rd(Si)	WG10A	10LD Ceramic SOIC
DS16F95WGFQMLV	5962F8961501VXA 300k rd(Si)	WG10A	10LD Ceramic SOIC

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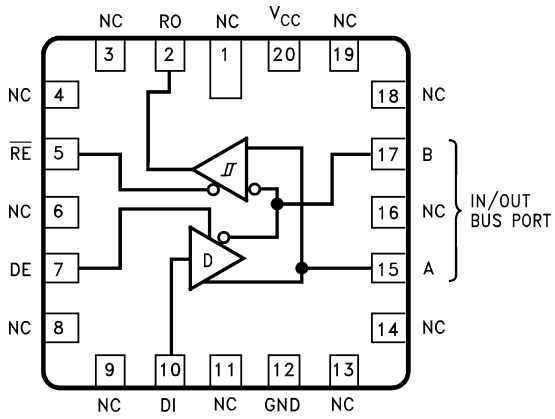
Connection Diagrams

20-Lead Ceramic Leadless Chip Carrier



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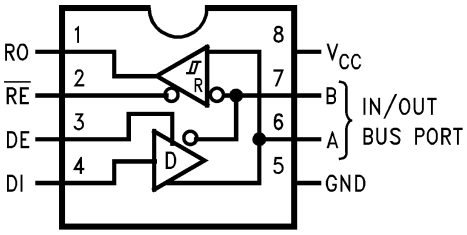
See NS Package Number E20A

8-Lead Dual-In-Line Package



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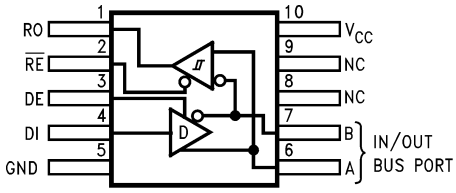
See NS Package Number J08A

10-Lead Flatpak/SOIC Package



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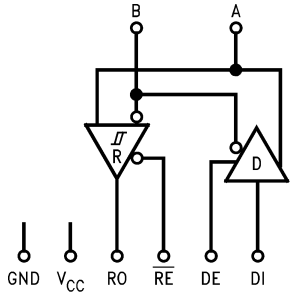
See NS Package Number W10A, WG10A

Logic Diagram



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Function Tables

Driver

Driver Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A–B	**$\overline{RE}$**	**RO**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

Absolute Maximum Ratings (Note 1)

Storage Temperature Range	$-65^{\circ}C \le T_A \le +175^{\circ}C$
Lead Temperature	
(Soldering, 60 sec.)	300˚C
Maximum Power Dissipation at 25˚C (Note 2)	
LCC 'E' Package	1800 mW
Cerdip 'J' Package	1274 mW
Cerpack 'W' Package	725 mW
Ceramic SOIC 'WG' Package	725 mW
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V
Junction Temperature (TJ)	+175˚C
Thermal Resistance	
θ_{JA}	
LCC 'E' Package	83˚C/W @ 0.5W
Cerdip 'J' Package	118˚C/W @ 1.0W
Cerpack 'W' Package	207˚C/W @ 0.5W
Ceramic SOIC 'WG' Package	207˚C/W @ 0.5W
θ_{JC}	
LCC 'E' Package	17˚C/W
Cerdip 'J' Package	14˚C/W
Cerpack 'W' Package	18˚C/W
Ceramic SOIC 'WG' Package	18˚C/W
ESD Tolerance (Note 3)	500V

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.50 to 5.50V
Voltage at Any Bus Terminal	
(Separately or Common Mode)	
(V_I or V_{CM})	−7.0V to +12V
Differential Input Voltage (V_{ID})	−7.0V to ±12V
Output Current HIGH (I_{OH})	
Driver	−60mA
Receiver	−400µA
Output Current LOW (I_{OL})	
Driver	60mA
Receiver	16mA
Operating Temperature (T_A)	−55˚C to +125˚C

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

DC - Driver Electrical Characteristics (Note 10)

The following conditions apply to all parameters, unless otherwise specified. V_{CC} = 5.5V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
VOD1	Differential Vout	V_{CC} = 5.5V, I_O = 0A, V_{IN} = .8V			6	V	1, 2, 3
		V_{CC} = 5.5V, I_O = 0A, V_{IN} = 2V			6	V	1, 2, 3
VOD2	Differential Vout	V_{CC} = 4.5V, R_L = 100Ω		2		V	1, 2, 3
	Figure 1	V_{CC} = 4.5V, R_L = 54Ω		1.5		V	1, 2, 3
Delta V_{OD}	Change In Differential Vout	V_{CC} = 4.5V, R_L = 100Ω	(Note 4)	-200	200	mV	1, 2, 3
		V_{CC} = 4.5V, R_L = 54Ω	(Note 4)	-200	200	mV	1, 2, 3
Delta V_{OC}	Change In Common Mode Vout	V_{CC} = 4.5V, R_L = 100Ω	(Note 4)	-200	200	mV	1, 2, 3
		V_{CC} = 4.5V, R_L = 54Ω	(Note 4)	-200	200	mV	1, 2, 3
V_{OC}	Common Mode Vout	R_L = 100Ω			3	V	1, 2, 3
		R_L = 54Ω			3	V	1, 2, 3
I_{IH}	Logical "1" Input Current	V_I = 2.4V			20	uA	1, 2, 3
I_O	Output Current	Output Disable, V_O = 12V			1	mA	1, 2, 3
		Output Disable, V_O = -7V	(Note 5)	-0.8		mA	1, 2, 3
		V_{CC} = 0, Output Disable, V_O = 12V			1	mA	1, 2, 3
		V_{CC} = 0, Output Disable, V_O = -7V	(Note 5)	-0.8		mA	1, 2, 3
I_{OS}	Output Short Circuit	V_{IN} = 3V, V_{OUT} = V_{CC}			150	mA	1, 2, 3
		V_{IN} = 3V, V_{OUT} = -7V	(Note 5)	-250		mA	1, 2, 3
		V_{IN} = 3V, V_{OUT} = 0V	(Note 5)	-150		mA	1, 2, 3
		V_{IN} = 3V, V_{OUT} = 12V			250	mA	1, 2, 3
		V_{IN} = 0V, V_{OUT} = 12V			250	mA	1, 2, 3
		V_{IN} = 0V, V_{OUT} = V_{CC}			150	mA	1, 2, 3
		V_{IN} = 0V, V_{OUT} = -7V	(Note 5)	-250		mA	1, 2, 3
		V_{IN} = 0V, V_{OUT} = 0V	(Note 5)	-150		mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_O = -20mA		3		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, I_O = 20mA			2	V	1, 2, 3
VOD3	Differential Vout	V_{CM} = -7V to 12V		1		V	1, 2, 3

DC - Receiver Electrical Characteristics (Note 10)

The following conditions apply to all parameters, unless otherwise specified. V_{CC} = 5.5V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
V_{OH}	Logical "1" Output Voltage ***Figure 2***	V_{CC} = 4.5V, V_{LD} = 200mV, I_{OH} = -400uA		2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage ***Figure 2***	V_{CC} = 4.5V, V_{LD} = -200mV, I_{OL} = 8mA			.45	V	1, 2, 3
		V_{CC} = 4.5V, V_{LD} = -200mV, I_{OL} = 16mA			.5	V	1, 2, 3
I_I	Line Input Current	Untested Input = 0V, V_I = 12V			1	mA	1, 2, 3
		Untested Input = 0V, V_I = -7V	(Note 5)	-.8		mA	1, 2, 3
		V_{CC} = 0V, Untested Input = 0V, V_I = 12V	(Note 5)		1	mA	1, 2, 3
		V_{CC} = 0V, Untested Input = 0V, V_I = -7V		-.8		mA	1, 2, 3
I_{IH}	Logical "1" Input Current	V_I = 2.7V (Receiver)			20	uA	1, 2, 3
R_{IN}	Input Resistance	Untested Input = 0V, V_I = 12V	(Note 6)	10		KΩ	1, 2, 3
		Untested Input = 0V, V_I = -7V	(Note 6)	10		KΩ	1, 2, 3
		V_{CC} = 0V, Untested Input = 0V, V_I = 12V	(Note 6)	10		KΩ	1, 2, 3
		V_{CC} = 0V, Untested Input = 0V, V_I = -7V	(Note 6)	10		KΩ	1, 2, 3
I_{OZ}	High Impedance State	V_I = .4V		-20	20	uA	1, 2, 3
		V_I = 2.4V		-20	20	uA	1, 2, 3
I_{OS}	Output Short Circuit	V_{IN} = 1V, V_{OUT} = 0V		-85	-15	mA	1, 2, 3
V_{TH}	Differential Input High Threshold	V_{CC} = 4.5V, V_O = 2.5V, V_{CM} = 12V & 0V & -7V, I_O = -.4mA			.2	V	1, 2, 3
		VCC = 5.5V, Vo = 2.5V, VCM = 12V & 0V & -7V, I_O = -.4mA			.2	V	1, 2, 3
V_T1	Differential Input Low Threshold	V_{CC} = 4.5V, V_O = .5V, V_{CM} = 12V & 0V & -7V, I_O = 8mA		-.2		V	1, 2, 3
		V_{CC} = 5.5V, V_O = .5V, V_{CM} = 12V & 0V & -7V, I_O = 8mA		-.2		V	1, 2, 3
V_{TH}+ - (V_{TH}-)	Hyteresis	V_{CC} = 4.5V, V_{CM} = 0V		35		mV	1, 2, 3
		V_{CC} = 5.5V, V_{CM} = 0V		35		mV	1, 2, 3

DC - Both Driver and Receiver Electrical Characteristics (Note 10)

The following conditions apply to all parameters, unless otherwise specified. V_{CC} = 5.5V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
I_{CC}	Supply Current I_{CC} Both Disable	$\overline{RE}$ = 2V, $\overline{DE}$ = .8V			25	mA	1, 2, 3
I_{CC}	Supply Current I_{CC} Both Enable	$\overline{RE}$ =.8V, $\overline{DE}$ = 2V			28	mA	1, 2, 3
V_{IC}	Input Clamp Volt	I_I = -18mA		-1.3		V	1, 2, 3
V_{IH}	Logical "1" Input Voltage			2		V	1, 2, 3
V_{IL}	Logical "0" Input Voltage				.8	V	1, 2, 3
V_{IH}	Logical "1" Enable Input Voltage			2		V	1, 2, 3
V_{IL}	Logical "0" Enable Input Voltage				.8	V	1, 2, 3
I_{IL}	Logical "0" Input Current	V_I = .4V	(Note 5)	-50		uA	1, 2, 3

AC - Driver Electrical Characteristics (Note 10)

The following conditions apply to all parameters, unless otherwise specified.

V_{CC} = 5V, PRR = 1MH$_Z$, $T_R \le T_F \le$ 6nS, 50% duty cycle, AMP = 3V, VL_O, Z_{OUT} = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
t_{DD}	Differential Output Delay Time ***Figure 3***	RL = 60Ω	(Note 9)	8	25	nS	9
			(Note 9)	8	30	nS	10, 11
t_{TD}	Differential Output Transition Time ***Figure 3***	RL = 60Ω	(Notes 8, 9)	8	25	nS	9
			(Notes 8, 9)	8	30	nS	10, 11
t_{PLH}	Propagation Delay Time Low to High ***Figure 4***	RL = 27Ω		6	18	nS	9
				6	25	nS	10, 11
t_{PHL}	Propagation Delay Time high to Low ***Figure 4***	RL = 27Ω		6	18	nS	9
				6	25	nS	10, 11
t_{PZH}	Output Enable Time to H ***Figure 5***	RL = 110Ω			35	nS	9
					45	nS	10, 11
t_{PZL}	Output Enable Time to L ***Figure 6***	RL = 110Ω			40	nS	9
					50	nS	10, 11
t_{PHZ}	Output Disable Time to H ***Figure 5***	RL = 110Ω			30	nS	9
					40	nS	10, 11
t_{PLZ}	Output Disable Time to L ***Figure 6***	RL = 110Ω			30	nS	9
					40	nS	10, 11
T_{SKEW}	Differential Output Skew Time ***Figure 3***				6	nS	9
					12	nS	10, 11

AC - Receiver Electrical Characteristics (Note 10)

The following conditions apply to all parameters, unless otherwise specified.

V_{CC} = 5V, PRR = 1MH$_Z$, $T_R \le T_F \le$ 6nS, 50% duty cycle, AMP = 3V, VL_O, Z_{OUT} = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
t_{PLH}	Propagation Delay Time Low to High ***Figure 7***	C_L = 15pF		10	27	nS	9
				10	38	nS	10, 11
t_{PHL}	Propagation Delay Time High to Low ***Figure 7***	C_L = 15pF		10	27	nS	9
				10	38	nS	10, 11
t_{PZH}	Output Enable Time to H ***Figure 8***	C_L = 15pF			20	nS	9
					30	nS	10, 11
t_{PZL}	Output Enable Time to L ***Figure 8***	C_L = 15pF			20	nS	9
					30	nS	10, 11
$\lvert t_{PLH} - t_{PHL} \rvert$	Output to Output Delay Time ***Figure 7***				8	nS	9
					16	nS	10, 11
t_{PHZ}	Output Disable Time From H ***Figure 8***	C_L = 20pF	(Notes 7, 15)		30	nS	9
			(Note 7)		40	nS	10, 11
		C_L = 5pF	(Note 7)		20	nS	9
			(Note 7)		30	nS	10, 11
t_{PLZ}	Output Disable Time From L ***Figure 8***	C_L = 5pF			20	nS	9
					30	nS	10, 11

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Above T_A = 25˚C, derate E package 12.1mW˚C, J package 8.5 mW/˚C, W & WG package 4.8mW/˚C.

Note 3: Human body model, 1.5kΩ in series with 100pF

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: Negative sign of the limits indicates the direction of the current flow only.

Note 6: R_{IN} is guaranteed by testing "Line Input Current" (II).

Note 7: Testing at 20pF assures conformance to spec at 5pF.

Note 8: tTD = Non-inverting output rise time + inverting output fall time / 2, Non-inverting output fall time + inverting output rise time / 2.

Note 9: Rise time 20% to 80%, Fall time 80% to 20%.

Note 10: Pre and post irradiation limits are identical to those listed under A C and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD 883, Method 1019, condition A.

Parameter Measurement Information

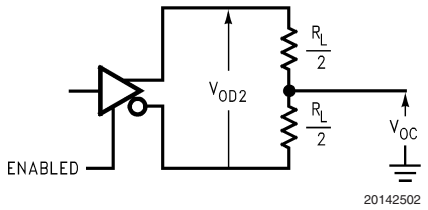


FIGURE 1. Driver V_{OD} and V_{OC} (Note 14)

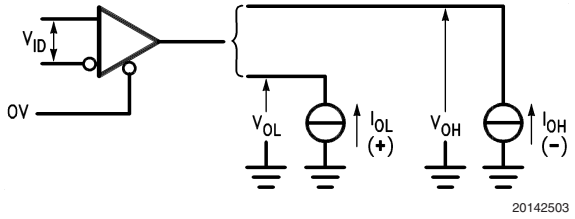
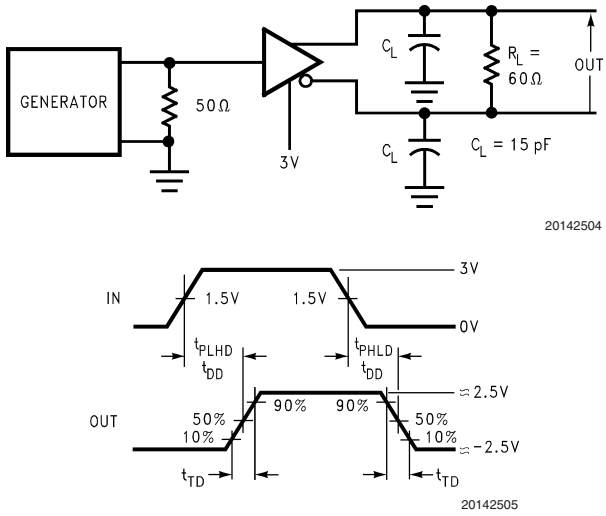


FIGURE 2. Receiver V_{OH} and V_{OL}

Parameter Measurement Information (Continued)



$t_{SKEW} = |t_{PLHD} - t_{PHLD}|$

FIGURE 3. Driver Differential Output Delay and Transition Times (Notes 11, 13)

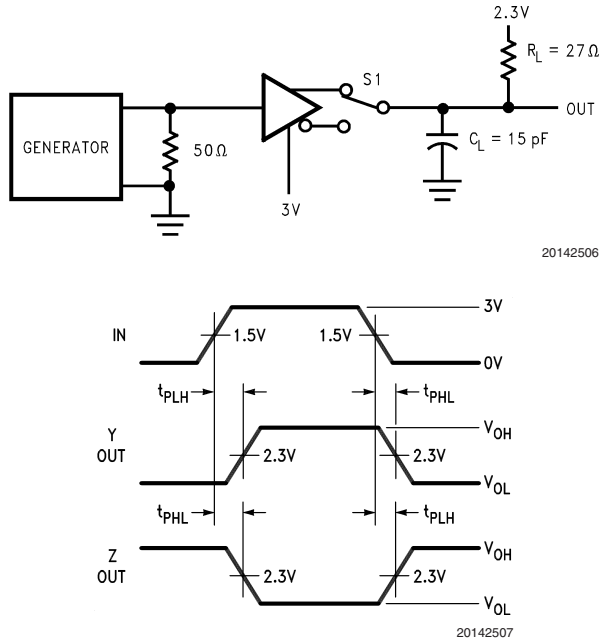


FIGURE 4. Driver Propagation Times (Notes 11, 12)

Parameter Measurement Information (Continued)

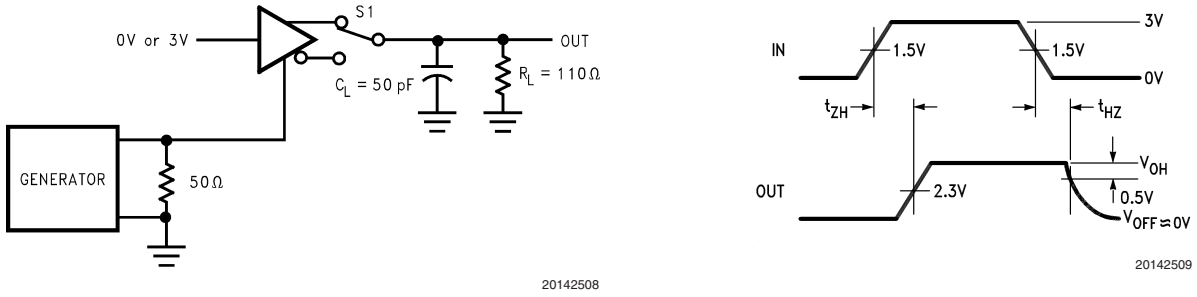


FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ}) (Notes 11, 12, 13)

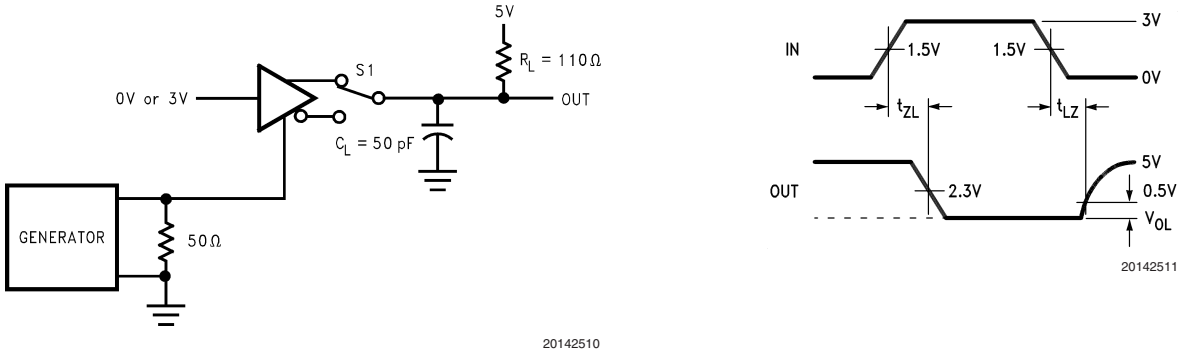


FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ}) (Notes 11, 12, 13)

FIGURE 7. Receiver Propagation Delay Times (Notes 11, 12)

Parameter Measurement Information (Continued)

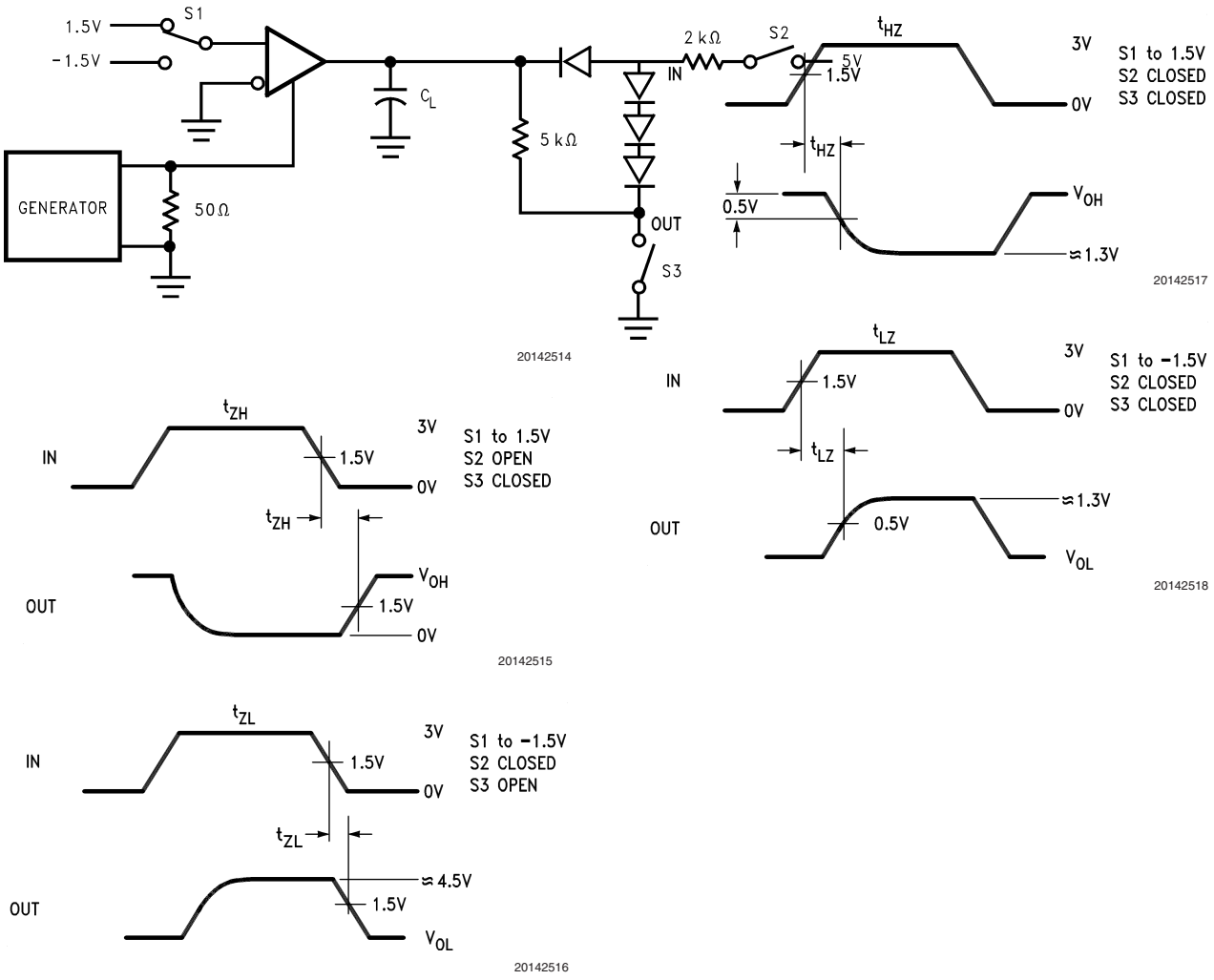


FIGURE 8. Receiver Enable and Disable Times (Notes 11, 12, 14)

Note 11: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

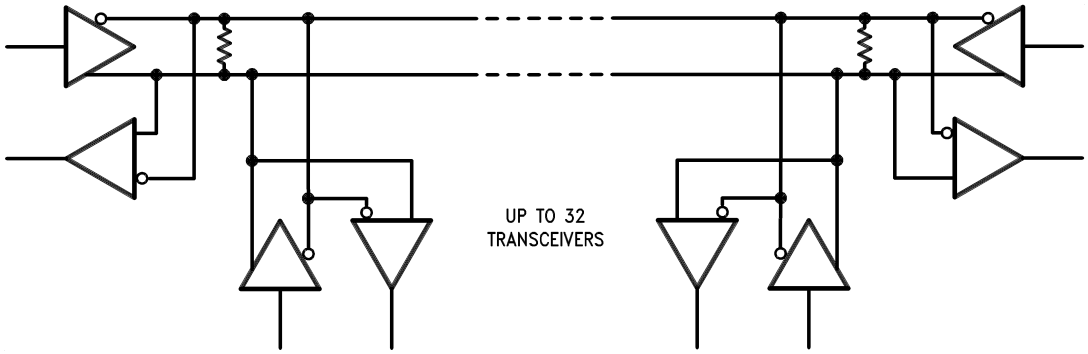
Note 12: C_L includes probe and stray capacitance.

Note 13: DS16F95 Driver enable is Active-High.

Note 14: All diodes are 1N916 or equivalent.

Note 15: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application



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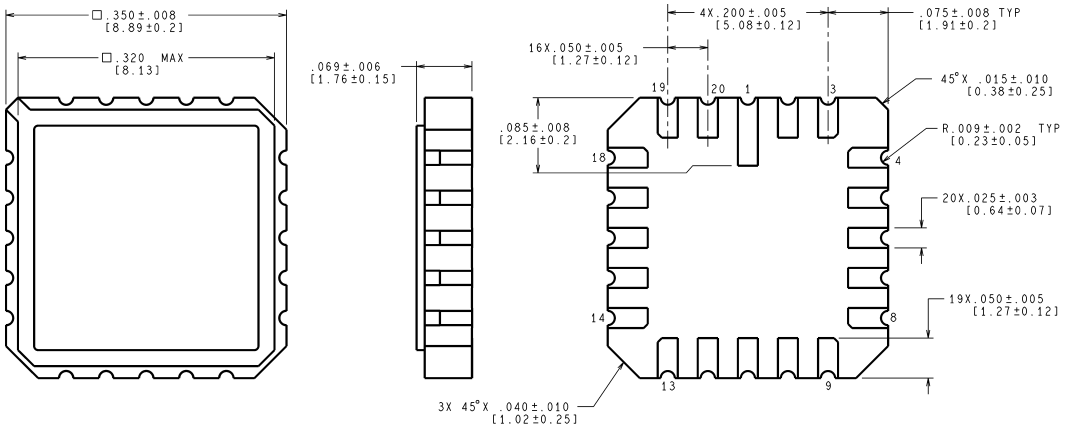
The line should be terminated at both ends in its characteristic impedance, typically 120Ω.

Stub lengths off the main line should be kept as short as possible.

Revision History

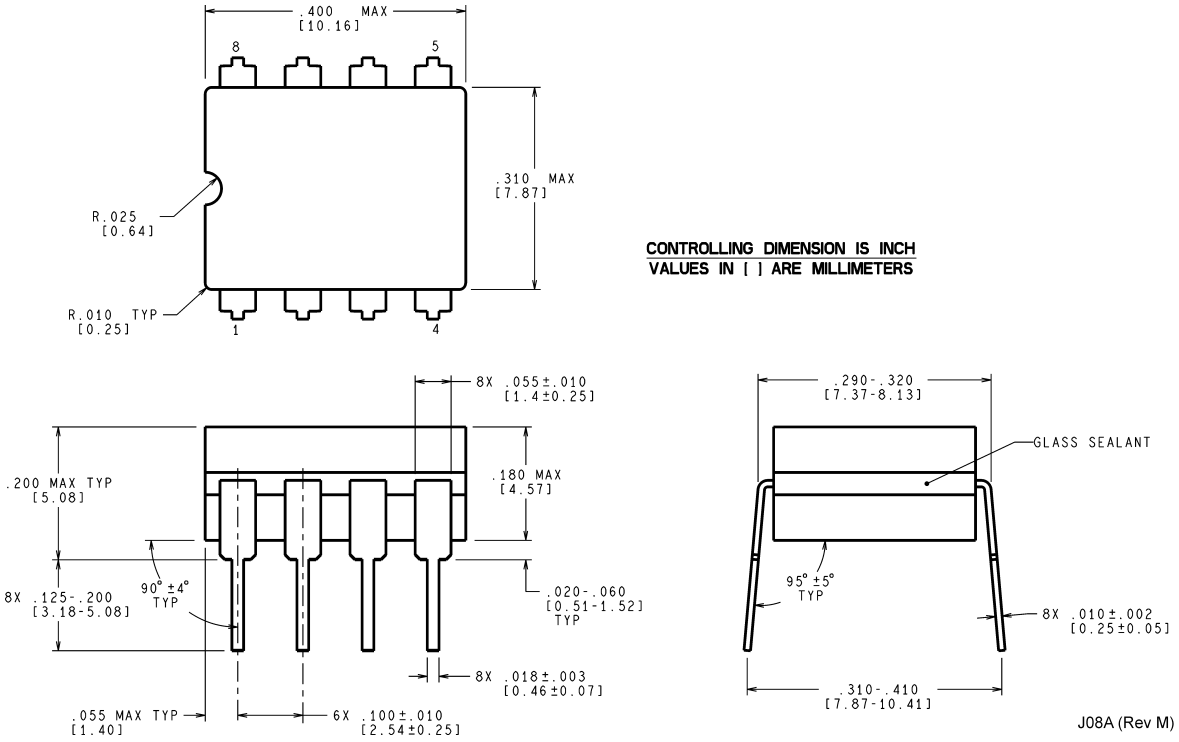
Date Released	Revision	Section	Originator	Changes
	A	New Release, Corporate format	R. Malone	1 MDS data sheet converted into Corporate data sheet format. MDS data sheet MNDS16F95-X-RH, Rev. 0A1 will be Archived.

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (Rev F)

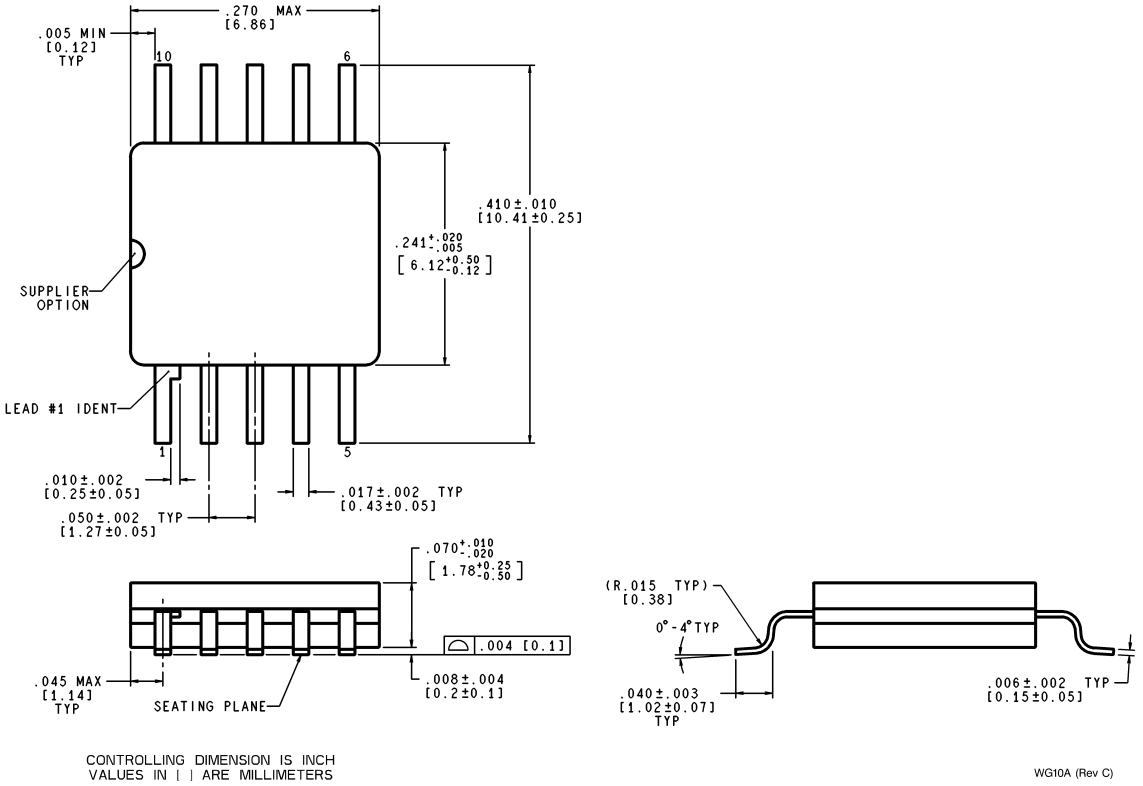
20-Lead Ceramic Leadless Chip Carrier (E)
NS Package Number E20A



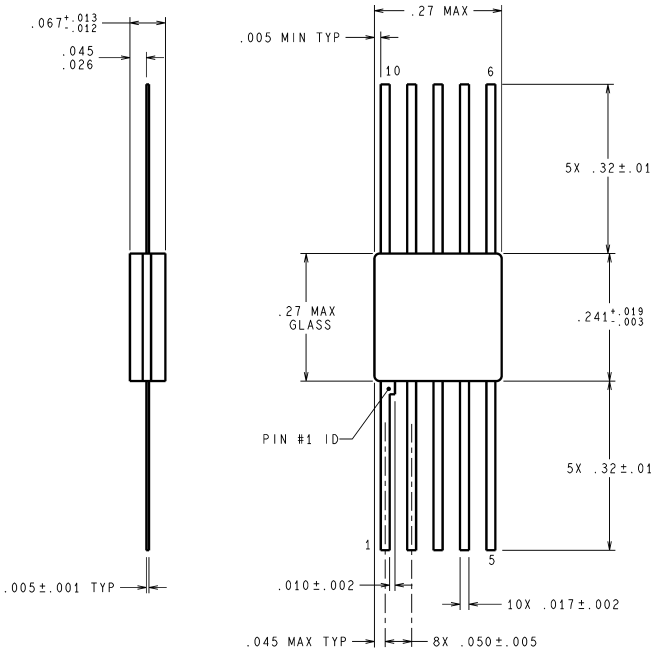
J08A (Rev M)

8 Narrow Lead Ceramic Dual-In-Line Package (J)
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Lead Ceramic SOIC (WG)
NS Package Number WG10A



10-Lead Ceramic Flatpak (W)
NS Package Number W10A

Notes

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