

## DP84240/DP84244 Octal TRI-STATE<sup>®</sup> MOS Drivers

### General Description

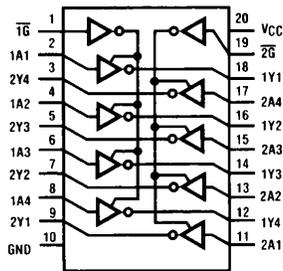
The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

TRI-STATE<sup>®</sup> is a registered trademark of National Semiconductor Corp.

### Features

- $t_{pd}$  specified with 250 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

### Connection Diagram



Top View

Order Number DP84240J or DP84240N  
See NS Package Numbers J20A or N20A

### Truth Table

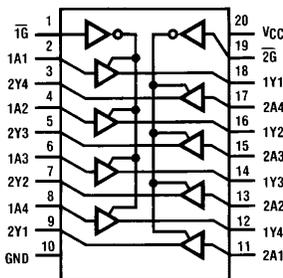
DP84240

| Inputs    |   | Outputs |
|-----------|---|---------|
| $\bar{G}$ | A | Y       |
| H         | X | Z       |
| L         | L | H       |
| L         | H | L       |

H = High Level  
L = Low Level  
X = Don't Care  
Z = High Impedance

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DP84244



Top View

Order Number DP84244J or DP84244N  
See NS Package Numbers J20A or N20A

| Inputs    |   | Outputs |
|-----------|---|---------|
| $\bar{G}$ | A | Y       |
| H         | X | Z       |
| L         | L | L       |
| L         | H | H       |

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                       |                 |
|---------------------------------------|-----------------|
| Supply Voltage, $V_{CC}$              | 7.0V            |
| Logical "1" Input Voltage             | 7.0V            |
| Logical "0" Input Voltage             | -1.5V           |
| Storage Temperature Range             | -65°C to +150°C |
| Power Dissipation                     |                 |
| Cavity Package                        | 1150 mW         |
| Molded Package                        | 1300 mW         |
| Lead Temperature (soldering, 10 sec.) | 300°C           |

## Operating Conditions

|                           | Min | Max | Units |
|---------------------------|-----|-----|-------|
| $V_{CC}$ Supply Voltage   | 4.5 | 5.5 | V     |
| $T_A$ Ambient Temperature | 0   | +70 | °C    |

## Electrical Characteristics $V_{CC} = 5V \pm 10\%$ , $0 \leq T_A \leq 70^\circ\text{C}$ . (Notes 2 and 3.)

| Symbol      | Parameter                  | Conditions  | Min             | Typ              | Max              | Units         |
|-------------|----------------------------|---|-----------------|------------------|------------------|---------------|
| $V_{IN(1)}$ | Logical "1" Input Voltage  |   | 2.0             |                  |                  | V             |
| $V_{IN(0)}$ | Logical "0" Input Voltage  |   |                 |                  | 0.8              | V             |
| $I_{IN(1)}$ | Logical "1" Input Current  | $V_{IN} = 2.7V$   |                 | 0.1              | 20               | $\mu\text{A}$ |
|             |                            | $V_{IN} = 7.0V$   |                 |                  | 100              | $\mu\text{A}$ |
| $I_{IN(0)}$ | Logical "0" Input Current  | $0 \leq V_{IN} \leq 0.4V$   |                 | -50              | -200             | $\mu\text{A}$ |
| $V_{CLAMP}$ | Input Clamp Voltage        | $I_{IN} = -18 \text{ mA}$   |                 | -1               | -1.2             | V             |
| $V_{OH}$    | Logical "1" Output Voltage | $I_{OH} = -100 \mu\text{A}$   | $V_{CC} - 1.15$ | 4.3              |                  | V             |
|             |                            | $I_{OH} = -1 \text{ mA}$  | $V_{CC} - 1.5$  | 3.9              |                  |               |
| $V_{OL}$    | Logical "0" Output Voltage | $I_{OL} = 10 \mu\text{A}$   |                 | 0.2              | 0.4              | V             |
|             |                            | $I_{OL} = 12 \text{ mA}$  |                 | 0.3              | 0.5              |               |
| $I_{1D}$    | Logical "1" Drive Current  | $V_{OUT} = 1.5V$  | -75             | -250             |                  | mA            |
| $I_{0D}$    | Logical "0" Drive Current  | $V_{OUT} = 1.5V$  | +100            | +150             |                  | mA            |
| Hi-Z        | TRI-STATE Output Current   | $0.4V \leq V_{OUT} \leq 2.7V$   | -100            |                  | +100             | $\mu\text{A}$ |
| $I_{CC}$    | Supply Current<br>DP84240  | All Outputs Open<br>All Outputs High<br>All Outputs Low<br>All Outputs Hi-Z |                 | 16<br>74<br>80   | 50<br>125<br>125 | mA            |
|             | DP84244                    | All Outputs High<br>All Outputs Low<br>All Outputs Hi-Z                     |                 | 40<br>100<br>115 | 75<br>130<br>150 |               |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

**Note 3:** Typical characteristics are taken at  $V_{CC} = 5.0V$  and  $T_A = 25^\circ\text{C}$ .

**Note 4:** The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See Figures 5 and 6 for the switching time variations.

**Switching Characteristics**  $V_{CC} = 5V \pm 10\%$ ,  $0 \leq T_A \leq 70^\circ C$ , all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

| Symbol     | Parameter                                 | Conditions   | Min | Typ | Max | Units |
|------------|---|--|-----|-----|-----|-------|
| $t_{PLH}$  | Propagation Delay from LOW-to-HIGH Output | <i>Figures 1 &amp; 3</i><br>CL = 250 pF<br>CL = 500 pF | 9   | 16  | 27  | ns    |
|            |   |  | 10  | 20  | 33  |       |
| $t_{PHL}$  | Propagation Delay from HIGH-to-LOW Output | <i>Figures 1 &amp; 3</i><br>CL = 250 pF<br>CL = 500 pF | 9   | 16  | 25  | ns    |
|            |   |  | 12  | 20  | 31  |       |
| $t_{PLZ}$  | Output Disable Time from LOW              | <i>Figures 2 &amp; 4</i> , S = 1, CL = 50 pF           |     | 11  | 24  | ns    |
| $t_{PHZ}$  | Output Disable Time from HIGH             | <i>Figures 2 &amp; 4</i> , S = 2, CL = 50 pF           |     | 12  | 24  | ns    |
| $t_{PZL}$  | Output Enable Time to LOW                 | <i>Figures 2 &amp; 4</i> , S = 1, CL = 500 pF          |     | 30  | 45  | ns    |
| $t_{PZH}$  | Output Enable Time to HIGH                | <i>Figures 2 &amp; 4</i> , S = 2, CL = 500 pF          |     | 23  | 35  | ns    |
| $t_{SKEW}$ | Output-to-Output Skew (Note 4)            | <i>Figures 1 &amp; 3</i> , CL = 500 pF                 |     | 3   |     | ns    |

**Capacitance**  $T_A = 25^\circ C$ ,  $f = 1 \text{ MHz}$ ,  $V_{CC} = 5V \pm 10\%$ . (Note 3.)

| Parameter | Conditions                | Typ | Units |
|-----------|---------------------------|-----|-------|
| $C_{IN}$  | All Other Inputs Tied Low | 6   | pF    |
| $C_{OUT}$ | Output in TRI-STATE Mode  | 20  | pF    |

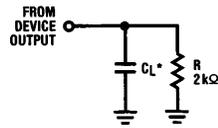
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

**Note 3:** Typical characteristics are taken at  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .

**Note 4:** The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5 and 6* for the switching time variations.

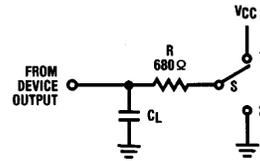
## Switching Test Circuits



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\* $C_L$  INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching

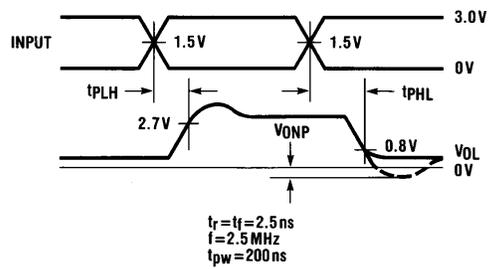


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FIGURE 2. TRI-STATE Enable/Disable

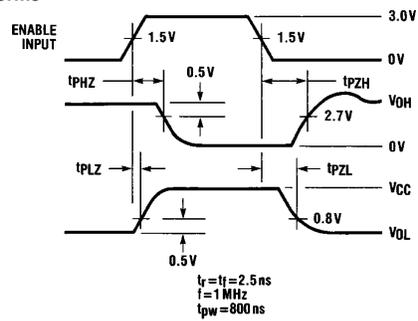
## Typical Switching Characteristics

### Voltage Waveforms



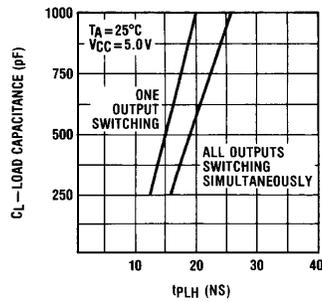
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FIGURE 3. Output Drive Levels



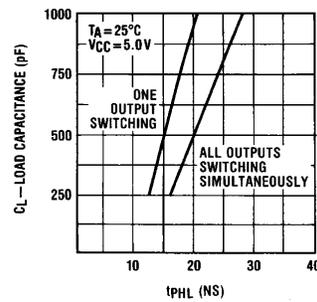
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FIGURE 4. TRI-STATE Control Levels



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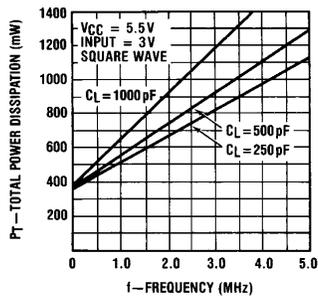
FIGURE 5.  $t_{PLH}$  Measured to 2.7V on Output vs.  $C_L$



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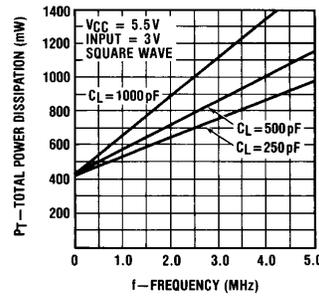
FIGURE 6.  $t_{PLH}$  Measured to 0.8V on Output vs.  $C_L$

## Typical Switching Characteristics (Continued)



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FIGURE 7. Typical Power Dissipation for DP84240 at  $V_{CC} = 5.5\text{ V}$  (All 8 drivers switching simultaneously)

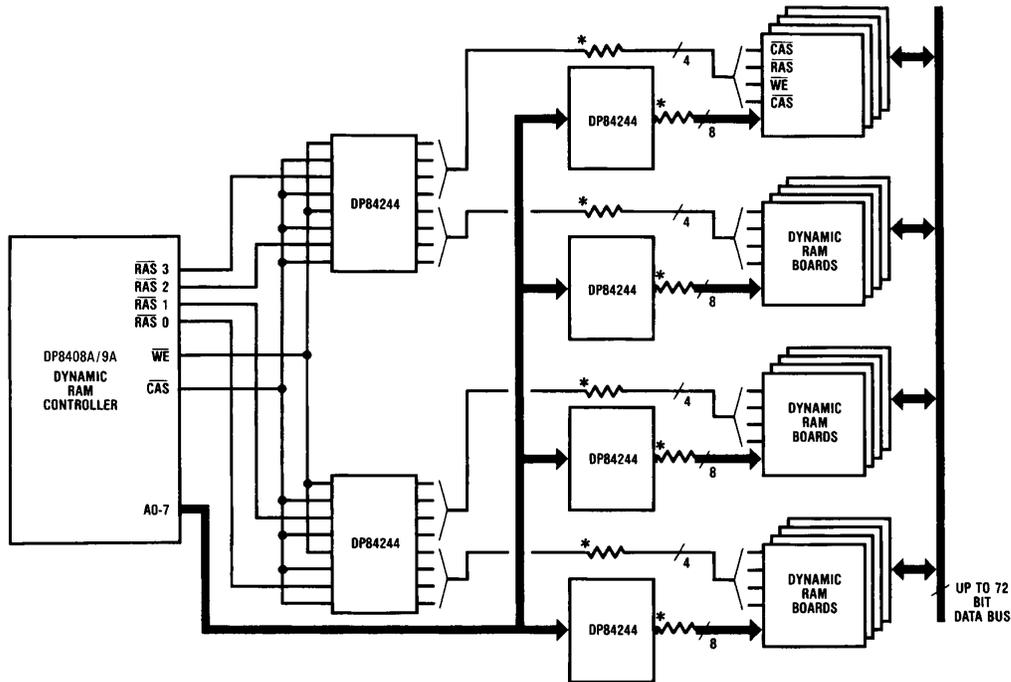


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FIGURE 8. Typical Power Dissipation for DP84244 at  $V_{CC} = 5.5\text{ V}$  (All 8 drivers switching simultaneously)

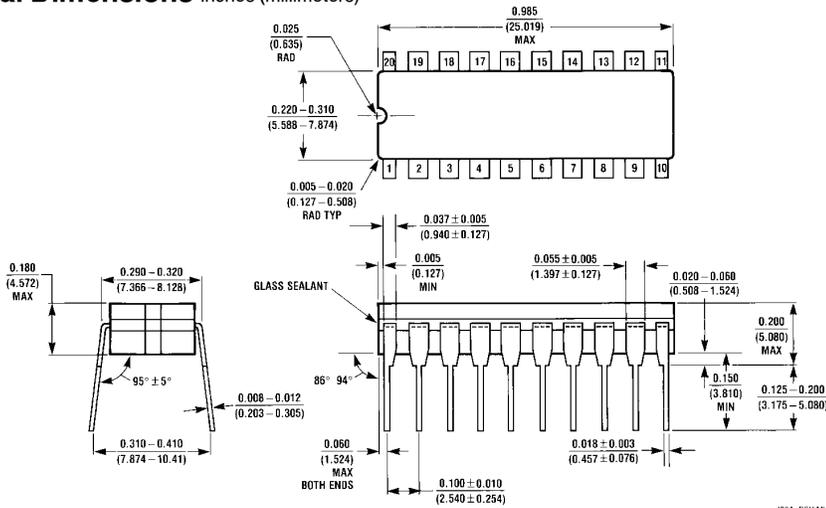
## Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)

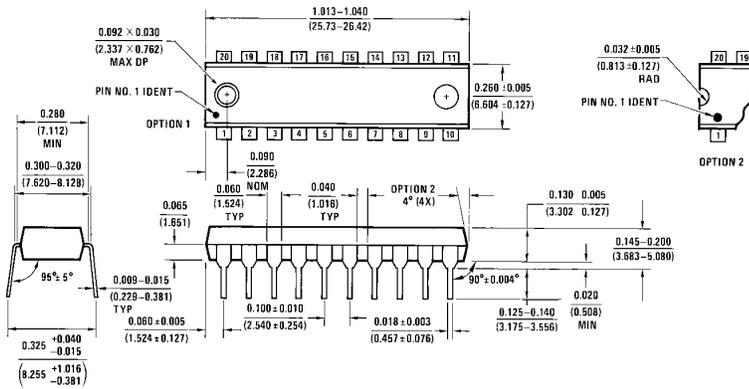


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**Physical Dimensions** inches (millimeters)



**20-Lead Dual-In-Line Package (J)**  
**Order Number DP84240J/DP84244J**  
**NS Package Number J20A**



**20-Lead Dual-In-Line Package (N)**  
**Order Number DP84240N/DP84244N**  
**NS Package Number N20A**

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