National Semiconductor

PRELIMINARY
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DP8402A/DP8403/DP8404/DP8405 32-Bit Parallel Error Detection and Correction Circuits (EDAC's)

DP8402A/DP8403/DP8404/DP8405 32-Bit Parallel Error Detection and Correction Circuits (EDAC's)

General Description

The DP8402A, DP8403, DP8404 and DP8405 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin DP8402A and DP8403 or 48-pin DP8404 and DP8405 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Double bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

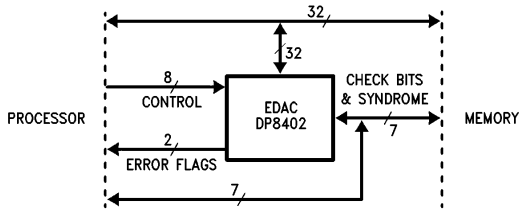
Read-modify-write (byte-control) operations can be performed with the DP8402A and DP8403 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB}}$0 thru $\overline{\text{OEB}}$3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

Features

- Detects and corrects single-bit errors
- Detects and flags double-bit errors
- Built-in diagnostic capability
- Fast write and read cycle processing times
- Byte-write capability . . . DP8402A and DP8403
- Fully pin and function compatible with TI's SN74ALS632A thru SN74ALS635 series

System Environment



TL/F/8535–1

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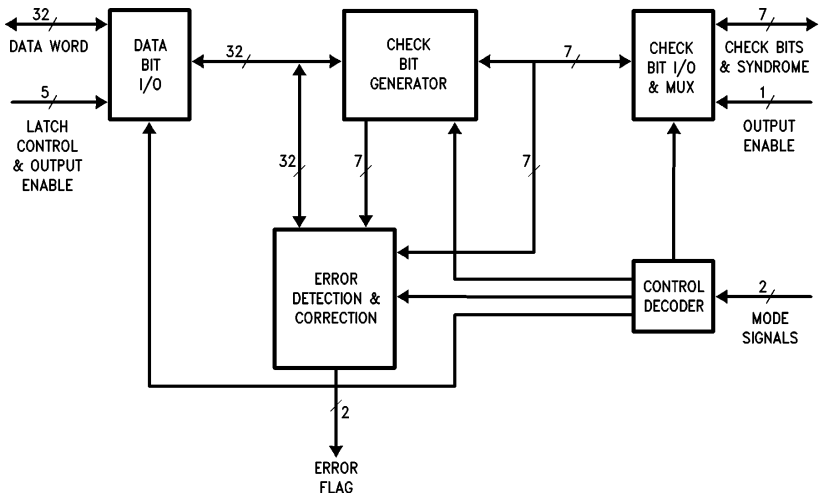
Simplified Functional Block and Connection Diagrams



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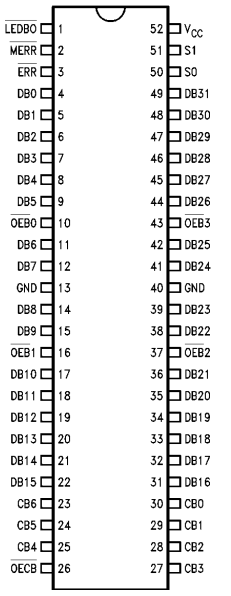
Device	Package	Byte-Write	Output
DP8402A	52-pin	yes	TRI-STATE®
DP8403	52-pin	yes	Open-Collector
DP8404	48-pin	no	TRI-STATE
DP8405	48-pin	no	Open-Collector

Dual-In-Line Packages



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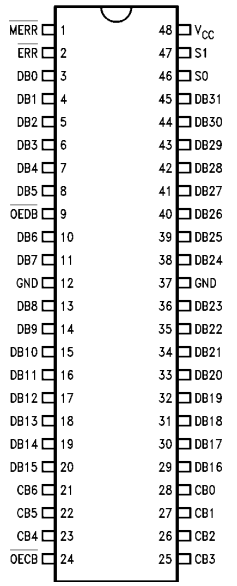
Top View



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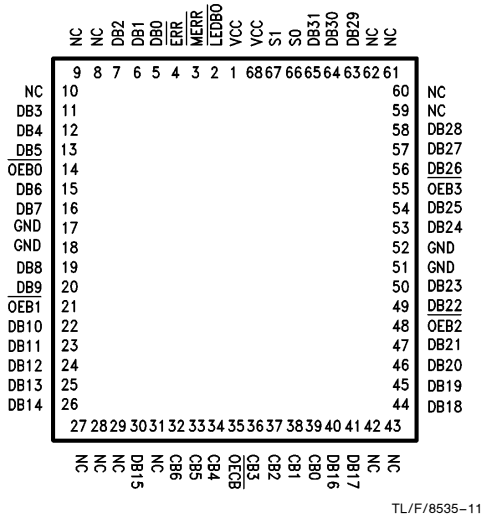
Top View

Order Number DP8402AD, DP8403D, DP8404D or DP8405D
See NS Package Number D48A or D52A

Plastic Chip Carrier



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Top View

Order Number DP8402AV
See NS Package Number V68A

Mode Definitions

MODE	PIN NAME S1	S0	DESCRIPTION MODE	OPERATION
0	L	L	WRITE	Input dataword and output checkword
1	L	H	DIAGNOSTICS	Input various data words against latched checkword/output valid error flags.
2	H	L	READ & FLAG	Input dataword and output error flags
3	H	H	CORRECT	Latched input data and checkword/output corrected data and syndrome code

Pin Definitions

S0, S1	Control of EDAC mode, see preceding Mode Definitions
DB0 thru DB31	I/O port for 32 bit dataword.
CB0 thru CB6	I/O port for 7 bit checkword. Also output port for the syndrome error code during error correction mode.
$\overline{OEB0}$ thru $\overline{OEB3}$ (DP8402A, DP8403)	Dataword output buffer enable. When high, output buffers are at TRI-STATE. Each pin controls 8 I/O ports. $\overline{OEB0}$ controls DB0 thru DB7, $\overline{OEB1}$ controls DB8 thru DB15, $\overline{OEB2}$ controls DB16 thru DB23 and $\overline{OEB3}$ controls DB24 thru DB31.
$\overline{LEDBO}$ (DP8402A, DP8403)	Data word output Latch enable. When high it inhibits input to the Latch. Operates on all 32 bits of the dataword.
$\overline{OEDB}$ (DP8404, DP8405)	TRI-STATE control for the data I/O port. When high output buffers are at TRI-STATE.
$\overline{OECB}$	Checkword output buffer enable. When high the output buffers are in TRI-STATE mode.
$\overline{ERR}$	Single error output flag, a low indicates at least a single bit error.
$\overline{MERR}$	Multiple error output flag, a low indicates two or more errors present.

PCC Pin Definitions DP8402A

pin 1	V_{CC}	pin 35	$O\overline{ECB}$
2	$\overline{LEDBO}$	36	CB3
3	$\overline{MERR}$	37	CB2
4	$\overline{ERR}$	38	CB1
5	DB0	39	CB0
6	DB1	40	DB16
7	DB2	41	DB17
8	NC	42	NC
9	NC	43	NC
10	NC	44	DB18
11	DB3	45	DB19
12	DB4	46	DB20
13	DB5	47	DB21
14	$\overline{OEBO}$	48	$\overline{OEB2}$
15	DB6	49	DB22
16	DB7	50	DB23
17	GND	51	GND
18	GND	52	GND
19	DB8	53	DB24
20	DB9	54	DB25
21	$O\overline{EB1}$	55	$\overline{OEB3}$
22	DB10	56	DB26
23	DB11	57	DB27
24	DB12	58	DB28
25	DB13	59	NC
26	DB14	60	NC
27	NC	61	NC
28	NC	62	NC
29	NC	63	DB29
30	DB15	64	DB30
31	NC	65	DB31
32	CB6	66	S0
33	CB5	67	S1
34	CB4	68	V_{CC}

TABLE I. Write Control Function

Memory Cycle	EDAC Function	Control S1	S0	Data I/O	DB Control $\overline{OEBn}$ or $\overline{OEDB}$	DB Output Latch DP8402A, DP8403 $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	$\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table II for details on check bit generation.

Memory Write Cycle Details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

TABLE II. Parity Algorithm

Check Word	32-Bit Data Word																													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X			X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X	X		X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by ''X'' for each bit.

Check bits 0, 1, 2 are odd parity or the exclusive NORing of the ''X''ed bits for the particular check bit. Check bits 3, 4, 5, 6 are even parity or the exclusive ORing of the ''X''ed bits for the particular check bit.

Memory Read Cycle (Error Detection & Correction Details)

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from the memory is acceptable to use as presented on the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table III represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE III. Error Function

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

The DP8402 check bit syndrome matrix can be seen in TABLE II. The horizontal rows of this matrix generate the check bits by selecting different combinations of data bits, indicated by ''X''s in the matrix, and generating parity from them. For instance, parity check bit ''0'' is generated by EXCLUSIVE NORing the following data bits together; 31, 29, 28, 26, 21, 19, 18, 17, 14, 11, 9, 8, 7, 6, 4, and 0. For example, the data word ''00000001H'' would generate the check bits CB6–0 = 48H (Check bits 0, 1, 2 are odd parity and check bits 3, 4, 5, 6 are even parity).

During a WRITE operation (mode 0) the data enters the DP8402 and check bits are generated at the check bit input/output port. Both the data word and the check bits are then written to memory.

During a READ operation (mode 2, error detection) the data and check bits that were stored in memory, now possibly in error, are input through the data and check bit I/O ports. New check bits are internally generated from the data word. These new check bits are then compared, by an EXCLUSIVE NOR operation, with the original check bits that were stored in memory. The EXCLUSIVE NOR of the original check bits, that were stored in memory, with the new check bits is called the syndrome word. If the original check bits are the same as the new check bits, a no error condition, then a syndrome word of all ones is produced and both error flags ($\overline{ERR}$ and $\overline{MERR}$) will be high. The DP8402 matrix encodes errors as follows:

TABLE IV. Read, Flag, and Correct Function

Memory Cycle	EDAC Function	Control S1	Control S0	Data I/O	DB Control $\overline{OEB}$n or $\overline{OEDB}$	DB Output Latch DP8402A, DP8403 $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†	
Read	Latch input data and check bits	H	H	Input data latched	H	L	Input check word latched	H	Enabled†	
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†	

†See Table III for error description.

‡See Table V for error location.

Memory Read Cycle (Error Detection & Correction Details) (Continued)

1) Single data bit errors cause 3 or 5 bits in the syndrome word to go low. The columns of the check bit syndrome matrix (TABLE II) are the syndrome words for all single bit data errors in the 32 bit word (also see TABLE V). The data bit in error corresponds to the column in the check bit syndrome matrix that matches the syndrome word. For instance, the syndrome word indicating that data bit 31 is in error would be (CB6-CB0) = ''0001010'', see the column for data bit 31 in TABLE II, or see TABLE V. During mode 3 (S0 = S1 = 1) the syndrome word is decoded, during single data bit errors, and used to invert the bit in error thus correcting the data word. The corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents the 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip.

2) A single check bit error will cause that particular check bit to go low in the syndrome word.

3) A double bit error will cause an even number of bits in the syndrome word to go low. The syndrome word will then be the EXCLUSIVE NOR of the two individual syndrome words corresponding to the 2 bits in error. The two-bit error is not correctable since the parity tree can only identify single bit errors.

If any of the bits in the syndrome word are low the ''$\overline{\text{ERR}}$'' flag goes low. The ''$\overline{\text{MERR}}$'' (dual error) flag goes low during any double bit error conditions. (See Table III).

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE V. Syndrome Decoding

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X

DB Y = error in data bit Y

2-bit = double-bit error

unc = uncorrectable multibit error

TABLE VI. Read-Modify-Write Function

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$ $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled
Read	Latch input data & check bits	H	H	Input data latched	H	L	Input check word latched	H	Enabled
Read	Latch corrected data word into output latch	H	H	Output data word latched	H	H	Hi-Z	H	Enabled
							Output Syndrome bits	L	
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H H
				Ouput unchanged BYTE0	L				

†$\overline{OEB}$0 controls DB_0–DB_7 (BYTE0), $\overline{OEB}$1 controls DB_8–DB_{15} (BYTE1), $\overline{OEB}$2 controls DB16–DB23 (BYTE2), $\overline{OEB}$3 controls DB24–DB31 (BYTE3).

Read-Modify-Write (Byte Control) Operations

The DP8402A and DP8403 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, SO = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{LEDBO}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{OEB}$0 through $\overline{OEB}$3 controls. $\overline{OEB}$0 controls DB0–DB7 (byte 0), $\overline{OEB}$1 controls DB8–DB15 (byte 1), $\overline{OEB}$2 controls DB16–DB23 (byte 2), and $\overline{OEB}$3 controls DB24–DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table VI lists the read-modify-write functions.

Diagnostic Operations

The DP8402A thru DP8405 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the DP8402A and DP8403, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the DP8404 and DP8405 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table VII DP8402A and DP8403 and Table VIII DP8404 and DP8405 list the diagnostic functions.

TABLE VII. DP8402A, DP8403 Diagnostic Function

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEB}n$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Input check bits latched	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Input diagnostic data word latched	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

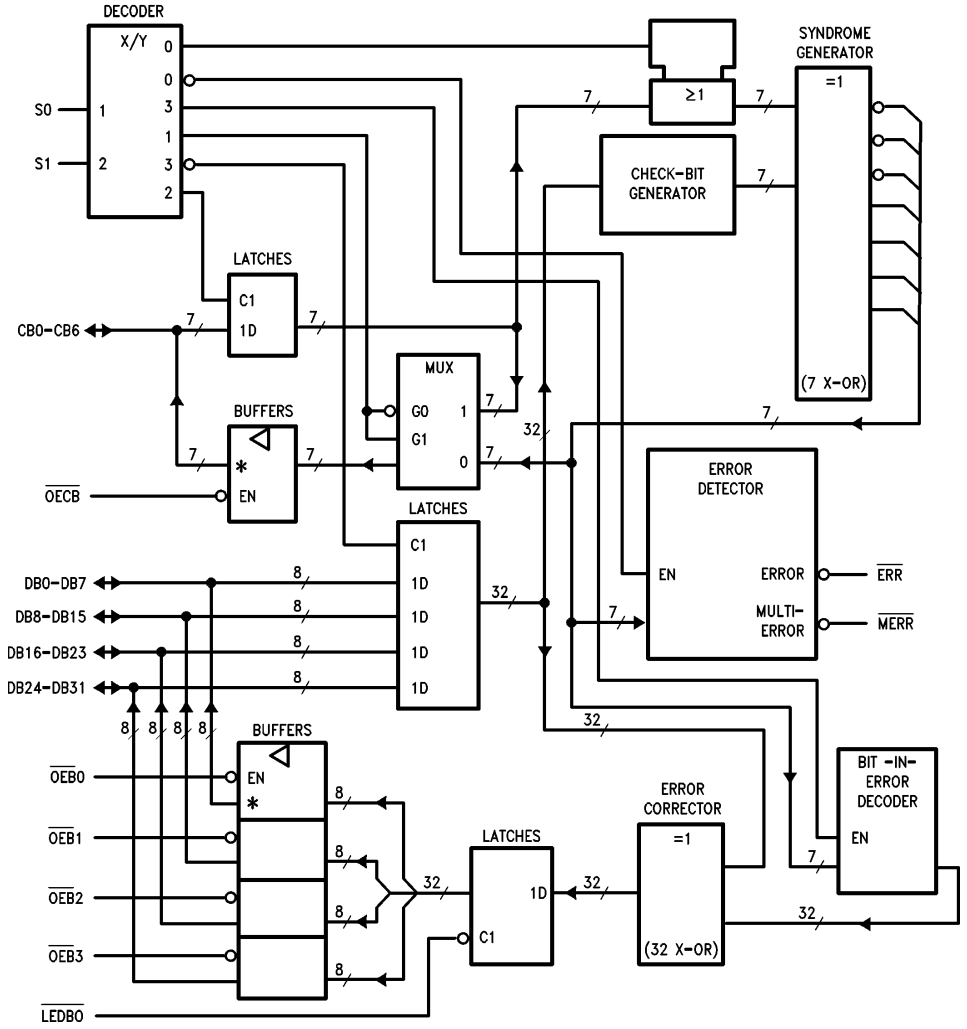
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE VIII. DP8404, DP8405 Diagnostic Function

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	DB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Input check bits latched	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Input diagnostic data word latched	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

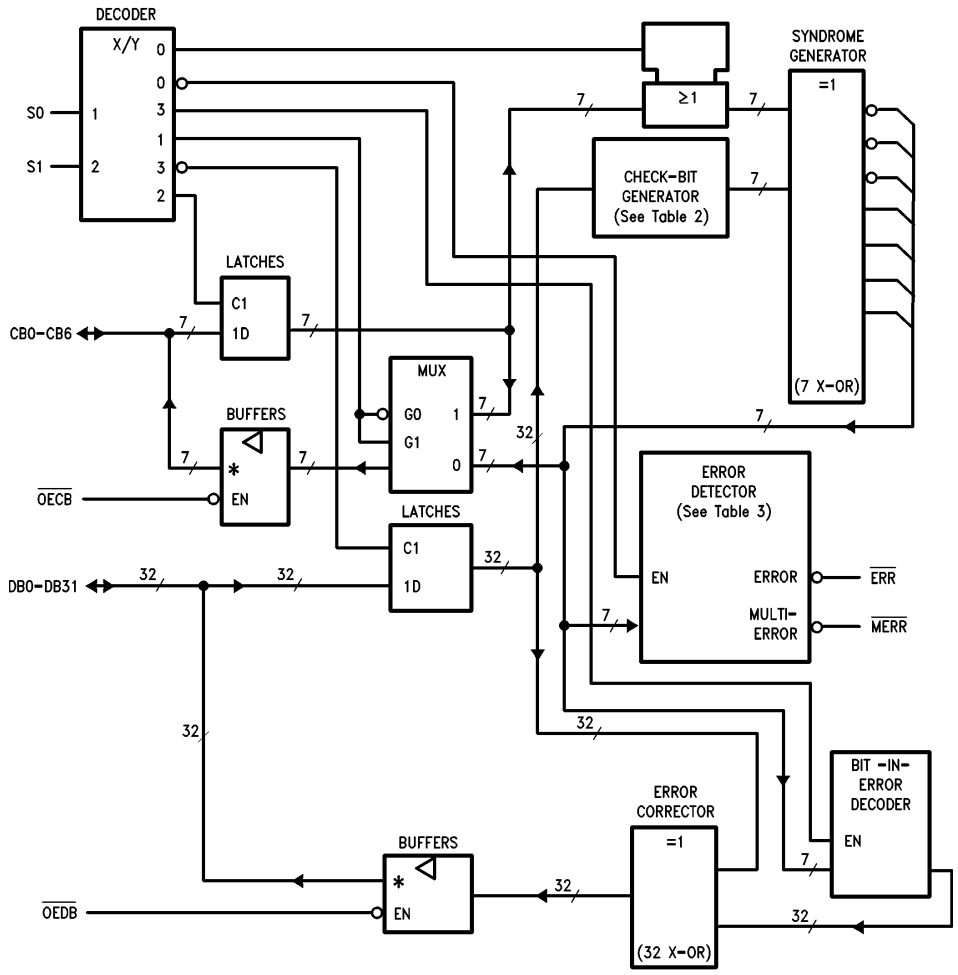
DP8402A, DP8403 Logic Diagram (Positive Logic)



DP8402A HAS TRI-STATE (▽) CHECK-BIT AND DATA OUTPUTS.
DP8403 HAS OPEN-COLLECTOR (◇) CHECK-BIT AND DATA OUTPUTS.

TL/F/8535–4

DP8404, DP8405 Logic Diagram (Positive Logic)



DP8404 HAS TRI-STATE (▽) CHECK-BIT AND DATA OUTPUTS.
DP8405 HAS OPEN-COLLECTOR (◇) CHECK-BIT AND DATA OUTPUTS.

TL/F/8535–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Over Operating Free-Air Temperature Range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) 7V

Input Voltage: CB and DB 5.5V

All Others 7V

Operating Free-Air Temperature: Military −55°C to +125°C

Commercial 0° to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current	$\overline{ERR}$ Or $\overline{MERR}$			−0.4			−0.4	mA
		DB Or CB DP8402A, DP8404			−1			−2.6	
I_{OL}	Low-Level Output Current	$\overline{ERR}$ Or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse Duration	$\overline{LEDBO}$ Low	25			25			ns
t_{su}	Setup Time	(1) Data And Check Word Before S0 ↑ (S1 = H)	15			10			ns
		(2) SO High Before $\overline{LEDBO}$ ↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ High Before The Earlier of S0 ↓ or S1 ↓ †	0			0			
		(4) $\overline{LEDBO}$ High Before S1 ↑ (S0 = H)	0			0			
		(5) Diagnostic Data Word Before S1 ↑ (S0 = H)	15			10			
		(6) Diagnostic Check Word Before The Later Of S1 ↓ or S0 ↑	15			10			
		(7) Diagnostic Data Word Before $\overline{LEDBO}$ ↑ (S1 = L and S0 = H)‡	25			20			
t_h	Hold Time	(8) Read-Mode, S0 Low And S1 High	35			30			ns
		(9) Data And Check Word After S0 ↑ (S1 = H)	20			15			
		(10) Data Word After S1 ↑ (S0 = H)	20			15			
		(11) Check Word After The Later of S1 ↓ or S0 ↑	20			15			
		(12) Diagnostic Data Word After $\overline{LEDBO}$ ↑ (S1 = L And S0 = H)‡	0			0			
t_{corr}	Correction Time (see *Figure 1*)*		65			58			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

*This specification may be interpreted as the maximum delay to guarantee valid corrected data at the output and includes the t_{su} setup delay.

†These times ensure that corrected data is saved in the output data latch.

‡These times ensure that the diagnostic data word is saved in the output data latch.

DP8402A, DP8404 Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ†	Max	Min	Typ†	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5V to 5.5V, I_{OH} = − 0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5V, I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5V, I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5V, I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
	All others	V_{CC} = 5.5V, V_I = 5.5V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
	All others‡				20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5V, V_I = 0.4V			−0.4			−0.4	mA
	All others‡				−0.1			−0.1	
I_O§		V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5V, (See Note 1)		150	250		150	250	mA

DP8403, DP8405 Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ†	Max	Min	Typ†	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5V, V_{OH} = 5.5V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5V, I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5V, V_I = 7V							mA
	All others	V_{CC} = 5.5V, V_I = 5.5V							
I_{IH}	S0 or S1	V_{CC} = 5.5V, V_I = 2.7V							μA
	All others‡								
I_{IL}	S0 or S1	V_{CC} = 5.5V, V_I = 0.4V							mA
	All others‡								
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5V, (See Note 1)		150			150		mA

†All typical values are at V_{CC} = 5V, T_A = +25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Note 1: I_{CC} is measured with S0 and S1 at 4.5V and all CB and DB pins grounded.

DP8402A Switching Characteristics

V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max (unless otherwise noted)

Symbol	From (Input)	To (Output)	Test Conditions	Military		Commercial		Units
				Min	Max	Min	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω	15	67	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500Ω	15	67	15	55	
t_{pd}	S0 ↓ and S1 ↓	CB	R1 = R2 = 500Ω	10	60	10	48	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω	10	60	10	48	ns
t_{pd}	$\overline{LEDB0}$ ↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω	7	35	7	30	ns
t_{pd}	S1 ↑	CB	S0 = H, R1 = R2 = 500Ω	10	60	10	50	ns
t_{en}	$\overline{OECB}$ ↓	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$ ↑	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↓	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↑	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns

DP8403 Switching Characteristics

V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max (unless otherwise noted)

Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R_L = 680Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680Ω		40			40		ns
t_{pd}	$\overline{LEDB0}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		26			26		ns
t_{pd}	S1 ↑	CB	S0 = H, R_L = 680Ω		40			40		ns
t_{PLH}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↑	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns

†All typical values are at V_{CC} = 5V, T_A = +25°C.

DP8404 Switching Characteristics, V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max

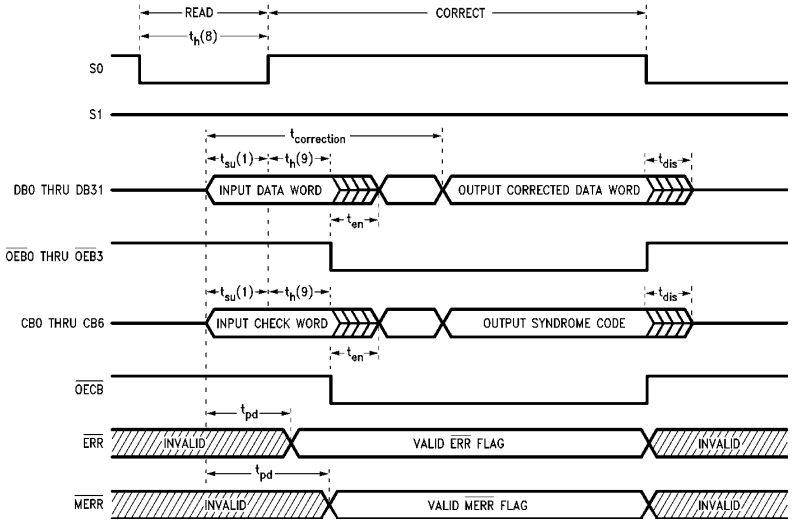
Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
			S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R1 = R2 = 500Ω		35			35		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω		35			35		ns
t_{pd}	S1 ↑	CB	S0 = H, R1 = R2 = 500Ω		35			35		ns
t_{en}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{dis}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{en}	$\overline{OECB}$ ↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{dis}	$\overline{OECB}$ ↑	DB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns

DP8405 Switching Characteristics, V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max

Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R_L = 680Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680Ω		40			40		ns
t_{pd}	S1 ↑	DB	S0 = H, R_L = 680Ω		40			40		ns
t_{PLH}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R_L = 500Ω		24			24		ns
t_{PHL}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$ ↑	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns

†All typical values are at V_{CC} = 5V, T_A = +25°C.

Switching Waveforms



TL/F/8535–6

FIGURE 1. Read, Flag, and Correct Mode

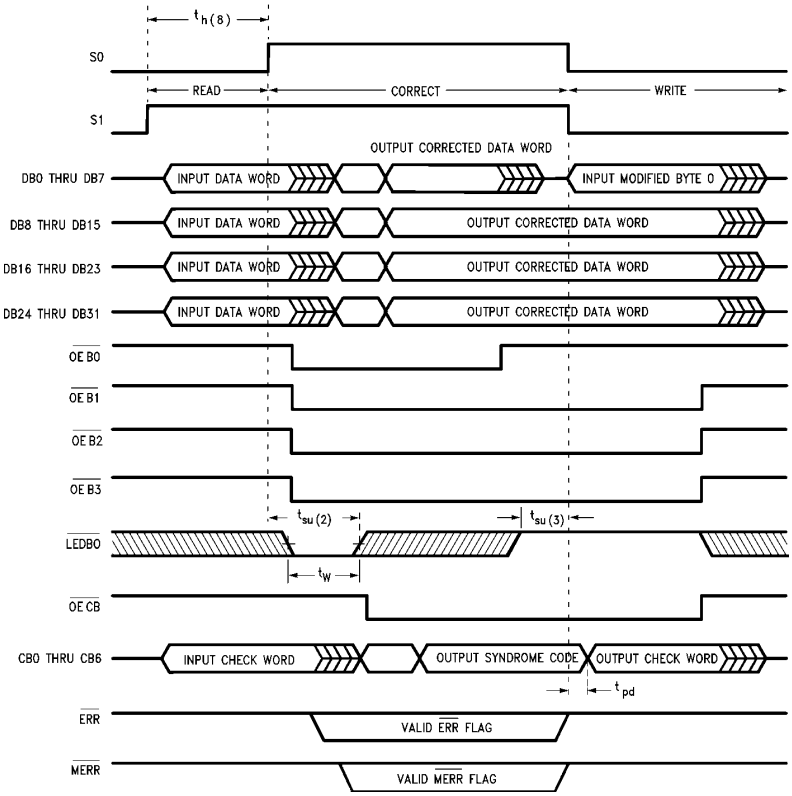


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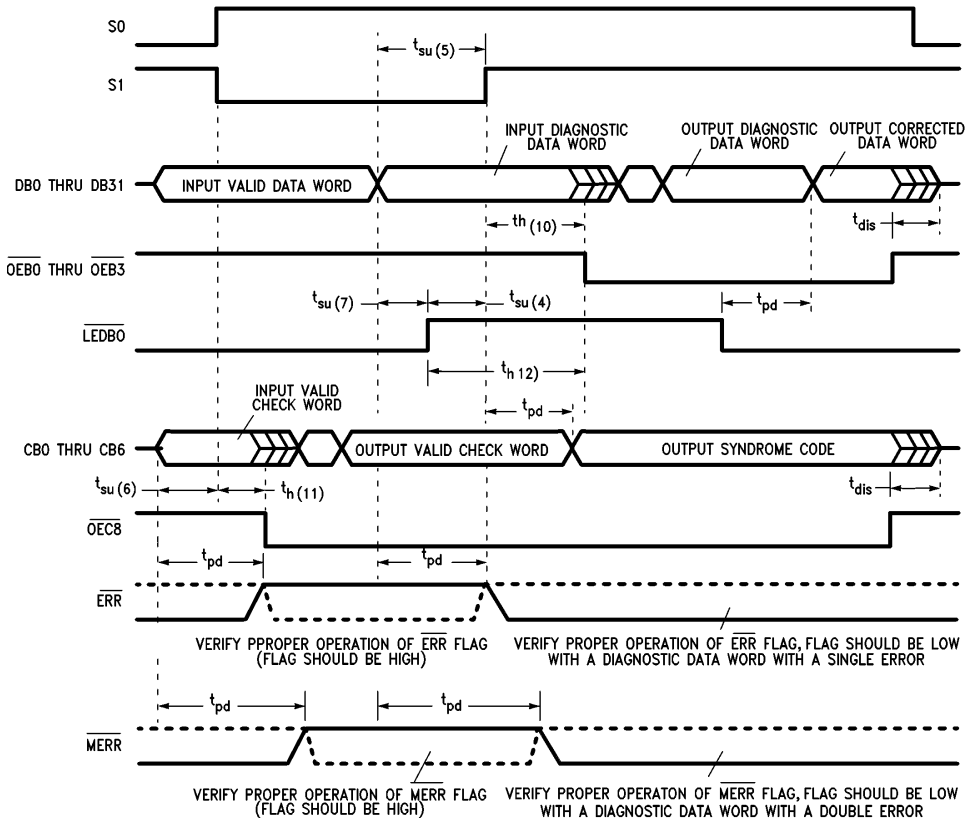
FIGURE 2. Read, Correct Modify Mode

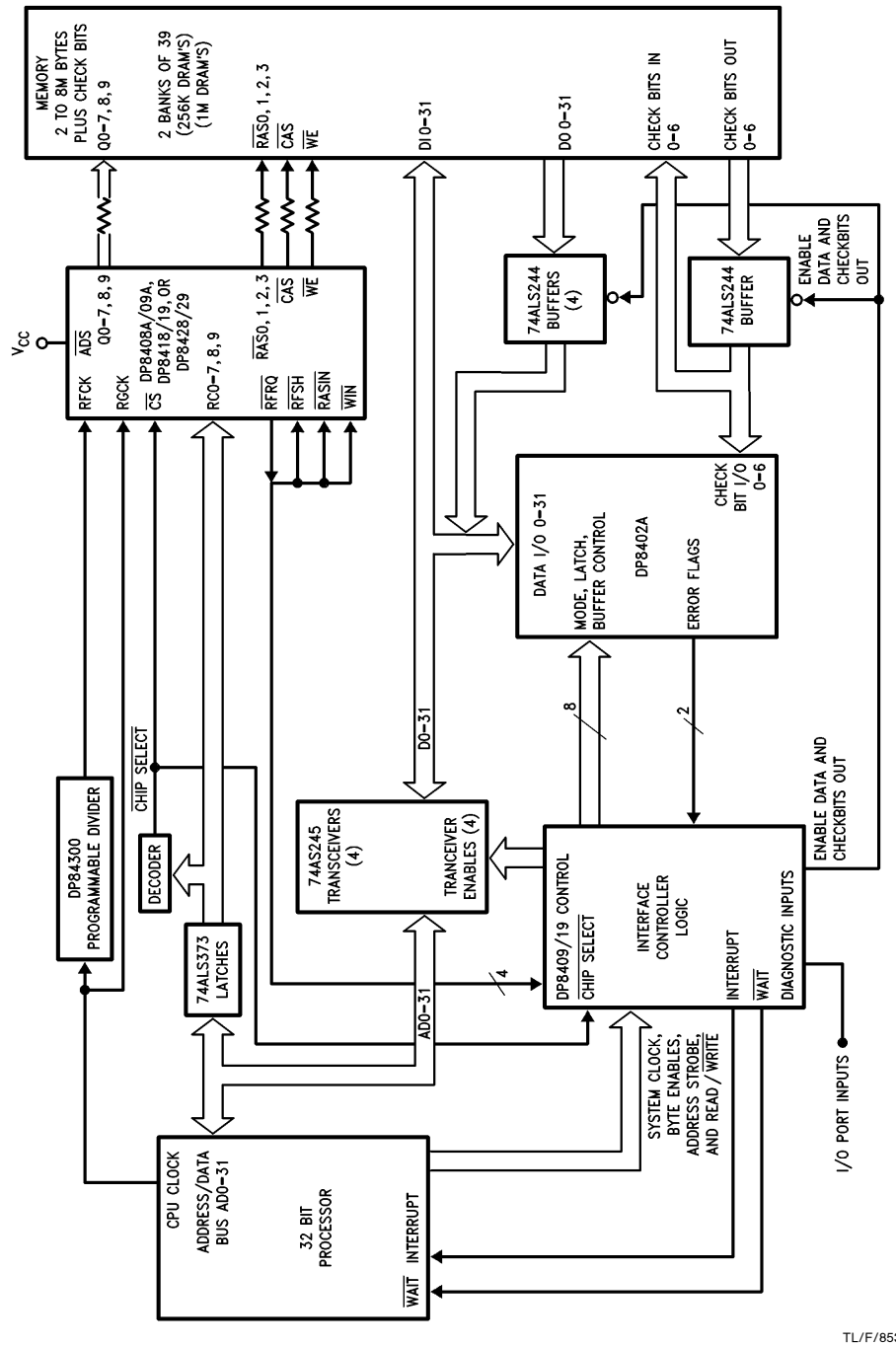
Switching Waveforms (Continued)



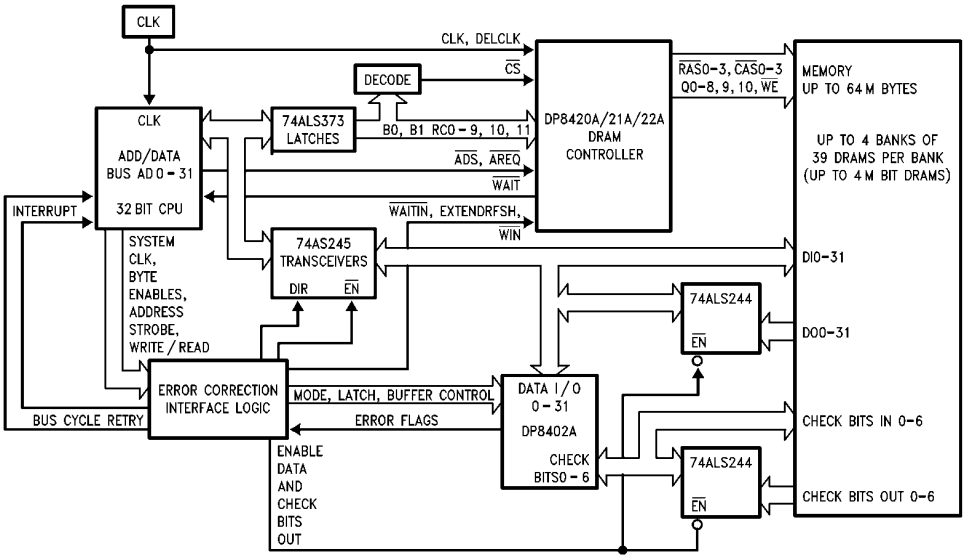
TL/F/8535–8

FIGURE 3. Diagnostic Mode

DP8402A Interfaced to the DP8418/19/28/29 System Diagram

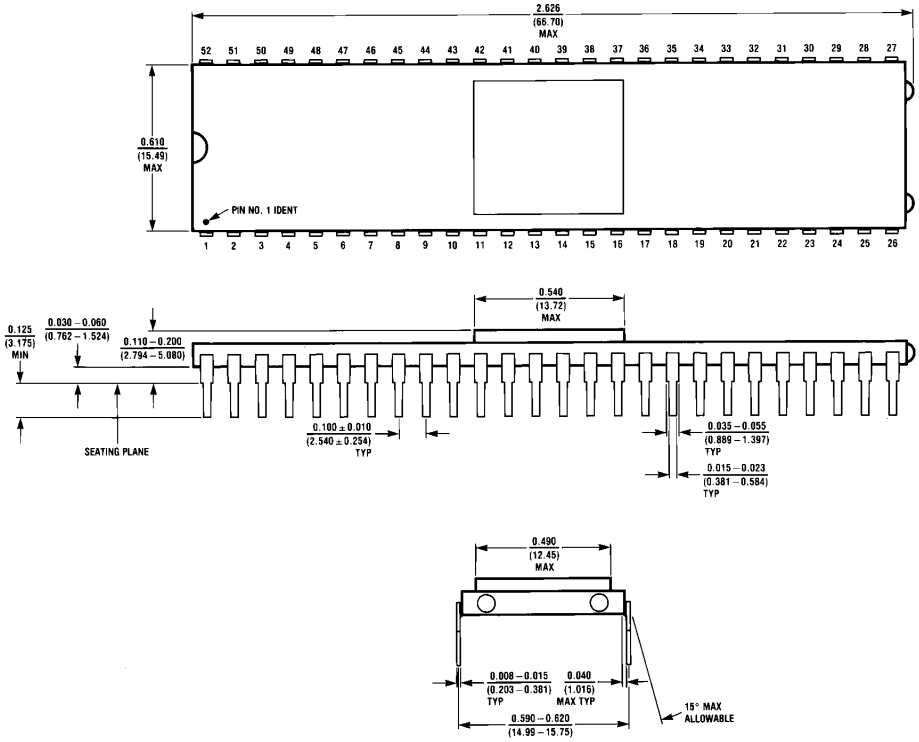


DP8402A Interfaced to the DP8420A/21A/22A System Diagram



TI/F/8535–12

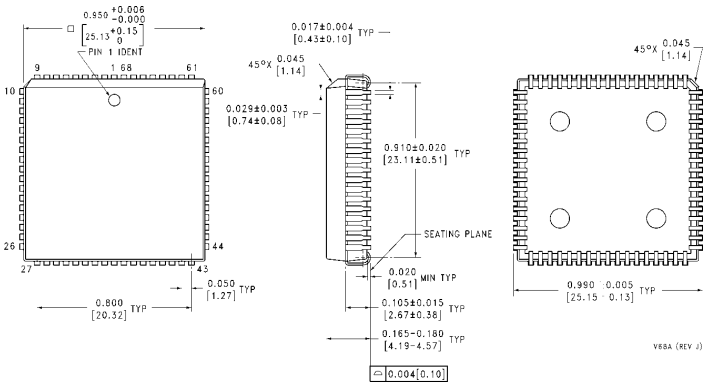
Physical Dimensions inches (millimeters)



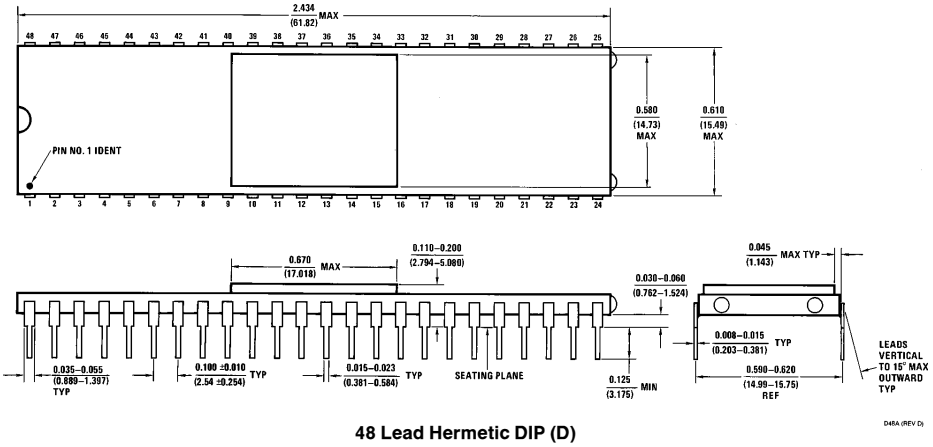
Hermetic Dual-In-Line (D)
Order Number DP8402AD or DP8403D
NS Package Number D52A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 103062



Plastic Chip Carrier (V)
Order Number DP8402AV
NS Package Number V68A



48 Lead Hermetic DIP (D)
Order Number DP8404D or DP8405D
NS Package Number D48A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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