National Semiconductor

ADVANCED INFORMATION

September 2003

DP83864 Quad GigPHYTER™ 10/100/1000 Ethernet Physical Layer

General Description

The DP83864 is an extremely efficient full featured Quad Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83864 contains four integrated ultra low power Gigabit Physical layers. It uses advanced 0.18 µm, 1.8 V CMOS technology, fabricated at National's South Portland, Maine facilities.

The DP83864 is designed for easy implementation of 10/100/1000 Mb/s Ethernet LANs. Each port interfaces directly to Twisted Pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII) or the IEEE 802.3z Gigabit Media Independent Interface (GMII). It also supports the reduced pin count RGMII (12 pins per port) and serial GMII (8 pins per port).

The DP83864 is a fourth generation of Gigabit Physical layer product with field proven architecture and performance. Its robust performance ensures drop in replacement of existing 10/100M equipment with 10/100/1000M Networking infrastructure.

Applications

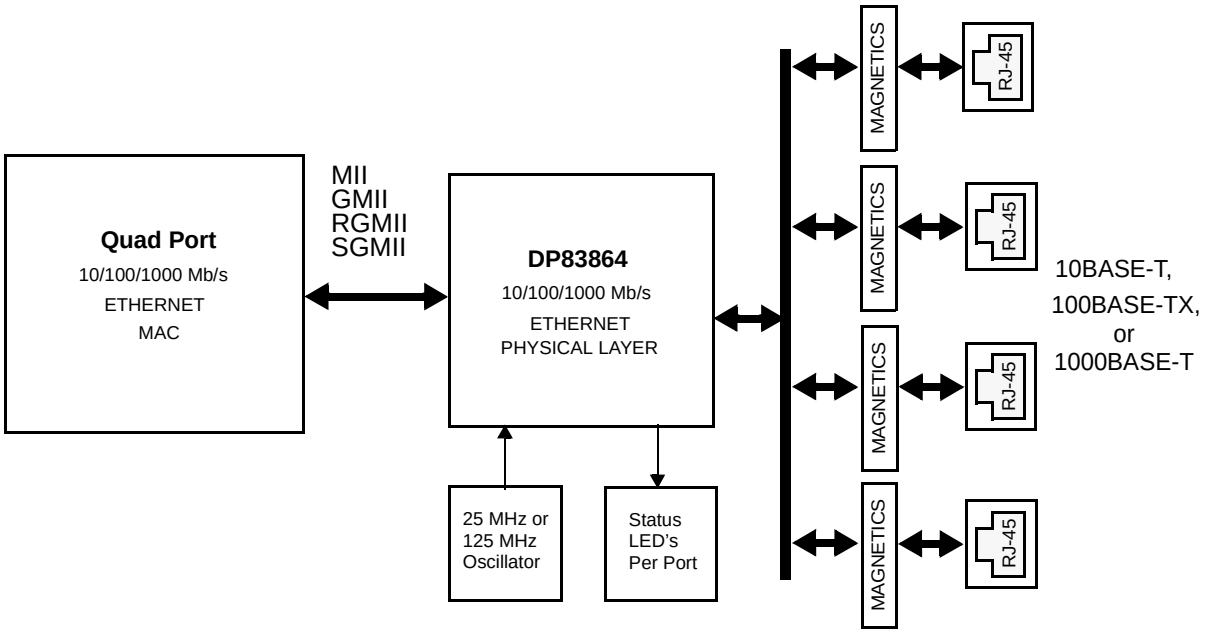
The DP83864 fits applications in:

- Switches with 10/100/1000 Mb/s capable ports
- High speed uplink ports with redundancies (backbone)
- Servers with Quad Ethernet ports

Features

- IEEE compliant 10BASE-T,100BASE-TX, 1000BASE-T
- Adaptive equalization and Baseline Wander comp.
- IEEE 802.3u Auto-Negotiation and Parallel Detection
  - Fully auto-negotiates between 1000 Mb/s, 100 Mb/s, and 10 Mb/s full duplex and half duplex devices
- 2.5 V/3.3 V MAC interfaces:
  - IEEE 802.3u MII with programmable bus ordering
  - IEEE 802.3z GMII with programmable bus ordering
  - Reduced GMII (RGMII) ver. 1.3
  - Serial GMII (SGMII)
- LED support (Link10, Link100, Link1000, Activity and Duplex indicators); Direct drive LED's thru management
- User Programmable Interrupt
- A 25Mhz or 125Mhz oscillator as reference clock input
- PHY level CRC checking on received packets and PHY level CRC generation for test mode transmit packets
- 292 BGA package
- Power dissipation approximately 1 W / port
- 1.8 V CMOS (core & analog); 2.5 V (analog & I/O); 3.3 V is optional for 3.3 V I/O voltage
- One management port per chip
- Supports Auto-MDIX/polarity at all speeds
- One JTAG interface per chip

System Diagram



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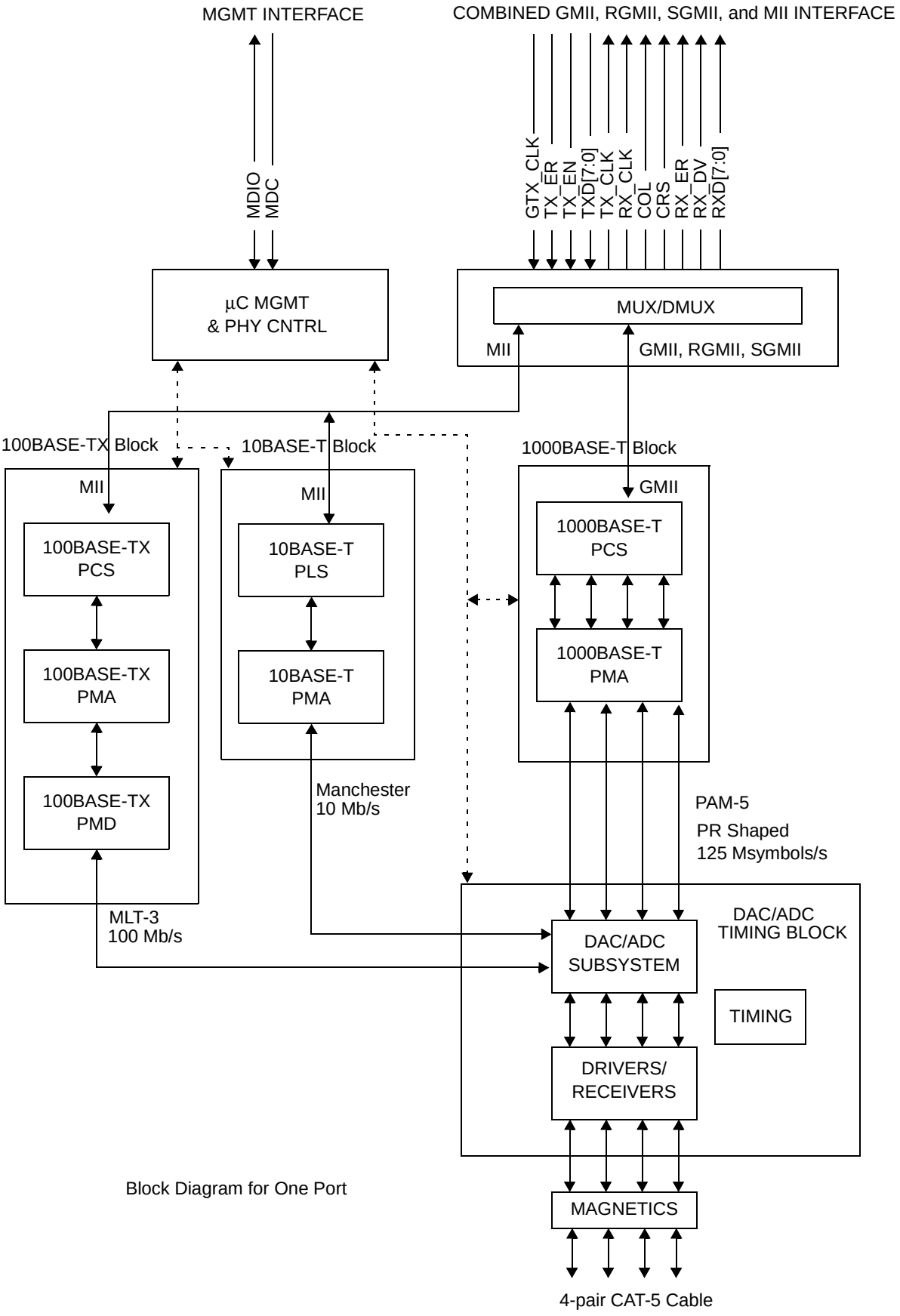
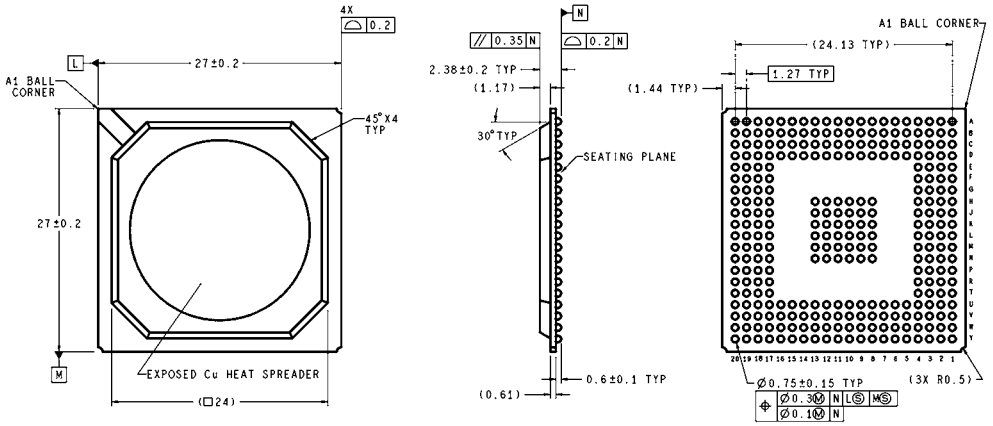
Block Diagram (Showing One Port)



Block Diagram for One Port

Notes:

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

UFH292A (Rev A)

NS Package BGA-292
Order Number DP83864AUT

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