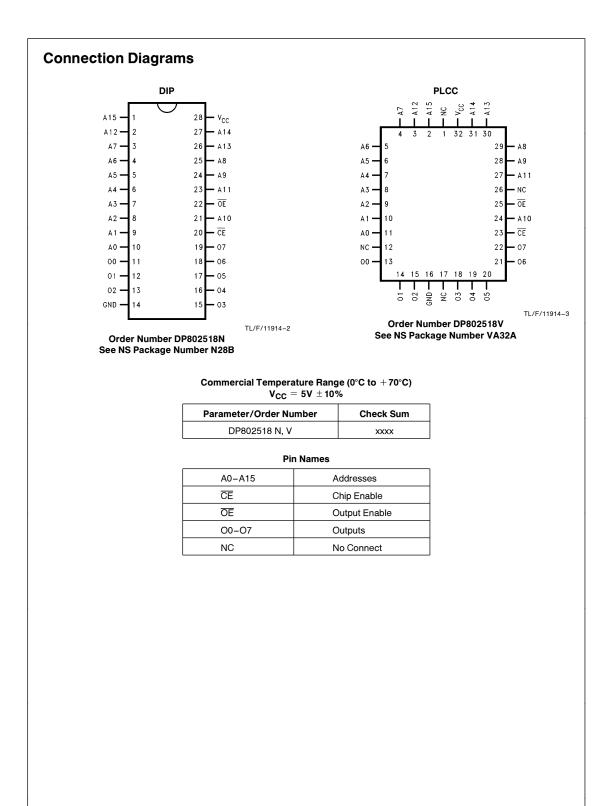


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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
All Input Voltages with Respect to Ground	-0.6V to +7V
V _{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V _{CC}	
Commercial	$0^{\circ}C$ to $+70^{\circ}C$	5V ±10%	

Read Operation

DC Electrical Characteristics Over operating range

Symbol	Parameter	Test Conditions	Min	Max	Units
V _{IL}	Input Low Level		-0.5	0.8	V
V _{IH}	Input High Level		2.0	$V_{CC} + 1$	V
V _{OL}	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
V _{OH}	Output High Voltage	$I_{OH} = -400 \ \mu A$	3.5		V
I _{SB1}	V _{CC} Standby Current (CMOS)	$\overline{\text{CE}} = \text{V}_{\text{CC}} \pm 0.3 \text{V}$		100	μΑ
I _{SB2}	V _{CC} Standby Current	$\overline{CE} = V_{H}$		1	mA
Icc	V _{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA		40	mA
ILI	Input Load Current	$V_{IN} = 5.5V \text{ or GND}$	-1	1	μΑ
ILO	Output Leakage Current	$V_{OUT} = 5.5V, OR GND$	-10	10	μΑ

AC Electrical Characteristics Over operating range

Symbol	Parameter	Min	Max	Units
t _{ACC}	Address to Output Delay		120	
t _{CE}	CE to Output Delay		120	
t _{OE}	OE to Output Delay		50	ns
t _{DF} (Note 2)	Output Disable to Output Float		25	
t _{OH} (Note 2)	Output Hold From Addresses, CE or OE, Whichever Occurred First	7		

$\label{eq:capacitance} \textbf{Capacitance} \ \textbf{T}_{A} = \ + \ \textbf{25^{\circ}C}, \ \textbf{1} = \ \textbf{1} \ \textbf{MHz} \ \textbf{(Note 2)}$

Symbol	Parameter	Conditions	Тур	Max	Units
C _{IN}	Input Capacitance	$V_{IN} = 0V$	13	20	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load

Input Rise and Fall Time

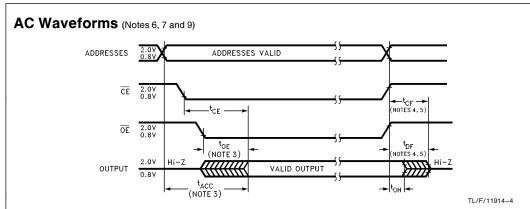
1 TTL Gate and	
C _L = 100 pF (Note 8)	
\leq 5 ns	

 Input Pulse Levels
 0.45V to 2.4V

 Timing Measurement Level (Note 8)
 (Note 8)

 Inputs
 0.8V and 2V

 Outputs
 0.8V and 2V



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3 \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impacting t_{ACC} .

Note 4: The t_{DF} and t_{CF} compare level is determined as follows

High to TRI-STATE®, the measure V_{CH1} (DC) - 0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) \pm 0.10V.

Note 5: TRI-STATE may be attained using \overline{OE} or \overline{CE} .

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.2 μ F ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC}\,+\,$ 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = $-400~\mu A.$

CL: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to $\,-2.0V$ for 20 ns max.

Functional Description

DEVICE OPERATION

The three modes of operation of the Tsunami are listed in Table I. It should be noted that all inputs of the three modes are at TTL levels. The power supply required is supplied via the V_{CC} pin and the power supply tolerance should be 5V \pm 10%.

Read Mode

The Tsunami has two control functions, both of which must be logically active to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}) . Data is available at the outputs t_{OE} after the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Tsunami has a standby mode which reduces the active power dissipation drastically, from 275 mW to 0.55 mW. The DP802518 is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output Disable

The DP802518 is placed in output disable by applying a TTL high signal to the \overline{OE} input. When in output disable, all circuitry is enabled except the outputs are in a high impedance state (TRI-STATE).

APPLICATION

In application, the DP802518 is connected to the DP80253 TROPIC II high performance token ring controllers as shown in *Figure 1*. The DP802518 is connected to the TROPIC II with outputs O0 to O7 connected to L_D0-L_ D7 respectively.

SYSTEM CONSIDERATION

The power switching characteristics of Tsunami require careful decoupling of the devices. The supply current $I_{\rm CC}$ has three segments that are of interest to the system designer: The standby current level, the active current level, and the transient current peaks that are produced by the voltage transition on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selecting decoupling capacitors. It is recommended that a 0.2 μ F ceramic capacitor be used between V_{CC} and GND for each of the eight devices. The bulk capacitor should be located near the point where the power supply is connected to the subsystem. The bulk capacitor is used to overcome the voltage drop caused by the inductive effects of the PC board traces.

