National Semiconductor

March 2001

# CLC450
# Single Supply, Low Power, High Output, Current Feedback Amplifier

## General Description

The CLC450 has a new output stage that delivers high output drive current (100mA), but consumes minimal quiescent supply current (1.5mA) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear phase response up to one half of the -3dB frequency.

The CLC450 offers superior dynamic performance with a 100MHz small signal bandwidth, 280V/µs slew rate and 6.1ns rise/fall times ($2V_{STEP}$). The combination of low quiescent power, high output current drive, and high speed performance make the CLC450 well suited for many battery powered personal communication/computing systems.

The ability to drive low impedance, highly capacitive loads, makes the CLC450 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC450 will drive a 100Ω load with only −75/−64dBc second/third harmonic distortion ($A_V$ =+2, $V_{OUT}$ = $2V_{PP}$, f = 1MHz). With a 25Ω load, and the same conditions, it produces only −70/−60dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high resolution A/D converters, the CLC450 provides excellent −79/−75dBc second/third harmonic distortion ($A_V$= +2, $V_{OUT}$ = $2V_{PP}$, f = 1MHz, $R_L$ = 1kΩ) and fast settling time.

Available in SOT23-5, the CLC450 is ideal for applications where space is critical.

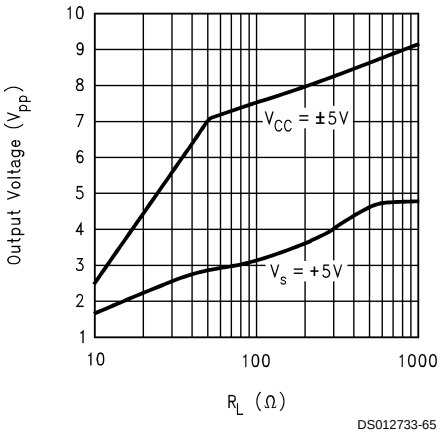
## Features

- 100mA output current
- 1.5mA supply current
- 100MHz bandwidth ($A_V$ = +2)
- −79/−75dBc HD2/HD3 (1MHz)
- 20ns settling to 0.05%
- 280V/µs slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V to ±5V supplies
- Available in Tiny SOT23-5 package

## Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery powered applications
- A/D driver

**Maximum Output Voltage vs. $R_L$**

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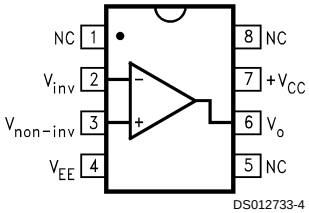
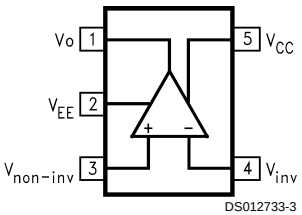
## Connection Diagrams




DS012733-4

**Pinout**
**DIP & SOIC**

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**Pinout**
**SOT23-5**

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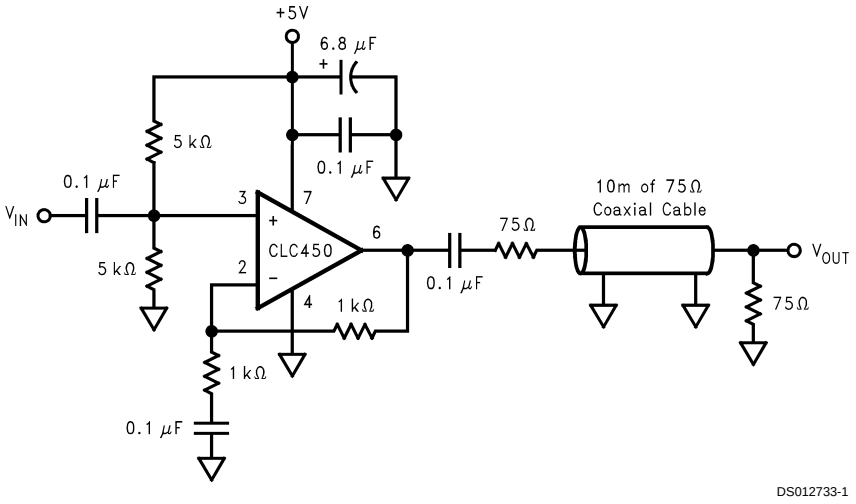
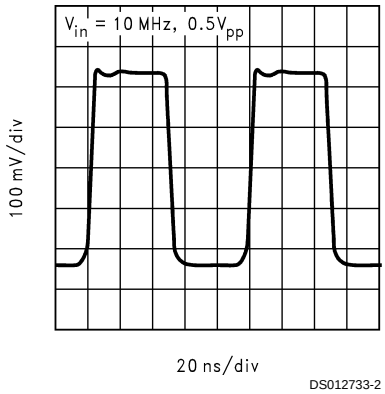
## Typical Application




**Single Supply Cable Driver**




**Response After 10m of Cable**

## Ordering Information

| Package | Temperature Range Industrial | Part Number | Package Marking | NSC Drawing |
|---|---|---|---|---|
| 8-pin plastic DIP | −40˚C to +85˚C | CLC450AJP | CLC450AJP | N08E |
| 8-pin plastic SOIC | −40˚C to +85˚C | CLC450AJE | CLC450AJE | M08A |
| 5-pin SOT | −40˚C to +85˚C | CLC450AJM5 | A20 | MA05A |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$ - $V_{EE}$) | +14V |
| Output Current (see note 3) | 140mA |
| Common Mode Input Voltage | $V_{EE}$ to $V_{CC}$ |
| Maximum Junction Temperature | +150˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Solder Duration (+300˚C) | 10 sec |
| ESD Rating (human body model) | 500V |

## Operating Ratings

Thermal Resistance

| Package | ($\theta_{JC}$) | ($\theta_{JA}$) |
|---|---|---|
| MDIP | 115˚C/W | 125˚C/W |
| SOIC | 130˚C/W | 150˚C/W |
| SOT23 | 140˚C/W | 210˚C/W |

## +5V Electrical Characteristics

$A_V$ = +2, $R_f$ = 1k, $R_L$ = 100Ω, $V_S$ = +5 (Note 4), $V_{CM}$ = $V_{EE}$ + ($V_S$/2), $R_L$ tied to $V_{CM}$; unless specified

| Symbol | Parameter | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|
| Ambient Temperature | | CLC450AJ | +25˚C | +25˚C | 0 to 70˚C | −40 to 85˚C | |
| **Frequency Domain Response** | | | | | | | |
| | -3dB Bandwidth | $V_O$ <0.5$V_{PP}$ | 100 | 85 | 75 | 70 | MHz |
| | | $V_O$ <2.0$V_{PP}$ | 75 | 60 | 55 | 50 | MHz |
| | −0.1dB Bandwidth | $V_O$ <0.5$V_{PP}$ | 30 | 25 | 20 | 20 | MHz |
| | Gain Ppeaking | <200MHz, $V_O$ <0.5$V_{PP}$ | 0 | 0.5 | 0.9 | 1.0 | dB |
| | Gain Rolloff | <30MHz, $V_O$ <0.5$V_{PP}$ | 0.1 | 0.3 | 0.4 | 0.5 | dB |
| | Linear Phase Deviation | <30MHz, $V_O$ = 0.5$V_{PP}$ | 0.2 | 0.4 | 0.5 | 0.5 | deg |
| **TIME DOMAIN RESPONSE** | | | | | | | |
| | Rise and Fall Time | 2V Step | 6.1 | 8.5 | 9.2 | 10.0 | ns |
| | Settling Time to 0.05% | 1V Step | 20 | 30 | 50 | 80 | ns |
| | Overshoot | 2V Step | 16 | 20 | 22 | 22 | % |
| | Slew Rate | 2V Step | 280 | 200 | 185 | 170 | V/µs |
| **DISTORTION AND NOISE RESPONSE** | | | | | | | |
| | 2nd Harmonic Distortion | 2$V_{PP}$,1MHz | −75 | - | - | - | dBc |
| | | 2$V_{PP}$, 1MHz, $R_L$ = 1kΩ | −79 | - | - | - | dBc |
| | | 2$V_{PP}$, 5MHz | −62 | -58 | -57 | -56 | dBc |
| | 3rd Harmonic Distortion | 2$V_{PP}$, 1MHz | −64 | - | - | - | dBc |
| | | 2$V_{PP}$, 1MHz, $R_L$ = 1kΩ | −75 | - | - | - | dBc |
| | | 2$V_{PP}$, 5MHz | −52 | -48 | -46 | -46 | dBc |
| | Equivalent Input Noise | | | | | | |
| | Voltage ($e_{ni}$) | >1MHz | 3.0 | 3.7 | 4.0 | 4.0 | nV/$\sqrt{Hz}$ |
| | Non-Inverting Current ($i_{bn}$) | >1MHz | 6.9 | 9 | 10 | 10 | pA/$\sqrt{Hz}$ |
| | Inverting Current ($i_{bi}$) | >1MHz | 8.5 | 11 | 12 | 12 | pA/$\sqrt{Hz}$ |
| **Static, DC Performance** | | | | | | | |
| | Input Offset Voltage (Note 5) | | 1 | 4 | 5 | 6 | mV |
| | Average Drift | | 7 | - | 15 | 15 | µV/˚C |
| | Input Bias Current (Non-Inverting) (Note 5) | | 5 | 12 | 15 | 16 | µA |
| | Average Drift | | 25 | - | 60 | 60 | nA/˚C |
| | Input Bias Current (Inverting) (Note 5) | | 3 | 10 | 12 | 13 | µA |
| | Average Drift | | 10 | - | 20 | 20 | nA/˚C |
| | Power Supply Rejection Ratio | DC | 54 | 50 | 48 | 48 | dB |
| | Common Mode Rejection Ratio | DC | 51 | 47 | 45 | 45 | dB |

## +5V Electrical Characteristics (Continued)

$A_V$ = +2, $R_f$ = 1k, $R_L$ = 100Ω, $V_S$ = +5 (Note 4), $V_{CM}$ = $V_{EE}$ + ($V_S$/2), $R_L$ tied to $V_{CM}$; unless specified

| Symbol | Parameter | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|
| **Static, DC Performance** | | | | | | | |
| | Supply Current (Note 5) | $R_L$ = ∞ | 1.5 | 1.7 | 1.8 | 1.8 | mA |
| **Miscellaneous Performance** | | | | | | | |
| | Input Resistance (Non-Inverting) | | 0.46 | 0.37 | 0.33 | 0.33 | MΩ |
| | Input Capacitance (Non-Inverting) | | 1.5 | 2.3 | 2.3 | 2.3 | pF |
| | Input Voltage Range, High | | 4.2 | 4.1 | 4.1 | 4.0 | V |
| | Input Voltage Range, Low | | 0.8 | 0.9 | 0.9 | 1.0 | V |
| | Output Voltage Range, High | $R_L$ = 100Ω | 4.0 | 3.9 | 3.9 | 3.8 | V |
| | Output Voltage Range, Low | $R_L$ = 100Ω | 1.0 | 1.1 | 1.1 | 1.2 | V |
| | Output Voltage Range, High | $R_L$ = ∞ | 4.1 | 4.0 | 4.0 | 3.9 | V |
| | Output Coltage Range, Low | $R_L$ = ∞ | 0.9 | 1.0 | 1.0 | 1.1 | V |
| | Output Current (Note 3) | | 100 | 80 | 65 | 40 | mA |
| | Output Resistance, Closed Loop | DC | 55 | 90 | 90 | 120 | mΩ |

## ± 5V Electrical Characteristics

$A_V$ = +2, $V_{CC}$ = ±5V, $R_L$ = 100Ω, $R_f$ = 1kΩ; unless specified

| Symbol | Parameterm | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|
| Ambient Temperature | | CLC450AJ | +25˚C | +25˚C | 0 to 70˚C | −40 to 85˚C | |
| **Frequency Domain Response** | | | | | | | |
| | -3dB Bandwidth | $V_O$ <1.0$V_{PP}$ | 135 | 115 | 105 | 100 | MHz |
| | | $V_O$ <4.0$V_{PP}$ | 55 | 45 | 42 | 40 | MHz |
| | −0.1dB Bandwidth | $V_O$ <1.0$V_{PP}$ | 40 | 30 | 25 | 25 | MHz |
| | Gain Peaking | <200MHz, $V_O$ <1.0$V_{PP}$ | 0 | 0.5 | 0.9 | 1.0 | dB |
| | Gain Rolloff | <30MHz, $V_O$ <1.0$V_{PP}$ | 0.1 | 0.3 | 0.4 | 0.5 | dB |
| | Linear Phase Deviation | <30MHz, $V_O$ <1.0$V_{PP}$) | 0.1 | 0.3 | 0.4 | 0.4 | deg |
| | Differential Gain | NTSC, $R_L$ = 150Ω | 0.03 | - | - | - | % |
| | Differential Phase | NTSC, $R_L$ = 150Ω | 0.3 | - | - | - | deg |
| **TIME DOMAIN RESPONSE** | | | | | | | |
| | Rise and Fall Time | 2V Step | 4.4 | 5.8 | 6.2 | 6.8 | ns |
| | Settling Time to ±0.05% | 2V Step | 15 | 25 | 40 | 60 | ns |
| | Overshoot | 2V Step | 15 | 20 | 22 | 22 | % |
| | Slew Rate | 2V Step | 370 | 280 | 260 | 240 | V/µs |
| **DISTORTION AND NOISE RESPONSE** | | | | | | | |
| | 2nd Harmonic Distortion | $2V_{PP}$, 1MHz | −86 | - | - | - | dBc |
| | | $2V_{PP}$, 1MHz, $R_L$ = 1kΩ | −85 | - | - | - | dBc |
| | | $2V_{PP}$, 5MHz | −68 | −64 | −61 | −60 | dBc |
| | 3rd Harmonic Distortion | $2V_{PP}$, 1MHz | −65 | - | - | - | dBc |
| | | $2V_{PP}$, 1MHz, $R_L$ = 1kΩ | −74 | - | - | - | dBc |
| | | $2V_{PP}$, 5MHz | −52 | −48 | −46 | −46 | dBc |
| | Equivalent Input Noise | | | | | | |
| | Voltage ($e_{ni}$) | >1MHz | 3.0 | 3.7 | 4.0 | 4.0 | nV/$\sqrt{Hz}$ |
| | Non-Inverting Current ($i_{bn}$) | >1MHz | 6.9 | 9 | 10 | 10 | pA/$\sqrt{Hz}$ |
| | Inverting Current ($i_{bi}$) | >1MHz | 8.5 | 11 | 12 | 12 | pA/$\sqrt{Hz}$ |

## ± 5V Electrical Characteristics (Continued)

$A_V$ = +2, $V_{CC}$ = ±5V, $R_L$ = 100Ω, $R_f$ = 1kΩ; unless specified

| Symbol | Parameterm | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|
| **Static, DC Performance** | | | | | | | |
| | Input Offset Voltage | | 2 | 6 | 7 | 8 | mV |
| | Average Drift | | 8 | - | 20 | 20 | µV/˚C |
| | Input Bias Current (Non-Inverting) | | 5 | 12 | 16 | 17 | µA |
| | Average Drift | | 40 | - | 70 | 70 | nA/˚C |
| | Input Bias Current (Inverting) | | 5 | 13 | 15 | 16 | µA |
| | Average Drift | | 20 | - | 45 | 45 | nA/˚C |
| | Power Supply Rejection Ratio | DC | 56 | 51 | 49 | 49 | dB |
| | Common-Mode Rejection Ratio | DC | 53 | 48 | 46 | 46 | dB |
| | Supply Current | $R_L$ = ∞ | 1.6 | 1.9 | 2.0 | 2.0 | mA |
| **Miscellaneous Performance** | | | | | | | |
| | Input Resistance (Non-Inverting) | | 0.62 | 0.50 | 0.45 | 0.45 | MΩ |
| | Input Capacitance (Non-Inverting) | | 1.2 | 1.8 | 1.8 | 1.8 | pF |
| | Common-Mode Input Range | | ±4.2 | ±4.1 | ±4.1 | ±4.0 | V |
| | Output Voltage Range | $R_L$ = 100Ω | ±3.8 | ±3.6 | ±3.6 | ±3.5 | V |
| | Output Voltage Range | $R_L$ = ∞ | ±4.0 | ±3.8 | ±3.8 | ±3.7 | V |
| | Output Current (Note 3) | | 130 | 100 | 80 | 50 | mA |
| | Output Resistance, Closed Loop | DC | 40 | 70 | 70 | 90 | mΩ |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

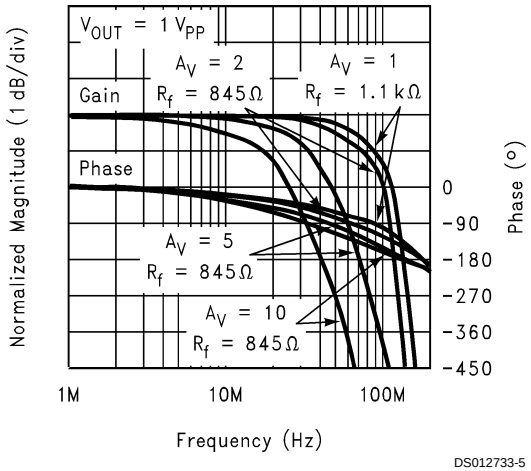
**Note 3:** The short circuit current can exceed the maximum safe output current.

**Note 4:** $V_S = V_{CC} - V_{EE}$

**Note 5:** AJ-level: spec. is 100% tested at +25˚C.

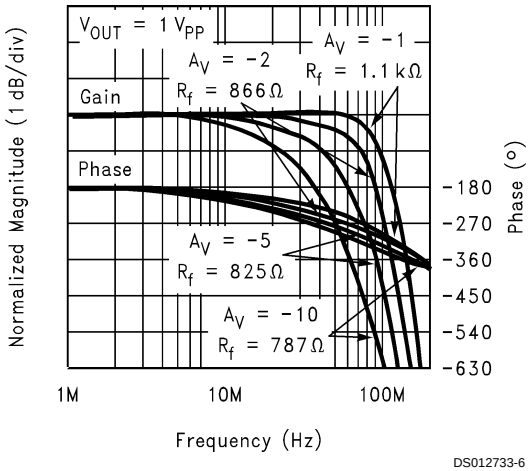
## +5V Typical Performance Characteristics

**Non-Inverting Frequency Response**




DS012733-5

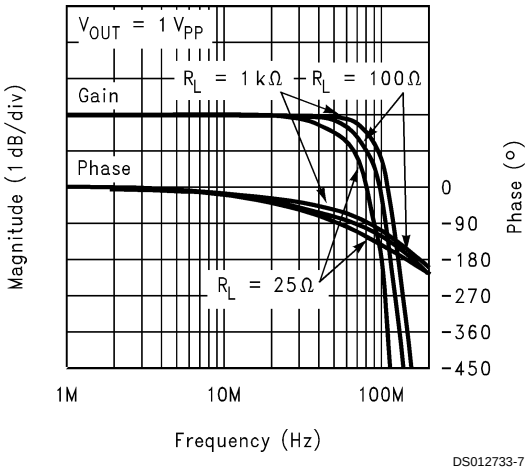
**Inverting Frequency Response**




DS012733-6

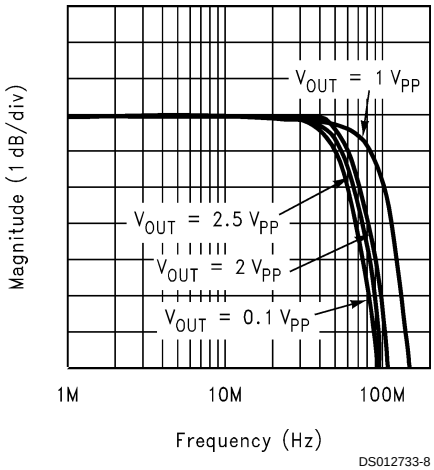
## +5V Typical Performance Characteristics (Continued)

**Frequency Response vs. $R_L$**



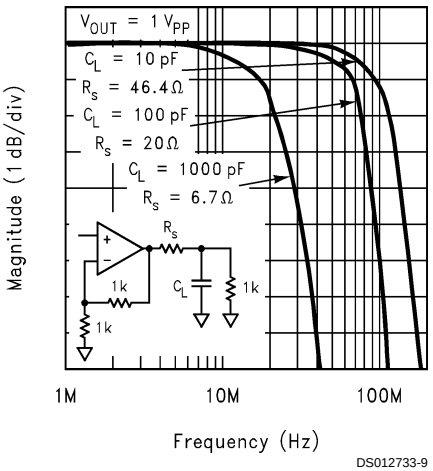

DS012733-7

**Frequency Response vs. $V_O$**



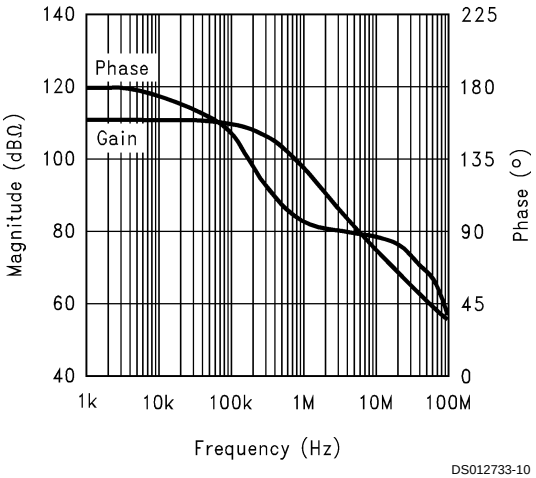

DS012733-8

**Frequency Response vs. $C_L$**



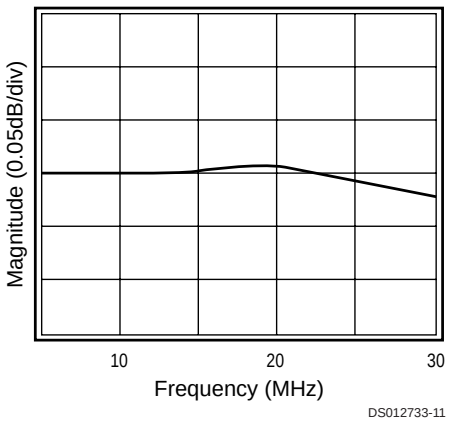

DS012733-9

**Open Loop Transimpedance Gain, Z(s)**



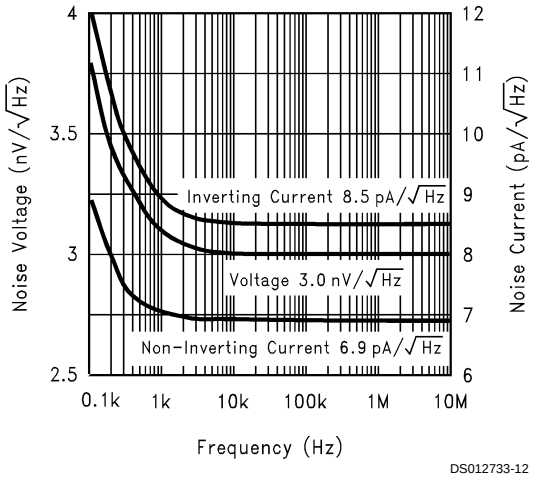

DS012733-10

**Gain Flatness**




DS012733-11

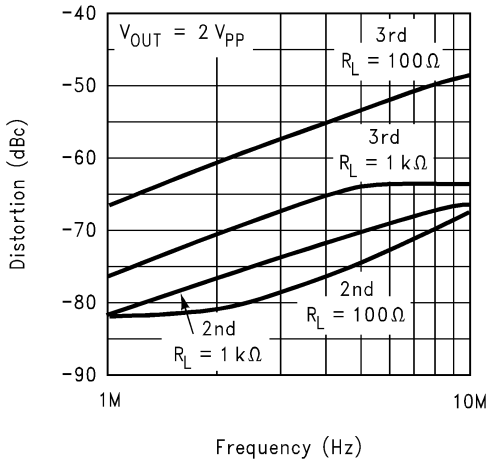
**Equivalent Input Noise**




DS012733-12

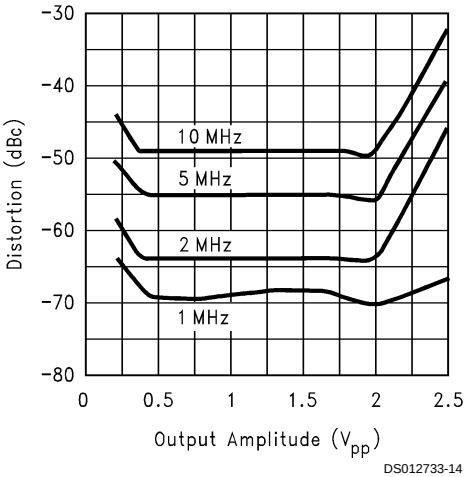
## +5V Typical Performance Characteristics (Continued)

**2nd & 3rd Harmonic Distortion**



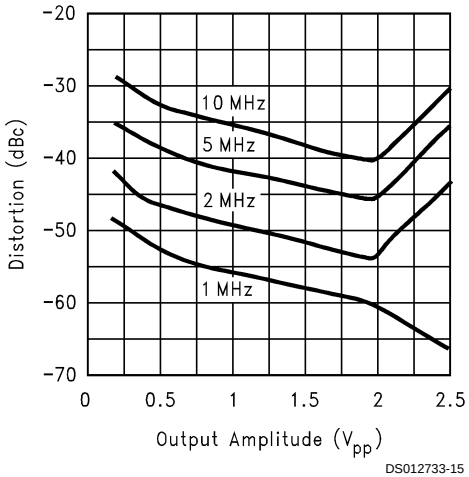

DS012733-13

**2nd Harmonic Distortion, $R_L$ = 25Ω**



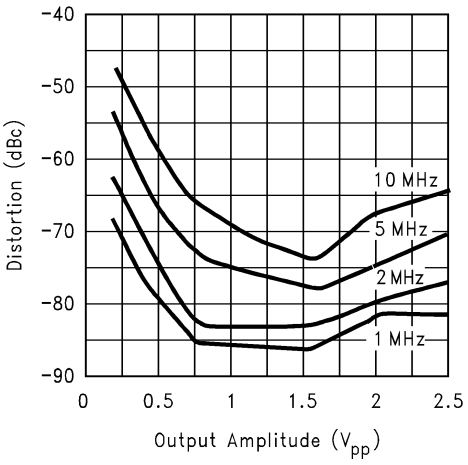

DS012733-14

**3rd Harmonic Distortion, $R_L$ = 25Ω**



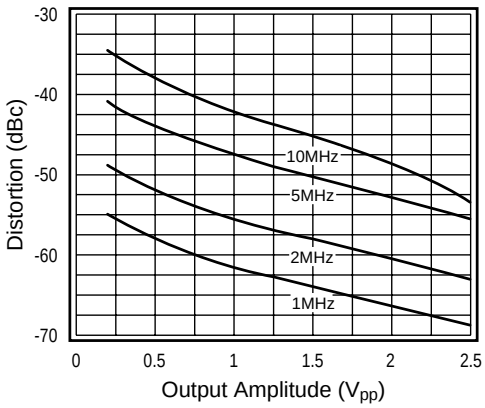

DS012733-15

**2nd Harmonic Distortion, $R_L$ = 100Ω**



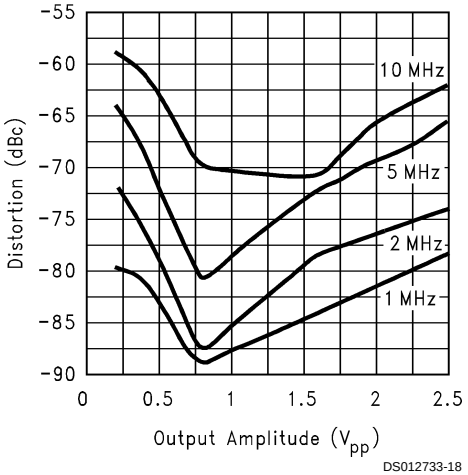

DS012733-16

**3rd Harmonic Distortion, $R_L$ = 100Ω**




DS012733-17

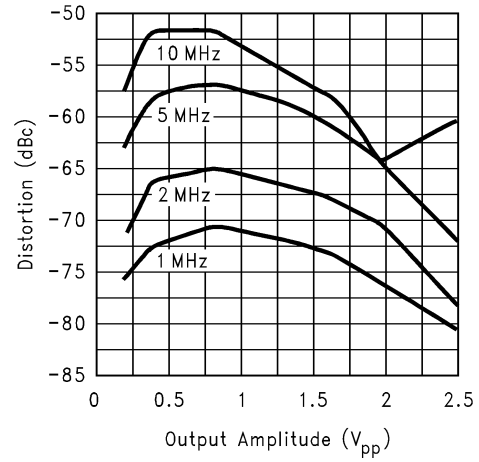
**2nd Harmonic Distortion, $R_L$ = 1kΩ**




DS012733-18

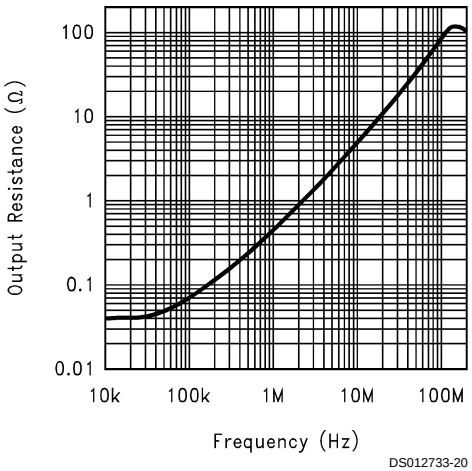
## +5V Typical Performance Characteristics (Continued)

**3rd Harmonic Distortion, $R_L$ = 1kΩ**



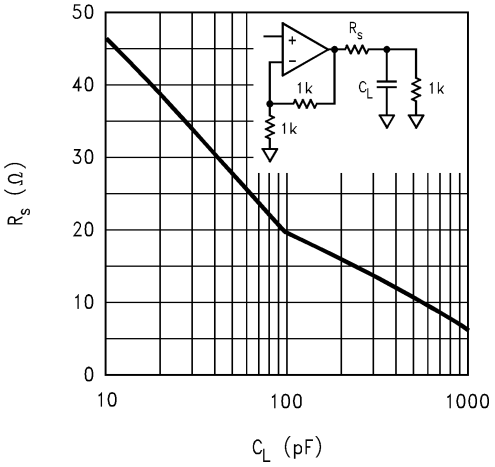

DS012733-19

**Closed Loop Output Resistance**



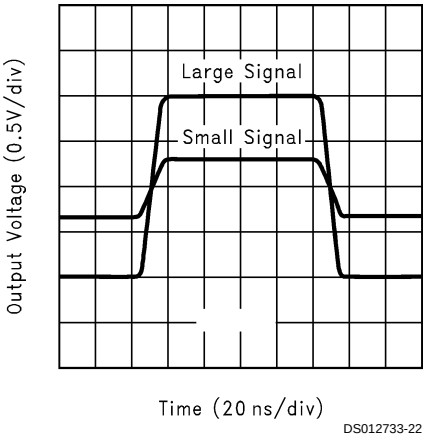

DS012733-20

**Recommended $R_S$ vs. $C_L$**



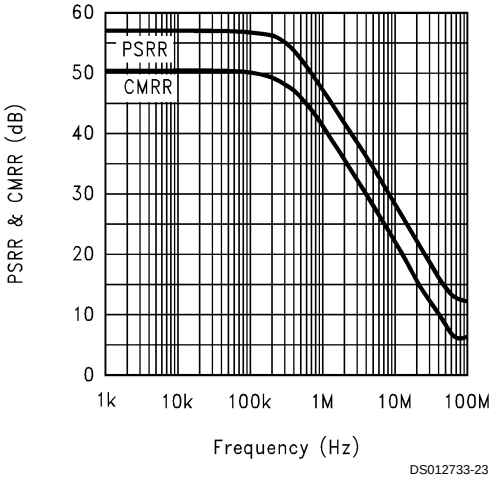

DS012733-21

**Large & Small Signal Pulse Response**



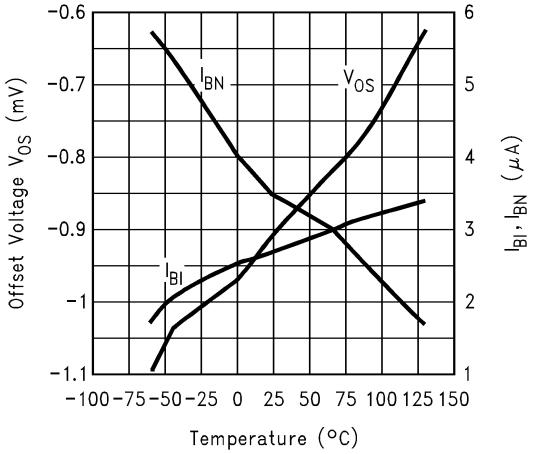

DS012733-22

**PSRR & CMRR**




DS012733-23

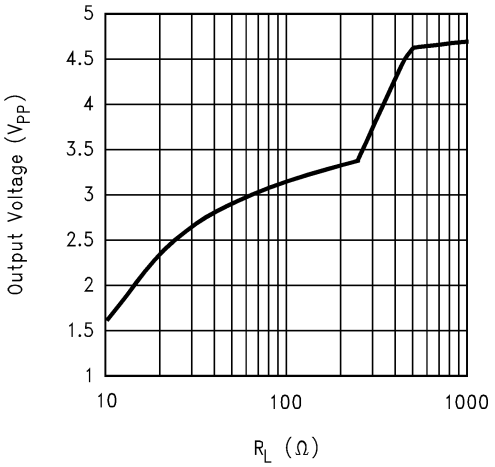
**$I_{BI}$, $I_{BN}$, $V_{OS}$ vs. Temperature**




DS012733-24

## +5V Typical Performance Characteristics (Continued)

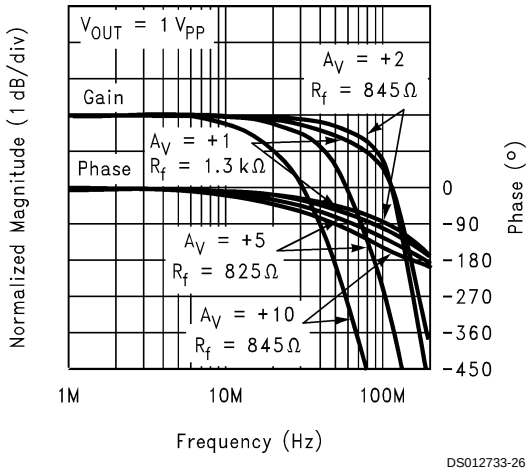
**Maximum Output Voltage vs. $R_L$**




DS012733-25

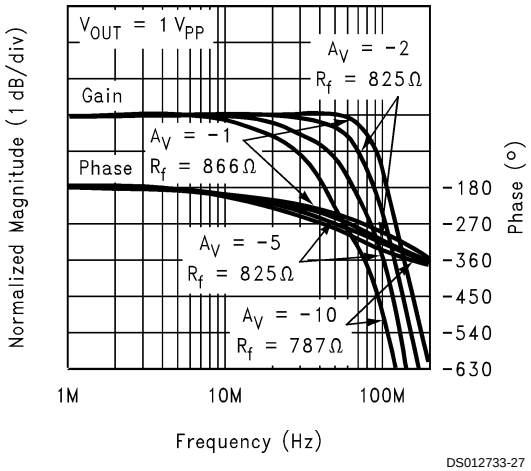
## ±5V Typical Performance Characteristics

**Non-Inverting Frequency Response**



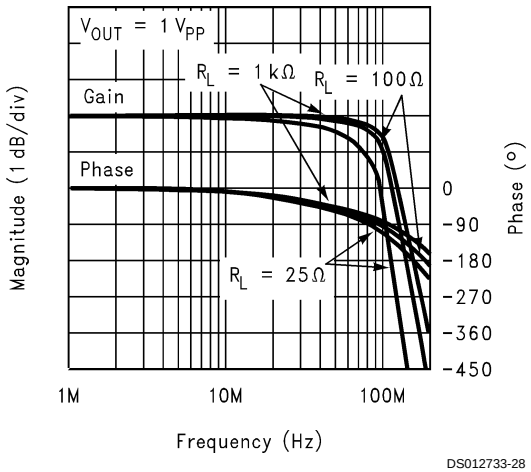

DS012733-26

**Inverting Frequency Response**



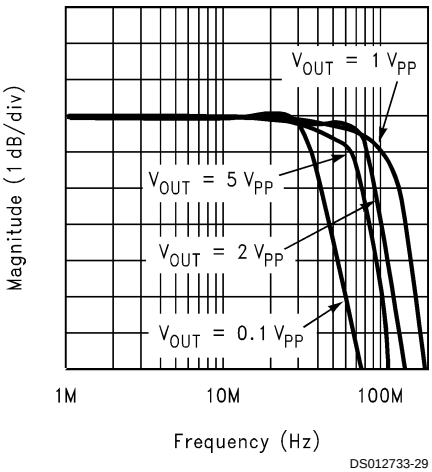

DS012733-27

**Frequency Response vs. $R_L$**




DS012733-28

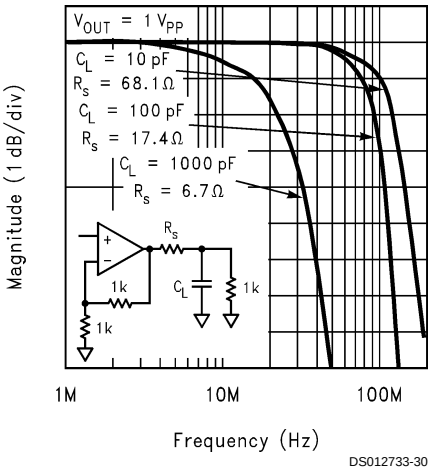
**Frequency Response vs. $V_O$**




DS012733-29

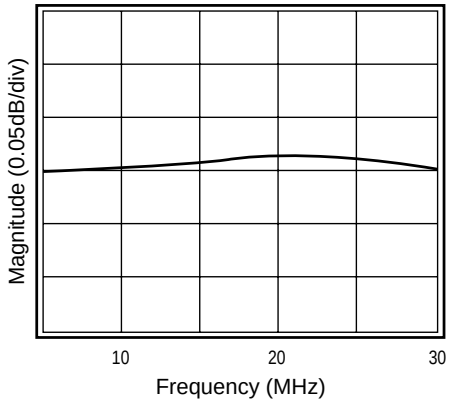
## ±5V Typical Performance Characteristics (Continued)

**Frequency Response vs. $C_L$**



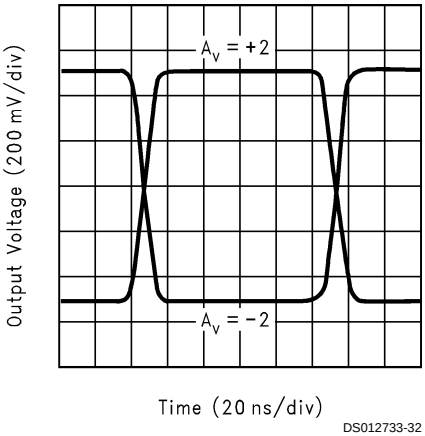

DS012733-30

**Gain Flatness**



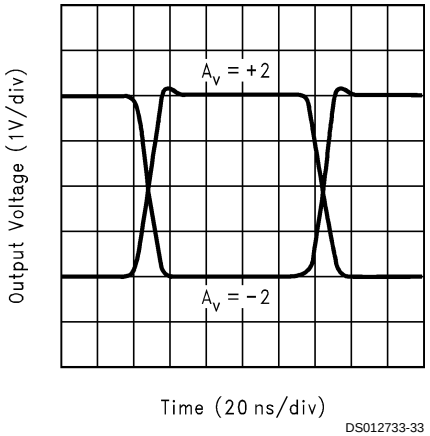

DS012733-31

**Small Signal Pulse Response**



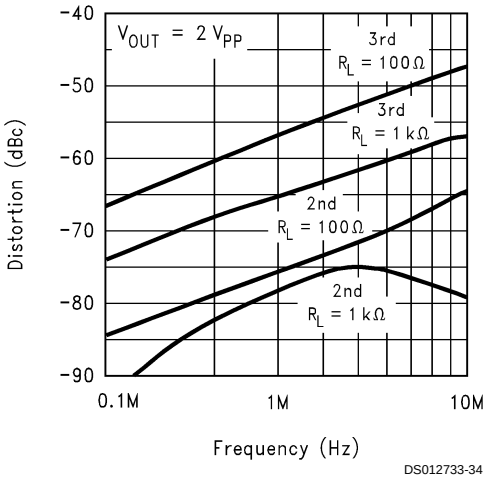

DS012733-32

**Large Signal Pulse Response**



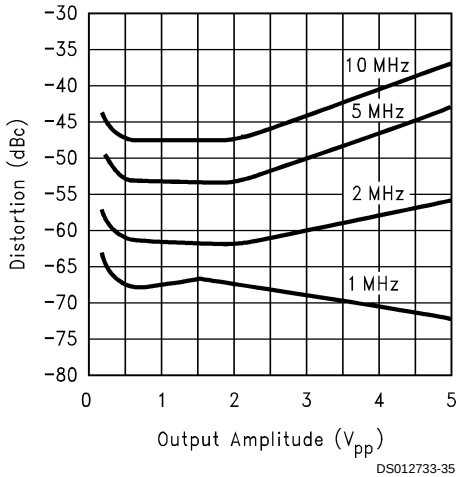

DS012733-33

**2nd & 3rd Harmonic Distortion**




DS012733-34

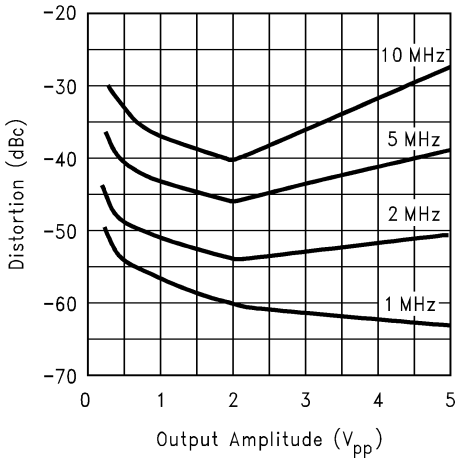
**2nd Harmonic Distortion, $R_L$ = 25Ω**




DS012733-35

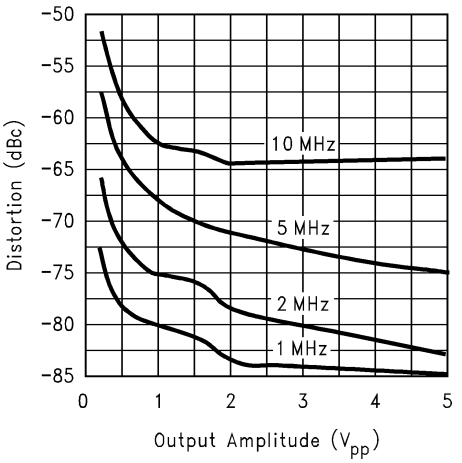
## ±5V Typical Performance Characteristics (Continued)

**3rd Harmonic Distortion, $R_L$ = 25Ω**



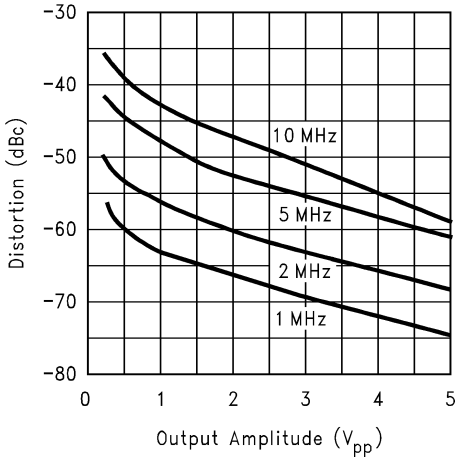

DS012733-36

**2nd Harmonic Distortion, $R_L$ = 100Ω**



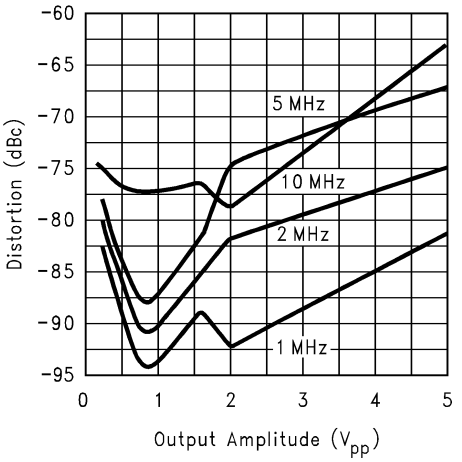

DS012733-37

**3rd Harmonic Distortion, $R_L$ = 100Ω**



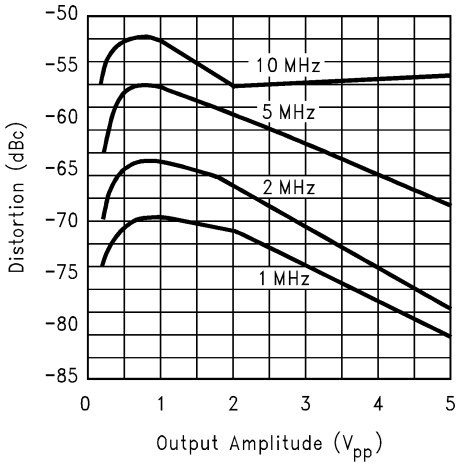

DS012733-38

**2nd Harmonic Distortion, $R_L$ = 1kΩ**



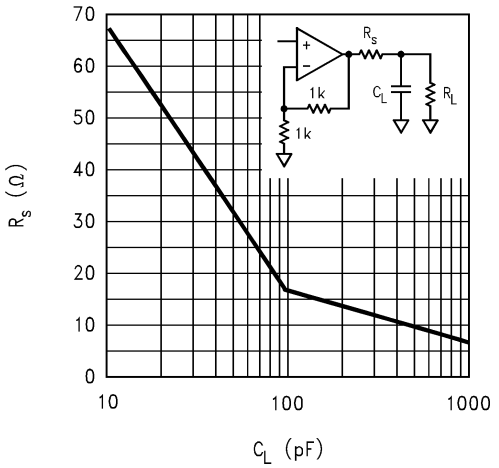

DS012733-39

**3rd Harmonic Distortion, $R_L$ = 1kΩ**




DS012733-40

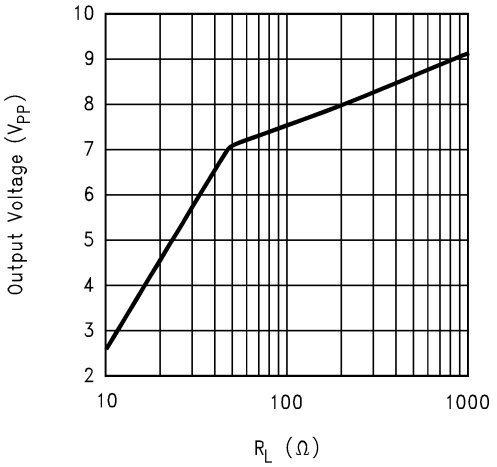
**Recommended $R_S$ vs. $C_L$**




DS012733-41

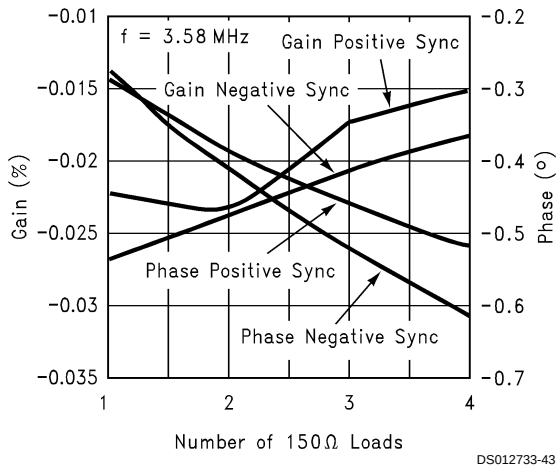
# ±5V Typical Performance Characteristics (Continued)

**Maximum Output Voltage vs. $R_L$**



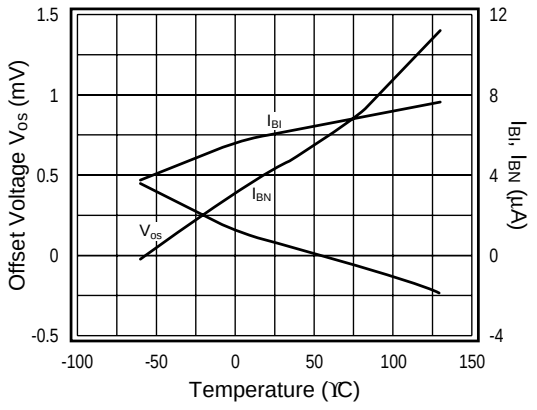

DS012733-42

**Differential Gain & Phase**



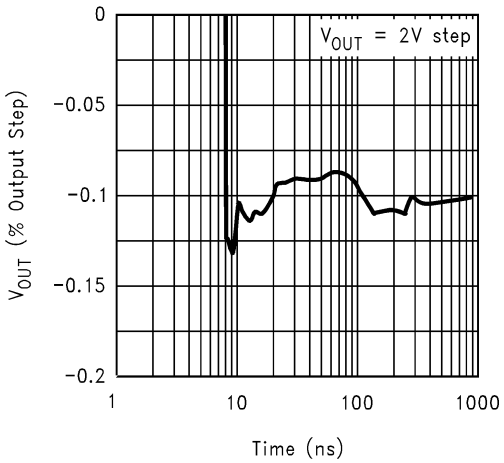

DS012733-43

**$I_{BI}$, $I_{BN}$, $V_{OS}$ vs. Temperature**



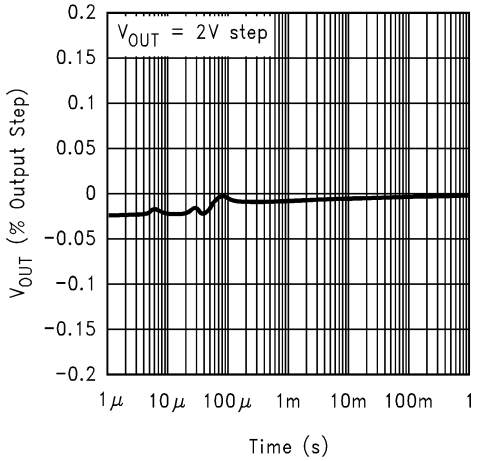

DS012733-44

**Short Term Settling Time**




DS012733-45

**Long Term Settling Time**




DS012733-46

# Application Division

### CLC450 Operation

The CLC450 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC450 operates from a single 5V supply or dual ±5V supplies. Operating from a single supply, the CLC450 has the following features:

- Provides 100mA of output current while consuming 7.5mW of power
- Offers low −79/−75dB 2nd and 3rd harmonic distortion
- Provides BW >60MHz and 1MHz distortion < −65dBc at $V_O = 2.5V_{PP}$

The CLC450 performance is further enhanced in ±5V supply application as indicated in the **±5V Electrical Characteristics** table and **±5V Typical Performance** plots.

### Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable fequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_V}{1 + \frac{R_f}{Z(j\omega)}} \quad (1)$$

where:

- $A_V$ is the closed loop DC voltage gain
- $R_f$ is the feedback resistor
- $Z_{(j(\omega)}$ is the CLC450's open loop transimpedance gain
- $Z_{(j(\omega)}/R_f$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between $R_f$ and $Z_{(j(\omega)}$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing $R_f$ has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

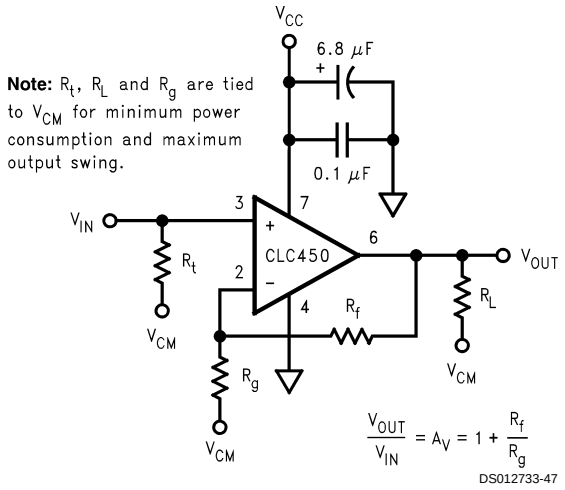
Refer to the **Feedback Resistor Selection** section for more details on selecting a feedback resistor value.

### Design Information

### Single Supply Operation ($V_{cc}$ = +5V, $V_{EE}$ = GND)

The specifications given in the **+5V Electrical Characteristics** table for single supply operation are measured with a common mode voltage ($V_{cm}$) of 2.5V. $V_{cm}$ is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, The Common Mode Input Range (CMIR) of the CLC450 is typically +0.8V to +4.2V. The typical output range with $R_L$ = 100Ω is +1.0V to +4.0V.




**Equation 1.**

**FIGURE 1. Non-Inverting Configuration**

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

### DC Coupled Single Supply Operation

*Figure 1* and *Figure 2* show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

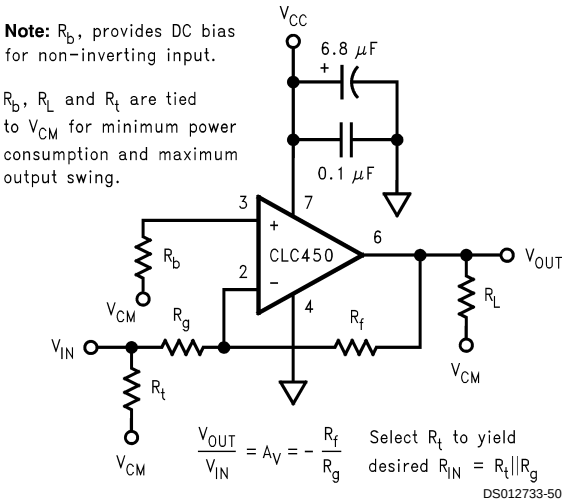



**FIGURE 2. Inverting Configuration**

### AC Coupled Single Supply Operation

*Figure 3* and *Figure 4* show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For $V_{CC}$ = +5V).

## Application Division (Continued)

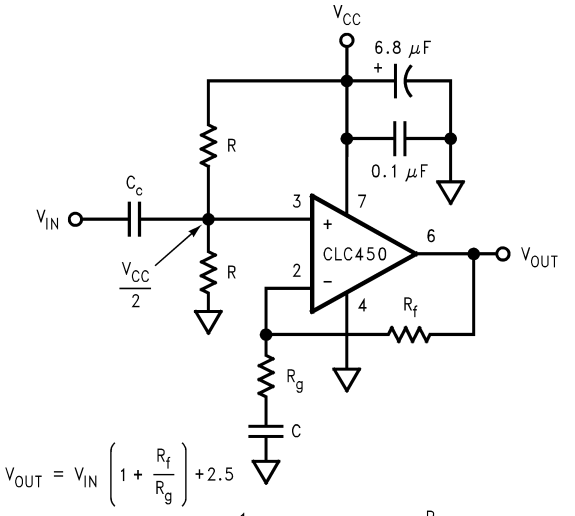



**FIGURE 3. AC Coupled Non -Inverting Configuration**

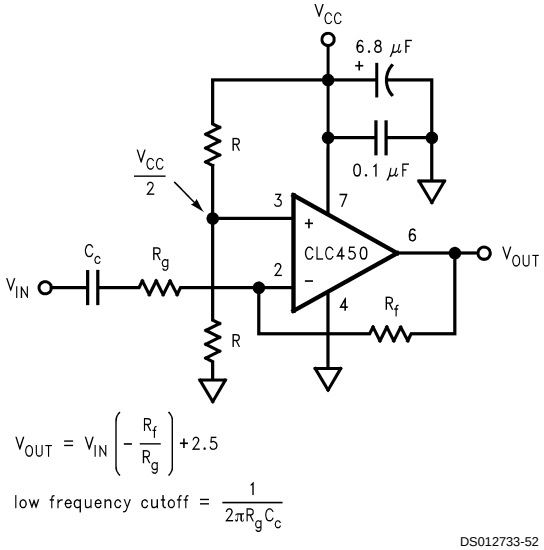



**FIGURE 4. AC Coupled Inverting Configuration**

### Dual Supply Operation

The CLC450 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in *Figure 5* and *Figure 6*.

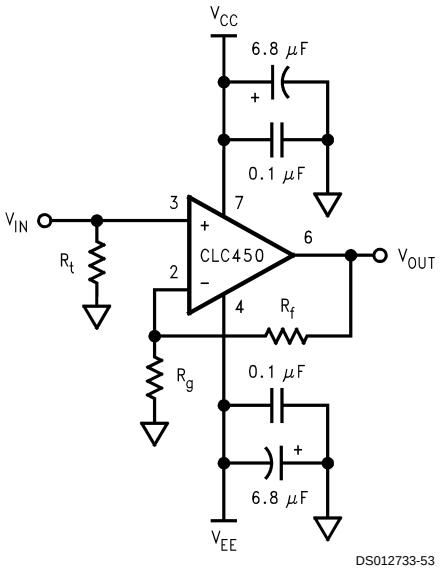



**FIGURE 5. Dual Supply Non-Inverting Configuration**

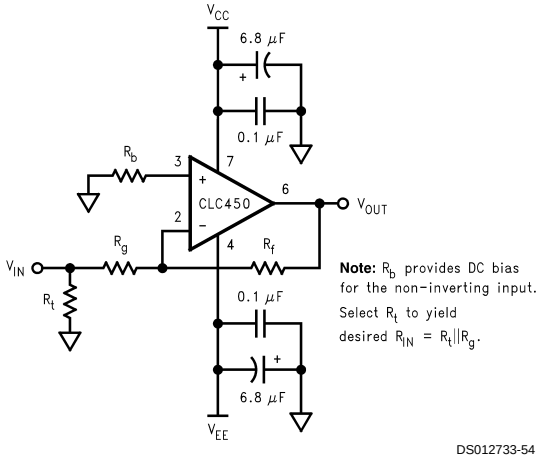



**FIGURE 6. Dual Supply Inverting Configuration**

### Feedback Resistor Selection

The feedback resistor, $R_f$, affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC450, at a gain of +2V/V, is achieved with $R_f$ equal to 1kΩ. The frequency response plots in the **Typical Performance** sections illustrate the recommended $R_f$ for several gains. These recommended values of $R_f$ provide the maximum bandwidth with minimal peaking. Within limits, $R_f$ can be adjusted to optimize the frequency response.

- Decrease $R_f$ to peak frequency response and extend bandwidth
- Increases $R_f$ to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended $R_f$ is doubled, then the bandwidth will be cut in half.

## Application Division (Continued)

### Unity Gain Operation

The recommended $R_f$ for unity gain (+1V/V) operation is 1.5kΩ. $R_g$ is left open. Parasitic capacitance at the inverting node may require a slight increase in $R_f$ to maintain a flat frequency response.

### Bandwidth vs. Output Amplitude

The bandwidth of the CLC450 is at a maximum for output voltages near 1Vpp. The bandwidth decreases for smaller and larger output amplitudes. Refer to the **Frequency Response vs. $V_o$** plots.

### Load Termination

The CLC450 can source and sink near equal amounts of current. For optimum performance, the load should be tied to $V_{cm}$.

### Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load application, a small series resistor at the output of the CLC450 will improve stability and settling performance. The **Frequency Response vs. $C_L$** and **Recommended $R_s$vs. $C_L$** plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

### Transmission Line Matching

One method for matching the characteristic impedance ($Z_o$) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. *Figure 7* shows typical inverting and non-inverting circuit configurations for matching transmission lines.

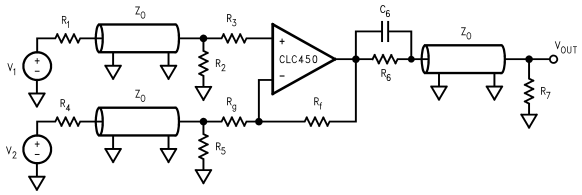



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**FIGURE 7. Transmission Line Matching**

Non-inverting gain applications:

- Connect $R_g$ directly to ground.
- Make $R_1$,$R_2$, $R_6$, $R_7$ equal to $Z_o$.
- Use $R_3$ to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect $R_3$ directly to ground.
- Make the resistors $R_4$, $R_6$, and $R_7$ equal to $Z_o$
- Make $R_5 \| R_g = Z_o$

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use $C_6$ to match the output transmission line over a greater frequency range. $C_6$ compensates for the increase of the amplifier's output impedance with frequency.

### Power Dissipation

Follow these steps to determine the power consumption of the CLC450:

1. Calculate the quiescent (no-load) power:
   $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage:$P_o = (V_{CC} - V_{load})(I_{load})$, where $V_{load}$ and $I_{load}$ are the RMS voltage and current across the external load.
3. Calculate the total RMS power:$P_t = P_{amp} + P_o$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in *Figure 8*. The power derating cure for any CLC450 package can be derived by utilizing the following equation:

$$\frac{(150^\circ - T_{amb})}{\theta_{JA}}$$

Where

- $T_{amb}$ = Ambient temperature (˚C)
- $\theta_{JA}$ = Thermal resistance, from junction to ambient, for a given package (˚C/W)

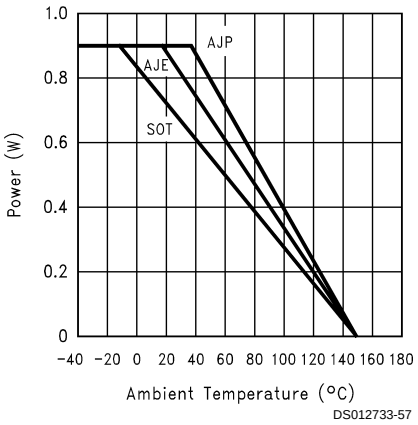


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**FIGURE 8. Power Derating Curves**

### Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC450 (730013-DIP, 730027-SOIC, 730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.
-

### Evaluation Board Information

Data sheet are available for the CLC730013/CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts

## Application Division (Continued)

- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of National's high speed amplifiers. This table for the CLC450 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

**Components Needed to Evaluate the CLC450 on the Evaluation Board:**

- $R_f$, $R_g$ — Use this product data sheet to select values.
- $R_{in}$, $R_{out}$ - Typically 50Ω (Refer to the **Basic Operation** section of the evaluation board data sheet for details
- $R_f$ — Optional resistor for inverting gain configurations (Select $R_f$ to yield desired input impedance = $R_g||R_f$
- $C_1$, $C_2$- 0.1 µF ceramic capacitors
- $C_3$, $C_4$- 6.8 µF tantalum capacitors
- $C_5$, $C_6$, $C_7$, $C_8$
- $R_1$ thru $R_8$

Components not used:

- $C_5$, $C_6$, $C_7$, $C_8$
- $R_1$ thru $R_8$

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

**SPICE Models**

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The **readme** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

**Application Circuits**

**Single Supply Cable Driver**

The typical application shown on the front page shows the CLC450 driving 10m of 75Ω coaxial cable. The CLC450 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at $V_o$.

**Single Supply Lowpass Filter**

*Figure 9* and *Figure 10* illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine $R_1$, $R_2$, $C_1$ and $C_2$ based on the desired Q and corner frequency.

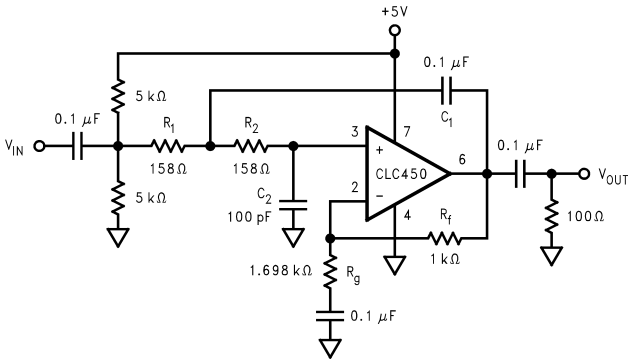


**FIGURE 9. Lowpass Filter Topology**

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1-K)\sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3-K)}$$

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**FIGURE 10. Design Equations**

This example illustrates a lowpass filter with Q = 0.707 and corner frequency $f_c$ = 10MHz. AQ of 0.707 was chosen to achieve a maximally flat, Butterworth response. *Figure 11* indicates the filter response.

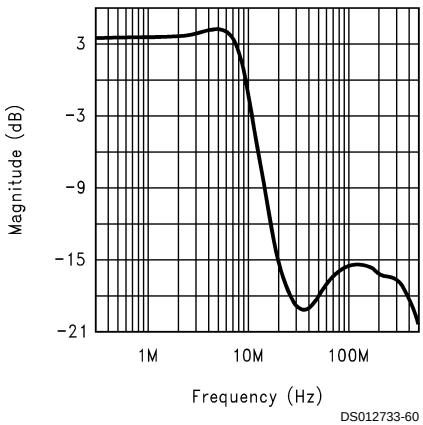



**FIGURE 11. Lowpass Response**

# Application Division (Continued)

### Twisted Pair Driver

The high output current and low distortion, of the CLC450, make it well suited for driving transformers. *Figure 12* illustrates a typical twisted pair driver utilizing the CLC450 and a transformer. The transformer provides the signal and its inversion for the twisted pair.

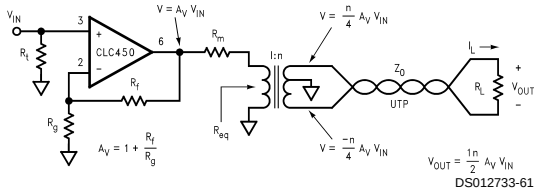



**FIGURE 12. Twisted Pair Driver**

To match the line's characteristic impedance ($Z_o$) set:

- $R_L = Z_O$
- $R_m = R_{eq}$

Where $R_{eq}$ is the transformed value of the load impedance, ($R_L$), and is approximated by:

$$R_{eq} = \frac{R_L}{n^2}$$

Select the transformer so that it loads the line with a value close to $Z_o$, over the desired frequency range. The output impedance, $R_o$, of the CLC450 varies within frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of $R_o$

$$\text{Return Loss (dB)} \approx -20\log_{10}\left|n^2 \cdot \frac{R_O}{Z_O}\right|$$

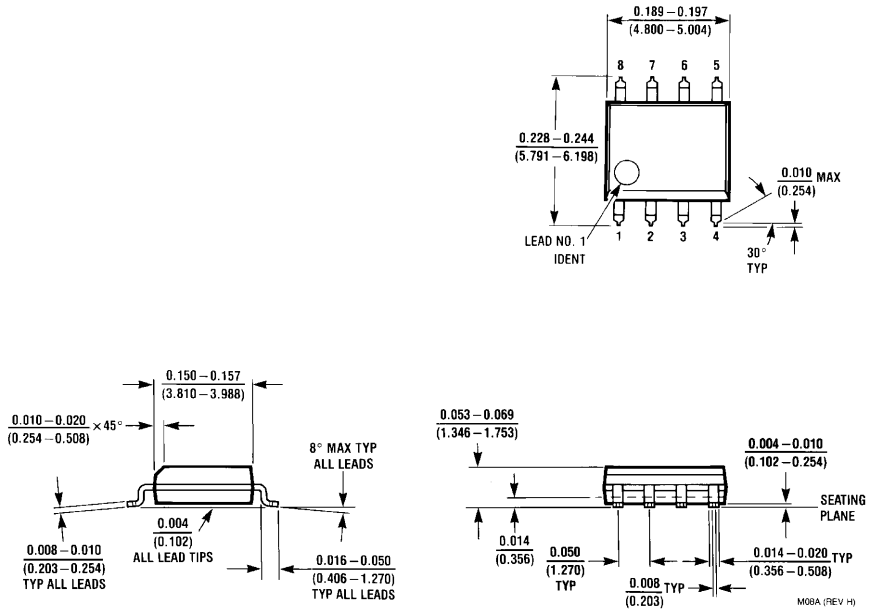
The load current ($I_i$) and voltage ($V_o$) are related to the CLC450's maximum output voltage and current by:

$$\left|V_O\right| \leq n \cdot V_{max}$$

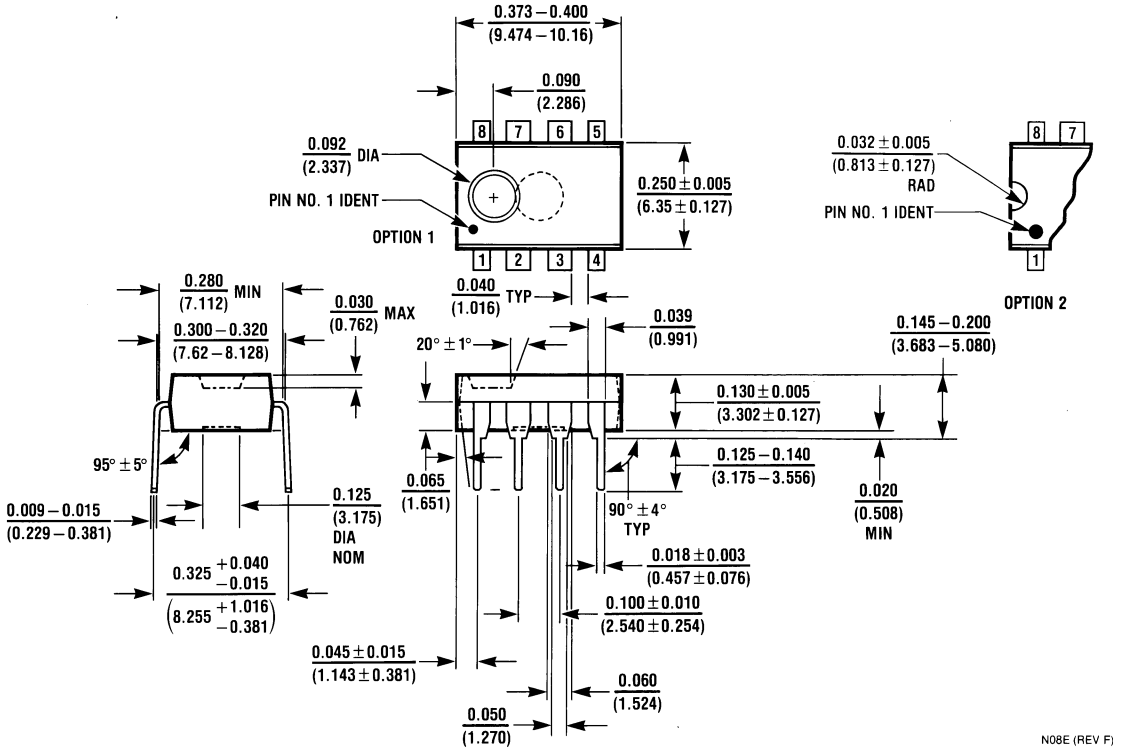
$$\left|I_L\right| \leq \frac{I_{max}}{n}$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

## Physical Dimensions inches (millimeters) unless otherwise noted

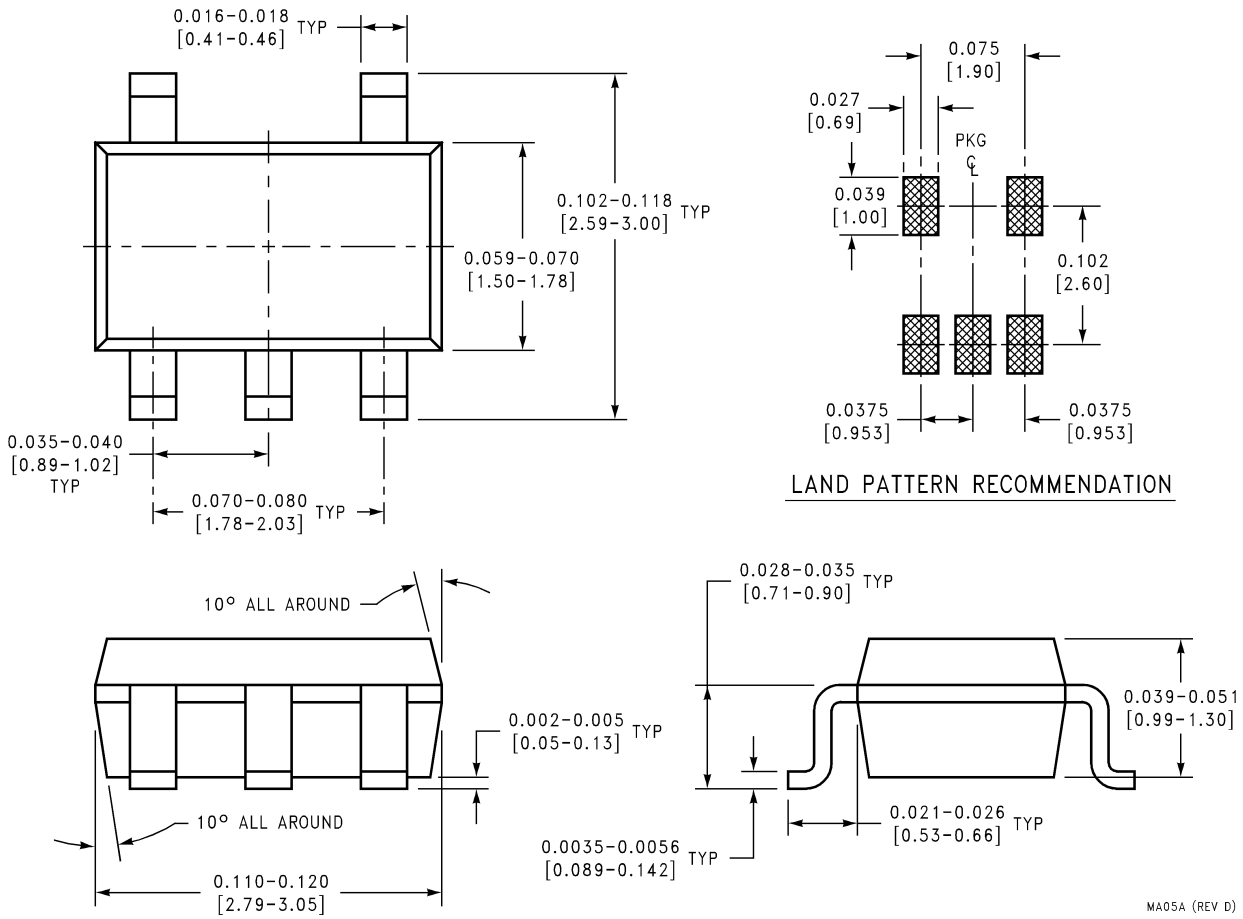



**8-Pin SOIC**
**NS Package Number M08A**




**8-Pin MDIP**
**NS Package Number N08E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**5-Pin SOT23**
**NS Package Number MA05A**

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