$\mathcal{N}$ **National** *Semiconductor*

CLC449
1.1GHz Ultra Wideband Monolithic Op Amp

General Description

The CLC449 is an ultra high speed monolithic op amp, with a typical −3dB bandwidth of 1.1GHz at a gain of +2. This wideband op amp supports rise and fall times less than 1ns, settling time of 6ns (to 0.2%) and slew rate of 2500V/µs. The CLC449 achieves 2nd harmonic distortion of −68dBc at 5MHz at a low supply current of only 12mA. These performance advantages have been achieved through improvements in National's proven current feedback topology combined with a high speed complementary bipolar process.

The DC to 1.2GHz bandwidth of the CLC449 is suitable for many IF and RF applications as a versatile op amp building block for replacement of AC coupled discrete designs. Operational amplifier functions such as active filters, gain blocks, differentiation, addition, subtraction and other signal conditioning functions take full advantage of the CLC449's unity-gain stable closed-loop performance.

The CLC449 performance provides greater headroom for lower frequency applications such as component video, high resolution workstation graphics, and LCD displays. The amplifier's 0.1dB gain flatness to beyond 200MHz, plus 0.8ns (2V step) rise and fall times are ideal for improved time domain performance. In addition, the 0.03%/0.02˚ differential gain/phase performance allows system flexibility for handling standard NTSC and PAL signals.

In applications using high speed flash A/D and D/A converters, the CLC449 provides the necessary wide bandwidth (1.1GHz), settling (6ns to 0.02%) and low distortion into 50Ω loads to improve SFDR.

Features

- 1.1GHz small-signal bandwidth (A_v =+2)
- 2500V/µs slew rate
- 0.03%, 0.02˚ D_G, D_Φ
- 6ns settling time to 0.2%
- 3rd order intercept, 30dBm @ 70MHz
- Dual ±5V or single 10V supply
- High output current: 80mA
- 2.5dB noise figure
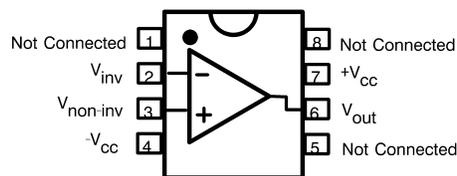
Applications

- High performance RGB video
- RF/IF amplifier
- Instrumentation
- Medical electronics
- Active filters
- High speed A/D driver
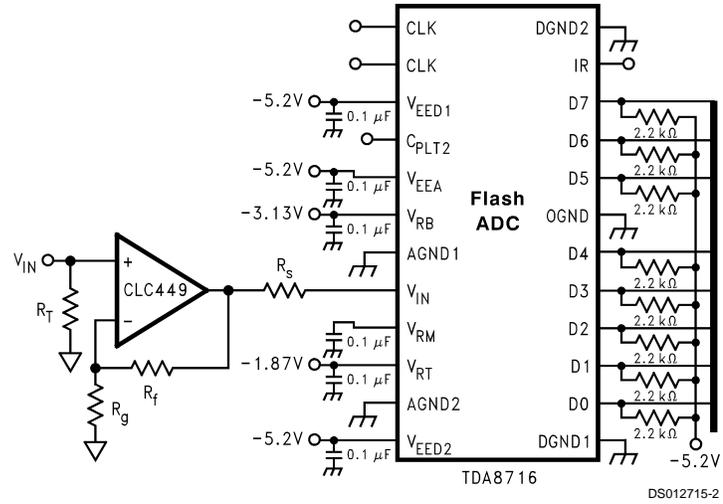- High speed D/A buffer

Frequency Response (A_V = +2V/V)
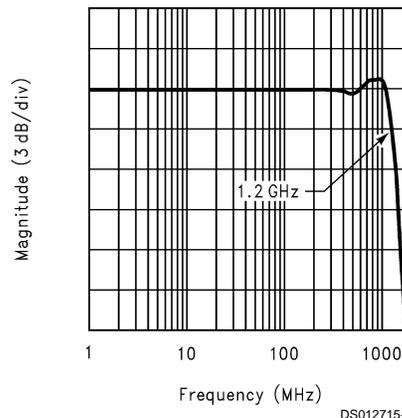
DS012715-1

Connection Diagram

DS012715-3

Pinout
DIP & SOIC

Typical Application

120MSPS High Speed Flash ADC Driver

DS012715-2

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40°C to +85°C	CLC449AJP	CLC449AJP	N08E
8-pin plastic SOIC	−40°C to +85°C	CLC449AJE	CLC449AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	±6V
I_{OUT} is short circuit protected to ground	
Common Mode Input Voltage	±V_{CC}
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Solder Duration (+300°C)	10 sec
ESD (human body model)	500V

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	90°C/W	105°C/W
SOIC	110°C/W	130°C/W

Electrical Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Ambient Temperature		CLC449AJ	+25°C	+25°C	0 to 70°C	−40 to +85°C	
Frequency Domain Response							
	-3dB Bandwidth						
	Small Signal	<0.2V_{PP}	1100				MHz
	Large Signal	<2.0V_{PP}	500	380	380	360	MHz
	±0.1 dB Bandwidth	<2.0V_{PP}	200				MHz
	Gain Glatness						
	Peaking	DC to 200MHz	0				dB
	Rolloff	DC to 200MHz	0.1	0.5	0.5	0.5	dB
	Linear Phase Deviation	<200MHz	0.8				deg
	Differential Gain	R_L = 150Ω, 4.43MHz	0.03	0.05	0.05	0.05	%
	Differential Phase	R_L = 150Ω, 4.43MHz	0.02	0.02	0.05	0.05	deg
Time Domain Response							
	Rise and Fall Time	2V Step	0.8	1.1	1.1	1.1	ns
	Settling Time to ±0.2%	2V Step	6				ns
	Settling Time to ±0.1%	2V Step	11				ns
	Overshoot	2V Step	10	18	18	18	%
	Slew Rate	4V Step	2500	2000	2000	2000	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	2V_{PP}, 5MHz	−63	−59	−59	−59	dBc
		2V_{PP}, 20MHz	−52	−48	−48	−48	dBc
		2V_{PP}, 50MHz	−44	−40	−40	−40	dBc
	3rd Harmonic Distortion	2V_{PP}, 5MHz	−84	−77	−75	−75	dBc
		2V_{PP}, 20MHz	−73	−66	−64	−64	dBc
		2V_{PP}, 50MHz	−62	−55	−53	−53	dBc
	3rd Order Intercept	70MHz	30				dBm
	1dB Gain Compression @ 50MHz		16				dBm
	Equivalent Input Noise						
	Non-Inverting Voltage	1MHz	2.2	2.9			nV/$\sqrt{Hz}$
	Inverting Current	1MHz	15	20.0			pA/$\sqrt{Hz}$
	Non-Inverting Current	1MHz	3	5.0			pA/$\sqrt{Hz}$
Static, DC Performance							
	Input Offset Voltage (Note 3)		3	7	9	9	mV

Electrical Characteristics (Continued)

$A_V = +2$, $V_{CC} = \pm5V$, $R_L = 100\Omega$, $R_f = 250\Omega$; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Static, DC Performance							
	Average Drift		25				µV/C˚
	Input Bias Current (Note 3)	Non-Inverting	6	30	45	60	µA
	Average Drift		50				nA/˚C
	Input Bias Current (Note 3)	Inverting	2	20	25	40	µA
	Average Drift		25				nA/C˚
	Power Supply Rejection Ratio	DC	48	43	41	41	dB
	Common Mode Rejection Ratio	DC	47	44	45	46	dB
	Supply Current (Note 3)	$R_L = \infty$	12	13.5	14	14	mA
Miscellaneous Performance							
	Input Resistance	Non-Inverting	400	200	200	150	KΩ
	Input Capacitance	Non-Inverting	1.3				pF
	Output Resistance	Closed Loop	0.1	0.15	0.15	0.25	Ω
	Output Voltage Range	$R_L = \infty$	3.3	3.1	3.1	3.1	V
		$R_L = 100\Omega$	2.9	2.8	2.8	2.8	V
	Input Voltage Range	Common-Mode	2.4	2.2	2.1	1.9	V
	Output Current		80	60	50	40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C.

Typical Performance Characteristics

Non-Inverting Frequency Response

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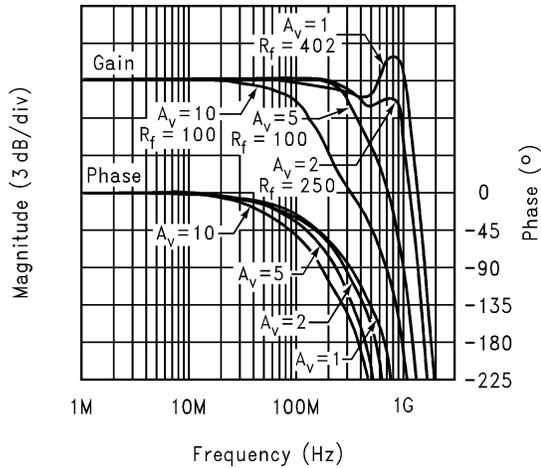
Inverting Frequency Response
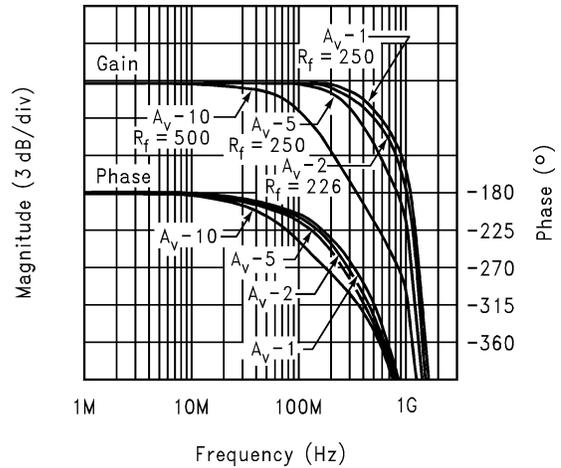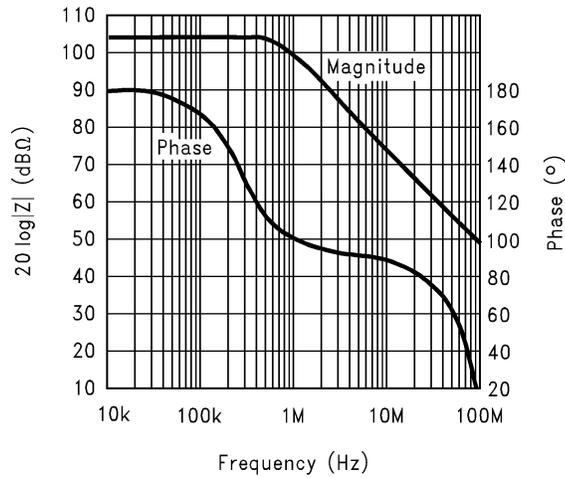

DS012715-5

Typical Performance Characteristics (Continued)
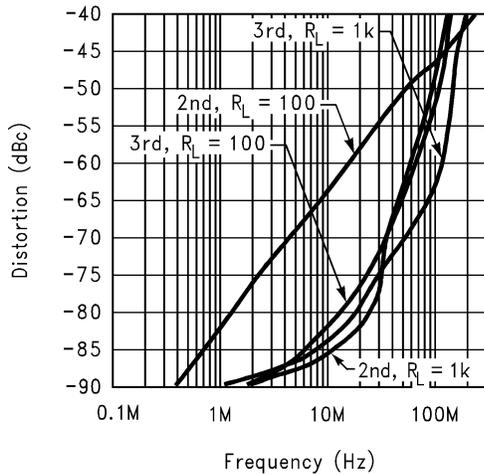
Frequency Response vs. Load
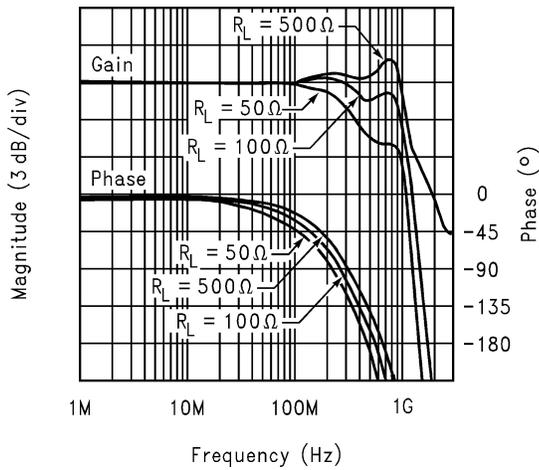
DS012715-6

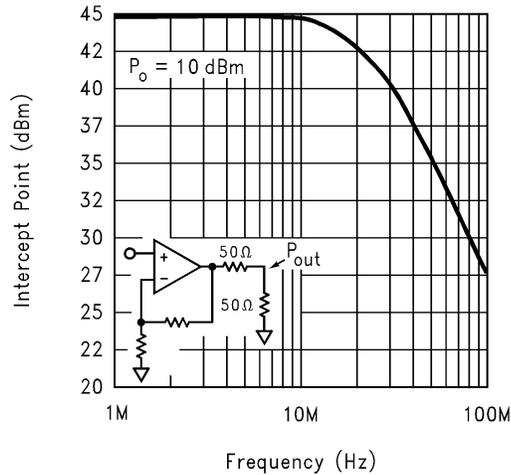**Open Loop Transimpedance, Z(s)**
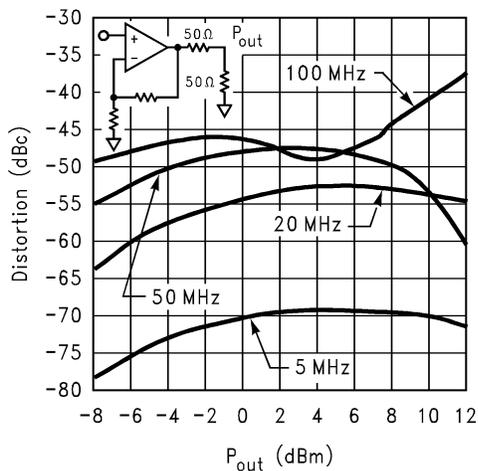

DS012715-7

Harmonic Distortion vs. Frequency

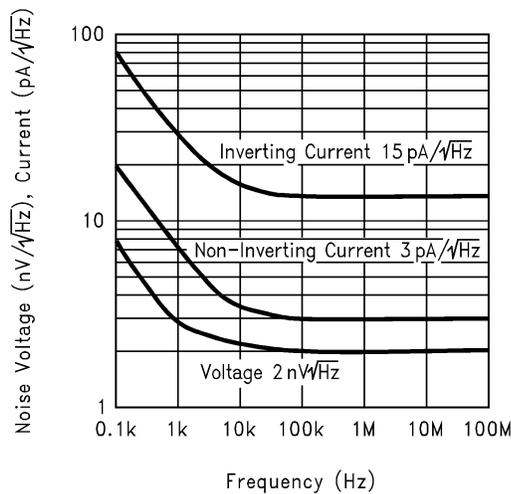DS012715-8

2-Tone, 3rd Order Intermodulation Intercept

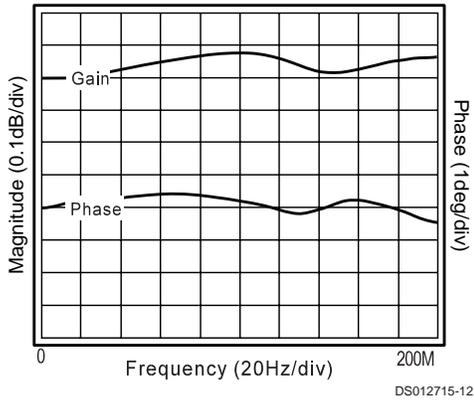

DS012715-9

2nd Harmonic Distortion vs. P$_{out}$

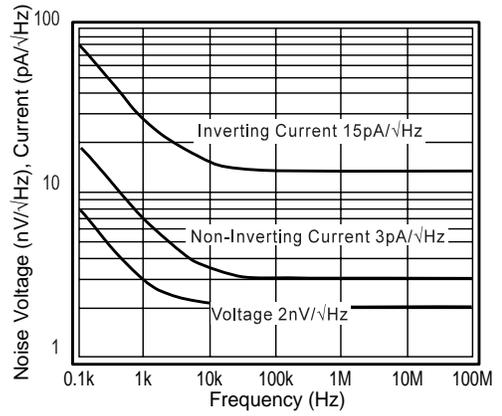DS012715-10

3rd Harmonic Distortion vs. P$_{out}$

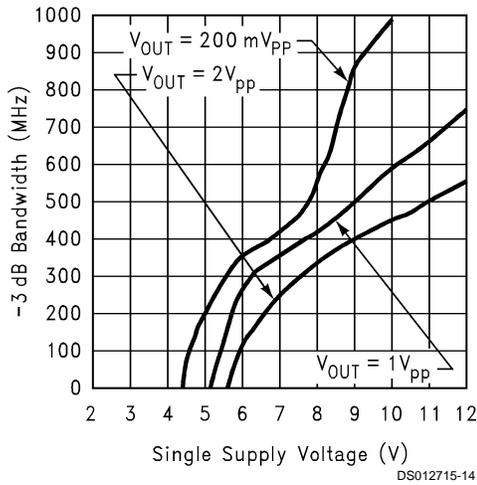DS012715-11

Typical Performance Characteristics (Continued)
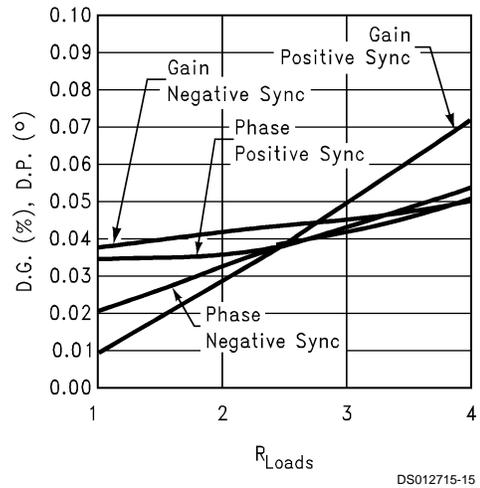
Gain Flatness and Linear Phase

DS012715-12

Equivalent Input Noise

DS012715-13

Single Supply −3dB Bandwidth

DS012715-14

Differential Gain and Phase

DS012715-15

PSRR, CMRR, and Closed Loop R_{OUT}
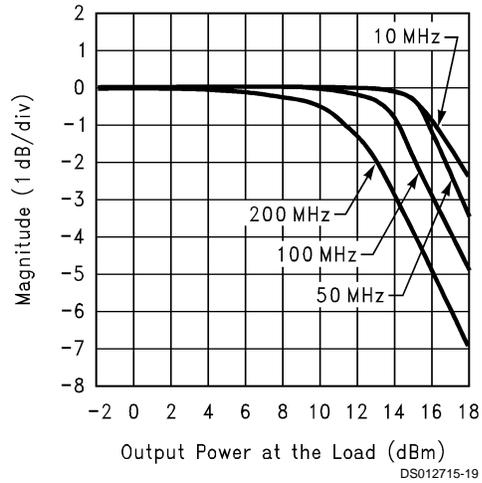

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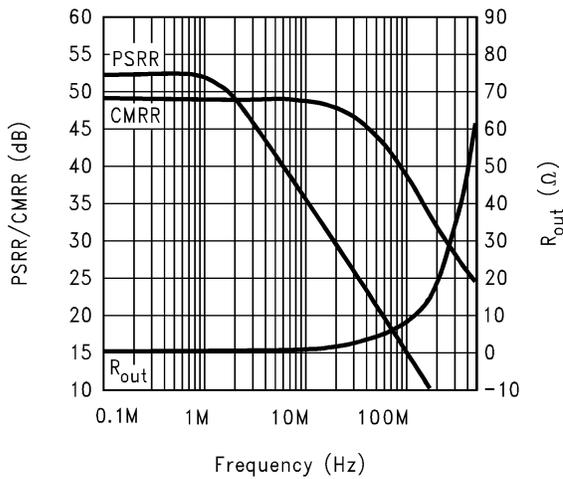
Small Signal Pulse Response

DS012715-17
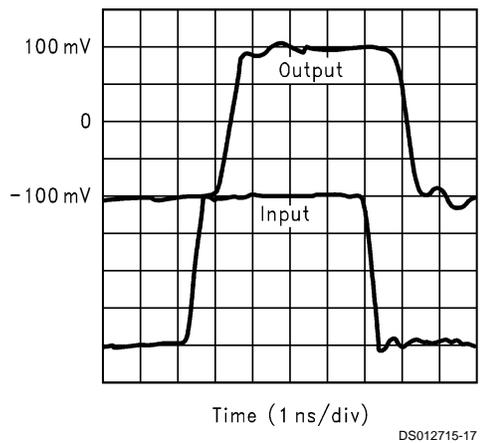
Typical Performance Characteristics (Continued)

Large Signal Pulse Response

DS012715-18
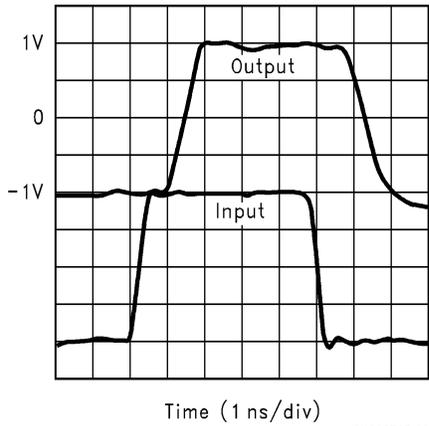
Gain Compression

DS012715-19

Typical I_{BI}, I_{BN}, V_{IO} vs. Temperature
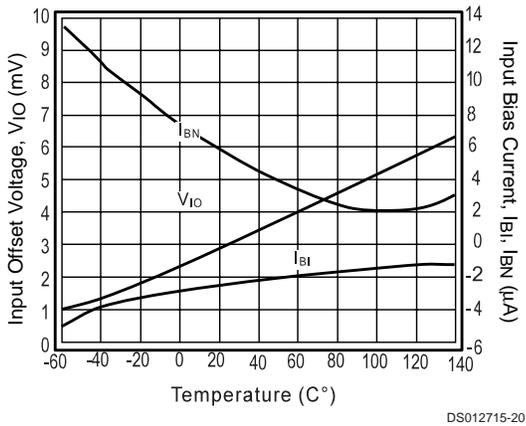
DS012715-20

R_S and Settling Time vs. C_L

DS012715-21

Input VSWR

DS012715-22

Output VSWR

DS012715-23

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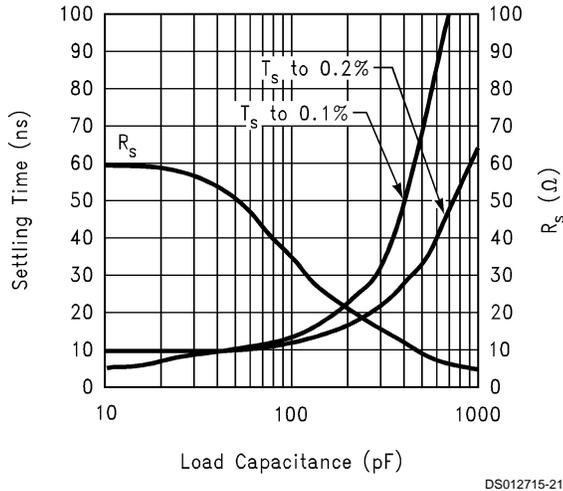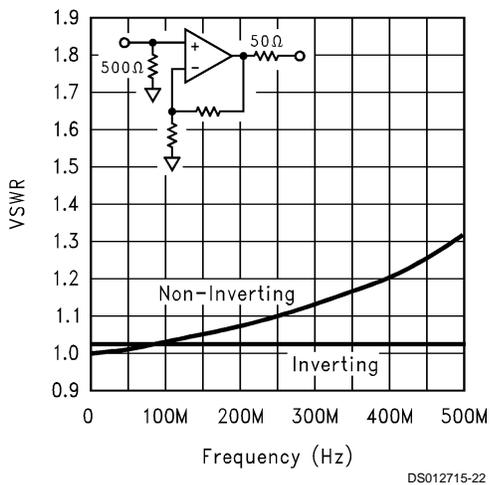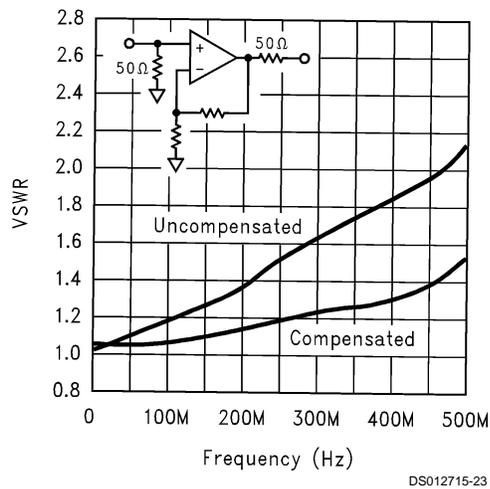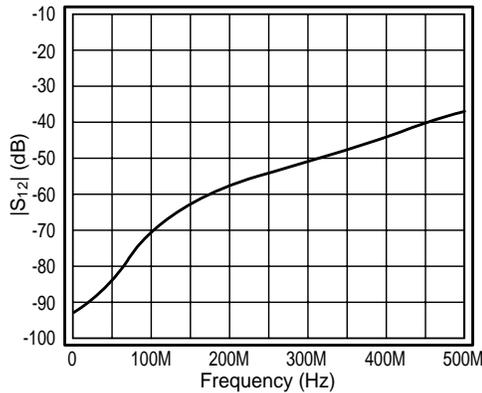
Typical Performance Characteristics (Continued)

Reverse Isolation (S$_{12}$)

DS012715-24

Application Division

CLC449 Operation

CLC449 Extended Application Information

The following design and application topics will supply you with:

- A comprehensive set of design parameters and design parameter adjustment techniques.
- A set of formulas that support design parameter change prediction
- A series of common applications that the CLC449 supports.
- A set of easy to use design guidelines for the CLC449.

Additional design applications are possible with the CLC449. If you have application questions, call 1-800-272-9959 in the U.S. to contact a technical staff member.

DC Gain (Non-inverting)

The non-inverting DC voltage gain for the configuration shown in is:

$$A_V = 1 + \frac{R_f}{R_g}$$
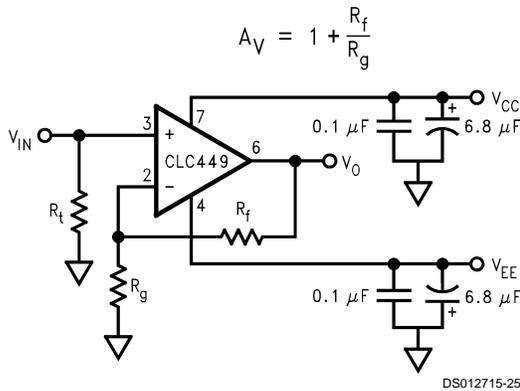
DS012715-25

FIGURE 1. Non-Inverting Gain

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors, R_f, for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor $_t$ in *Figure 1* provides DC bias for the non-inverting input.

For $A_V \leq 5$, calculate the recommended R_f as follows:

$R_f \cong 340 - A_V \times R_i$ where $R_i = 45\Omega$. For $A_V > 5$, the minimum recommended R_f is 100Ω.

Select R_g to set the DC gain:

$$R_g = \frac{R_f}{A_V - 1}$$

Accuracy of DC gain is usually limited by the tolerance of R_f and R_g.

DC Gain (unity gain buffer)

Unity gain buffers are easily designed with a current-feedback amplifier as long as the recommended feedback resistor $R_f = 402\Omega$ is used and $R_g = \infty$, i.e., open. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC Gain (inverting)

The inverting DC voltage gain for the configuration shown in *Figure 2* is

$$A_V = - \frac{R_f}{R_g}$$
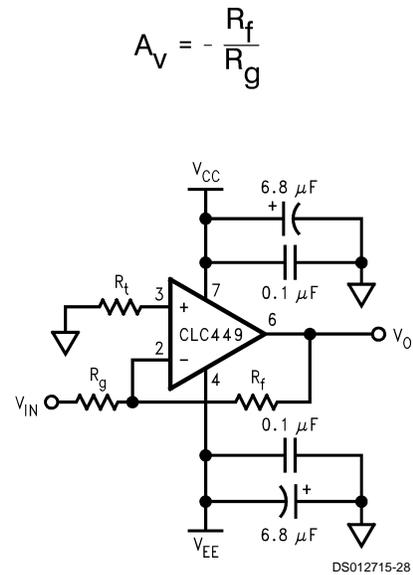
DS012715-28

FIGURE 2. Inverting Gain

Application Division (Continued)

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors R_f for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t in *Figure 2* provides DC bias for the non-inverting input.

For $|A_V| \leq 4$, calculate the recommended R_f as follows:

$R_f \cong 295 - |A_V| \times R_i$ where $R_i = 45\Omega$. For $|A_V| > 4$, the minimum recommended R_f is 100Ω.

Select R_g to set the DC gain:

$$R_g = \frac{R_f}{|A_V|}$$

At large gains, R_g becomes small and will load the previous stage. This situation is resolved by driving R_g with a low impedance buffer like the CLC111, or increasing R_f and R_g see the **Bandwidth (Small Signal)** sub-section for the tradeoffs).

Accurate DC gain is usually limited by the tolerance of the external resistors R_f and R_g.

Bandwidth (Small Signal)

The CLC449 current-feedback amplifier bandwidth is a function of the feedback resistor (R_f), not of the DC voltage gain (A_v). The bandwidth is approximately proportional to $1/R_f$. As a rule, if R_f doubles, the bandwidth is cut in half. Other AC specifications will also be degraded. **Decreasing R_f from the recommended value increases peaking and for very small values of R_f oscillation will occur.**

With an inverting amplifier design, peaking is sometimes observed. This is often the result of layout parasitics caused by inadequate ground planes or long traces. If this is observed, placing a 50 to 200Ω resistor between the non-inverting pin and ground will usually reduce the peaking.

Bandwidth (Minimum Slew Rate)

Slew rate influences the bandwidth for large signal sinusoids. To determine an approximate value of slew rate, necessary to support large sinusoids use the following equation:

$$SR \approx 5 \times f \times V_{peak}$$

V_{peak} is the peak output sinusoid voltage, f is the frequency of the sinusoid.

The slew rate of the CLC449 in inverting gains is always higher than in non-inverting gains.

DC Design (Level Shifting)

Figure 3 shows a DC level shifting circuit for inverting gain configurations. V_{ref} produces a DC output level shift of

$$^{-}V_{ref} \times \frac{R_f}{R_{ref}}$$

which is independent of the DC output produced by V_{in}.
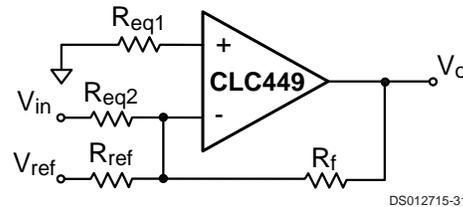

DS012715-31

FIGURE 3. Level Shifting Circuit

DC Design (Single Supply)

Figure 4 is a typical single-supply circuit. Resistors R_1 and R_2 form a voltage divider that sets the non-inverting input DC voltage. This circuit has a DC gain of 1. The coupling capacitor C_1 isolates the DC bias point from the previous stage. Both capacitors make a high pass response; the high frequency gain is determined by R_f and R_g.
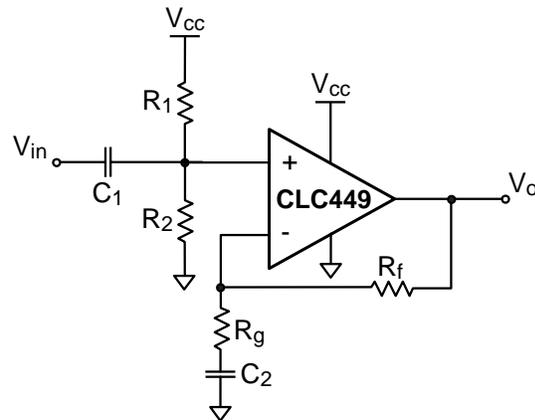

DS012715-32

FIGURE 4. Single Supply Circuit

The complete gain equation for the circuit in *Figure 4* is

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{1+s\tau_1} \cdot \frac{1+s\tau_2 \cdot \left(1+\frac{R_f}{R_g}\right)}{1+s\tau_2}$$

where $s = j\omega$, $\tau_1 = (R_1 \| R_2) \times C_1$, and $\tau_2 = R_g C_2$.

DC Design (DC Offsets)

The DC offset model shown in *Figure 5* is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = -\left(V_{os} + I_{BN} \cdot R_{eq1}\right) \cdot \left(1 + \frac{R_f}{R_{eq2}}\right) + \left(I_{BI} \cdot R_f\right)$$

The current offset terms, I_{BN} and I_{BI}, **do not track each other.** The specifications are stated in terms of magnitude only. Therefore, the terms V_{OS}, I_{BN}, and I_{BI} may have either positive or negative polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

Application Division (Continued)
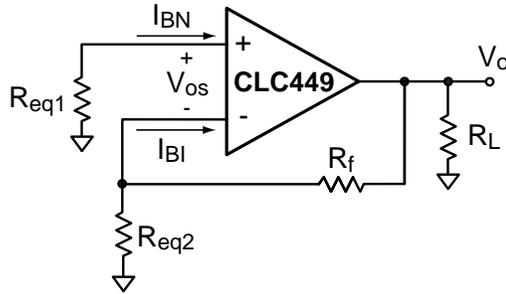
DS012715-35

FIGURE 5. DC Offset Model

DC Design (Output Loading)

R_L, R_f, and R_g load the op amp output. The equivalent closed-loop load impedance seen by the output in *Figure 5* is:

$R_{L\_eq} = R_L \| (R_f + R_{eq2})$, non-inverting gain

$R_{L\_eq} = R_L \| R_f$ inverting gain

R_{L_eq} needs to be kept large enough so that the minimum available output current can produce the required output voltage swing.

Capacitive Loads

Capacitive loads, such as found in A/D converters, require a series resistor (R_s in the output to improve settling performance. The **R_s and Settling Time vs. C_L** plot in the **Typical Performance Characteristics** section provides the information for selecting this resistor.

Also, use a series resistor to reduce the effects of reactive loads on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. *Figure 6* shows the typical circuit configurations for matching transmission lines.

In non-inverting gain applications, R_g is connected directly to ground. The resistors R_1, R_2, R_6, and R_7 are equal to the characteristic impedance
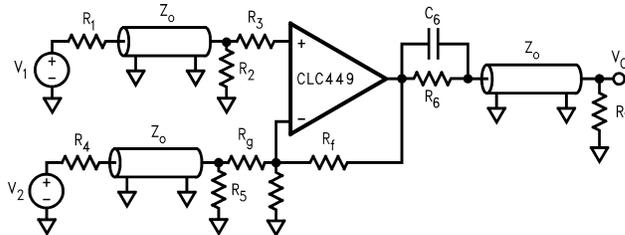
DS012715-36

FIGURE 6. Transmission Line Matching

In inverting gain applications, R_3 is connected directly to ground. The resistor R_4, R_6, and R_7 are equal to Z_0. The parallel combination of R_5 and R_g is also equal to Z_0.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

Thermal Design

To calculate the power dissipation for the CLC449, follow these steps:

1. Calculate the no-load op amp power:

$P_{amp} = I_{cc} (V_{cc} - V_{EE})$

2. Calculate the output stage's RMS power:

$P_o = (V_{cc} - V_{load}) I_{load}$, where V_{load} and I_{load} are the RMS voltage and current across the external load.

3. Calculate the total op amp RMS power:

$P_t = P_{amp} + P_o$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 150 - P_t \times \theta_{JA}$ where θ_{JA} is the thermal resistance from junction to ambient in ˚C/W, and T_{amb} is in ˚C. The **Package Thermal Resistance** section contains the thermal resistance for various packages.

Dynamic Range (input/output protection)

Input ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

Dynamic Range (input/output levels) The **Electrical Characteristics** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current also specified in the **Electrical Characteristics** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range.

For transimpedance or inverting gain applications, the current (I_{inv}) injected at the inverting input of the op amp needs to be:

$$|I_{in}| \le \frac{V_{max}}{R_f}$$

where V_{max} is the Output Voltage Range .

The voltage ranges discussed above are achieved as long as the equivalent output load is large enough so that the output current can produce the required output voltage swing. See the **DC Design (output loading)** sub-section for details.

Dynamic Range (Intermods)

In RF applications, the CLC449 specifies a third order intercept of 30dBm at 70MHz and P_O = 10dBm.at a gain of 10. A **2-Tone, 3rd Order IMD Intercept** plot is found in the **Typical Performance Characteristics** section. The output power level is taken at the load. Third-order harmonic distortion is calculated with the formula:
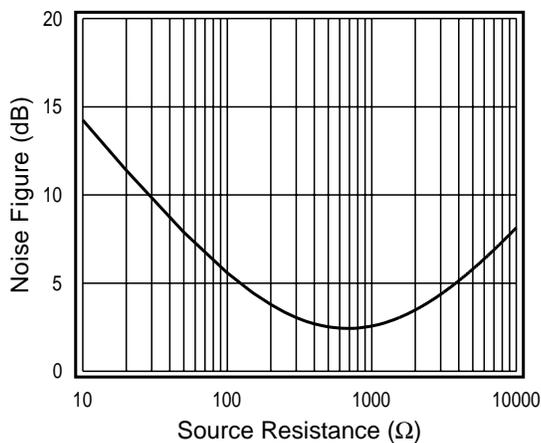
$HD3^{rd} = 2 \times (IP3_O - P_O)$

where:

• $IP3_O$ = Third-order output intercept, dBm at the load.

• P_O = output power level, dBm at the load.

• $HD3^{rd}$ = Third-order distortion from the fundamental, –dBc.

Application Division (Continued)

$$e^2{}_{R_f} = 4kTR_s \cdot \left(\frac{R_s}{R_{in} \cdot (1+G)} \right)$$

The noise of a simple input matching resistor connected to ground can be calculated by setting G to 0 in this equation. Thus, this circuit reduces the thermal noise power produced by the matching resistor by a factor of (1+G).

Rectifier Circuit

Wide bandwidth rectifier circuits have many applications. *Figure 10* shows a 200MHz wideband full-wave rectifier circuit using a CLC449 and a CLC522 amplifier. Schottky or PIN diodes are used for D_1 and D_2. They produce an active half-wave rectifier whose signals are taken at the feedback diode connection. The CLC522 takes the difference of the two half-wave rectified signals, producing a full-wave rectifier. The CLC522 is used at a gain of 5 to achieve high differential bandwidth. For best high frequency performance, maintain low parasitic capacitance from the diodes D_1 and D_2 to ground, and from the input of the CLC522 to ground.
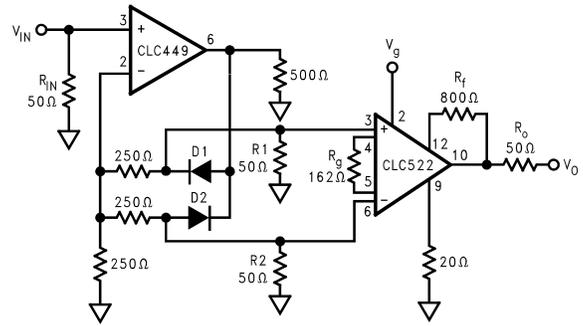
DS012715-44

FIGURE 10. Full-Wave Rectifier

Flash A/D Application

The Typical Application circuit on the front page shows the CLC449 driving a flash A/D. Flash A/D's require fast settling, low distortion, low noise and wide bandwidth to achieve high Effective Number of Bits and Spurious Free Dynamic Range (SFDR).

This circuit connects a CLC449 to a TDA8716, 8-bit, 120MHz Flash Converter. The input capacitance for this converter is typically 13pF plus layout capacitace. From the **R_s and Settling Time vs. C_L** plot in the **Typical Performance Characteristics** section, select a series resistor (R_s) of 55Ω. Place R_s in series with the output of the CLC449 to achieve settling to 0.1% in approximately 11ns.

Keep the amplifier noise seen at the A/D input at least 3dB lower than the A/D's noise, to avoid degrading A/D noise performace.

Physical Dimensions inches (millimeters) unless otherwise noted

0.189 − 0.197
(4.800 − 5.004)

0.228 − 0.244
(5.791 − 6.198)

0.010 MAX
(0.254)

LEAD NO. 1
IDENT

30°
TYP

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020 × 45°
(0.254 − 0.508)

8° MAX TYP
ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M08A (REV H)
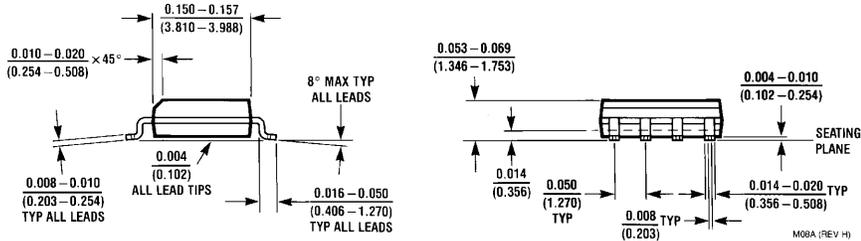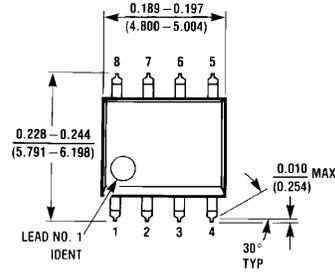
8-Pin SOIC
NS Package Number M08A

0.373 − 0.400
(9.474 − 10.16)

0.090
(2.286)

0.092
(2.337) DIA

PIN NO. 1 IDENT

OPTION 1

0.250 ± 0.005
(6.35 ± 0.127)

0.032 ± 0.005
(0.813 ± 0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280 MIN
(7.112)

0.030 MAX
(0.762)

0.300 − 0.320
(7.62 − 8.128)

95° ± 5°

0.009 − 0.015
(0.229 − 0.381)

0.125
(3.175)
DIA
NOM

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.045 ± 0.015
(1.143 ± 0.381)

0.050
(1.270)

0.040 TYP
(1.016)

20° ± 1°

0.065
(1.651)

0.039
(0.991)

0.130 ± 0.005
(3.302 ± 0.127)

0.125 − 0.140
(3.175 − 3.556)

90° ± 4°
TYP

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

0.060
(1.524)

0.145 − 0.200
(3.683 − 5.080)

0.020
(0.508)
MIN

N08E (REV F)

8-Pin MDIP
NS Package Number N08E

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.