

CLC115QML

Quad, Closed-Loop Monolithic Buffer

General Description

The CLC115 is a high performance, closed-loop quad buffer designed for high density applications requiring a low-cost-per-channel solution to buffering high-frequency signals. The CLC115's high performance includes a 700MHz small signal bandwidth (0.5V_{PP}) and a 2700V/μs slew rate while requiring only 11mA quiescent current per channel. Signal fidelity is maintained with low harmonic distortion (-62dBc 2nd and 3rd harmonics at 20MHz), and channel separation (60dB crosstalk at 10MHz).

Featuring a unique closed-loop design, the CLC115 offers true unity-gain stability and very low output impedance plus a 60mA per channel output drive capability. The CLC115 is ideally suited for buffering video signals with its 0.08%/0.04° differential gain and phase performance at 3.58MHz. Applications such as analog multiplexing and high-speed A/D converters will benefit from the CLC115's high signal fidelity.

The CLC115 offers a low-cost-per-channel solution to high-speed buffering with four high-performance, closed-loop buffers integrated in one 14-pin package.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures.

Features

- Closed-loop quad buffer
- 700MHz small-signal bandwidth
- 2700V/μs slew rate
- 0.08%/0.04° differential gain/phase
- 60dB channel isolation (10MHz)
- -62dBc 2nd and 3rd harmonics at 20MHz
- 60mA current output per channel

Applications

- Multi-channel video distribution
- Video switching buffers
- High-speed analog multiplexing
- Channelized EW
- High-density buffering
- Instrumentation amps
- Active filters

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DESCRIPTION
CLC115AJ-QML		J14A	14LD Cerdip

Absolute Maximum Ratings (Note 1)

Supply Voltage	$\pm 7V_{DC}$
Output Current	$\pm 96mA$
Thermal Resistance (Note 2)	
θ_{JA}	$75^{\circ}C/W$
θ_{JC}	$28^{\circ}C/W$
Junction Temperature	$+175^{\circ}C$
Operating Temperature	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
Storage Temperature	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Temperature (Soldering 10 seconds)	$+300^{\circ}C$

Recommended Operating Conditions

Supply Voltage	$\pm 5V_{DC}$
Ambient Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

CLC115 Electrical Characteristics

DC Parameters

(The following conditions apply, unless otherwise specified.) $R_{LOAD} = 100W$, $V_{CC} = \pm 5V$, $-55^{\circ}C < T_A < =125^{\circ}C$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
I_{BN}	Input Bias Current Non-inverting			-20	20	μA	1, 2
				-35	35	μA	3
V_{OS}	Output Offset Voltage			-9.0	9.0	mV	1, 2
				-17	17	mV	3
I_{CC}	Supply Current				61.0	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio			48		dB	1
				46		dB	2
				44		dB	3

CLC115 Electrical Characteristics

AC Parameters

(The following conditions apply, unless otherwise specified.) $R_{LOAD} = 100W$, $V_{CC} = \pm 5V$, $-55^{\circ}C < T_A < =125^{\circ}C$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
GFPH	Gain Flatness Peaking	30 to 200MHz			1.15	dB	4, 5
					1.4	dB	6
GFR	Gain Flatness Rolloff	30 to 200MHz		-0.5		dB	4, 5, 6
HD ₂	2 _{ND} Harmonic Distortion	2V _{PP} at 20MHz			-47	dB _C	4, 5
					-45	dB _C	6
HD ₃	3 _{RD} Harmonic Distortion	2V _{PP} at 20MHz			-53	dB _C	4, 6
					-50	dB _C	5

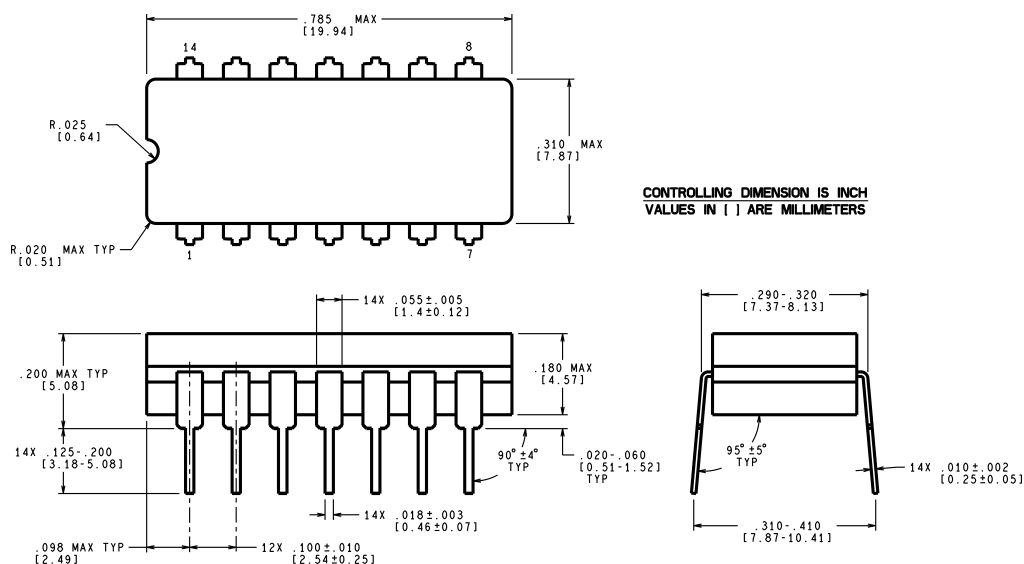
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Revision History Section

Date Released	Revision	Section	Originator	Changes
7/01/05	A	New Data Sheet, Initial Release	R. Malone	New Data Sheet, Initial Release

Physical Dimensions inches (millimeters) unless otherwise noted



J14A (Rev J)

Ceramic Dual-In-Line Package (J)
NS Package Number J14A

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