National Semiconductor

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CLC-DRCS7-PCASM
DRCS7 Evaluation Board User's Guide

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Overview

The Diversity Receiver Chipset (DRCS) is an IF sampling receiver optimized for GSM/EDGE systems. It provides the extreme dynamic range required for EDGE through a novel AGC-based architecture. The chipset consists of two CLC5526 Digital Variable Gain Amplifiers (DVGAs), two CLC5957 Analog-to-Digital Converters (ADCs), and one CLC5902 Dual Digital Tuner/AGC.

The DRCS7 Evaluation Board (CLC-DRCS7-PCASM) supports complete evaluation of the Diversity Receiver Chipset (DRCS). Configuration of the Digital Tuner/AGC is controlled by a COP8 micro-controller. Several useful configurations can be directly loaded by the COP8 or specialized configurations can be created and loaded with the provided DRCS Control Panel software (*drcscp.exe*).

A Data Capture Board (CLC-CAPT-PCASM) and accompanying software (*capture.exe*) are available for use with the DRCS7 Evaluation Board. The Capture Board enables the user to capture and transfer data from the DRCS7 Evaluation Board into a file on a PC. Matlab® script files are provided to assist in data analysis.

Figure 1 shows a functional block diagram of the DRCS. The DVGA controls the ADC's input level to expand the dynamic range. The ADC sub-samples the input and feeds the digitized IF to the CLC5902. The CLC5902 mixes the IF with a digital oscillator, removes the DVGA gain steps, and filters the result. A final output of quadrature baseband signals is provided in both serial and parallel formats.

Required Evaluation Items

- DRCS7 Board (CLC-DRCS7-PCASM)
- +5V/1A power supply
- Signal generator
- DRCS Control Panel software
- PC running Windows® 95/98/NT
- Matlab® software or other data analysis software
- One PC serial port

Suggested Evaluation Items

- Data Capture Board (CLC-CAPT-PCASM)
- Data Capture Board software
- Second PC serial port

Reference Documents

- CLC5957 data sheet
- CLC5526 data sheet
- CLC5902 data sheet
- Data Capture Board User's Guide
- Evaluation Board Interoperability User's Guide

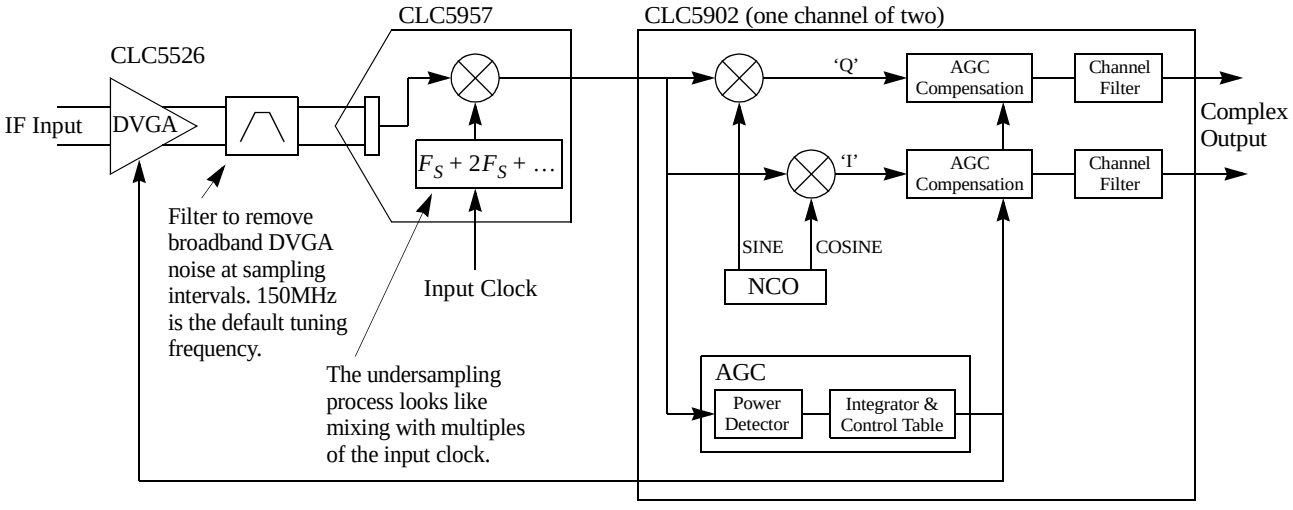

Figure 1 Diversity Receiver Chipset Single Channel Functional Block Diagram

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Key Concepts

Definition of Terms

Full Scale - The maximum digital output level (+/-2^{11} or +2047/-2048 for 12-bit ADCs). Full scale for the CLC5902 can be set for 8, 16, 24, or 32 bits. The DRCS7 Board defaults to 24-bit outputs. This value is often related back to the corresponding analog input voltage (2Vpp differential for the CLC5957).

Fundamental - Desired input signal shown on an FFT plot.

Tone - A signal shown on the FFT plot. The fundamental will usually be the tone with the largest amplitude on the FFT plot.

dBc - dB relative to carrier (or fundamental) level.

dBFS - dB relative to the ADC or DRCS Full-Scale output level.

Pinput - Magnitude of the largest signal found in the FFT. Measured in dBFS since it is relative to the full scale output value. The DRCS and ADC FFT routines include variables to specify the full scale value appropriately.

SFDR - Spurious Free Dynamic Range. The difference between the fundamental amplitude and the next largest signal on the FFT (excluding DC). Includes all distortion terms. Typically in dBc.

Integrated Noise Floor - The sum of the FFT bins excluding DC, the fundamental, and the first 50 harmonics. Measured in dBFS. The excluded information is replaced by the average noise floor level.

SNR - Signal to Noise Ratio. The sum of the FFT bins excluding DC, the fundamental, and the first 50 harmonics. Typically in dBc. Add back the number of dB below full scale (Pinput) to get the noise floor or SNR in dBFS.

ENOB - Effective number of bits. (Noise floor - 1.76) / 6.02. Each bit represents 6.02dB in the analog domain. This is of interest since a perfect 12 bit ADC would provide a 74dB noise floor. Real ADC performance falls short of this ideal and ENOB is a measure of the real performance.

SINAD - Signal-to-noise + Distortion. The sum of the FFT bins excluding only DC and the fundamental. This metric approximates the root sum of squares of both SNR and SFDR. For example, if SNR=52.63dBc and SFDR=57.4dBc then SINAD will be about 52.6dBc dominated by the SNR.

THD - The sum of all harmonic energy relative to full scale. Any non-harmonic spurs will be excluded.

Sub-Sampling

The process of sub-sampling can be thought of as mixing the input signal with the sampling frequency and its harmonics. This means that many signals can be mixed down to DC and their original frequency can no longer be determined. For example, if the sample frequency (F_S) is 52MHz then inputs at 6MHz, 52-6=46, 52+6=58, 98, 110, 150, 162,... would all mix down to 6MHz. The IF SAW filter will only allow a single frequency to be sampled by the ADC so the original input or carrier frequency is known.

Sub-sampling cannot be used if the original input frequency must be determined at the ADC output without an IF filter. This is because the Nyquist criteria is violated. Sub-sampling still proves useful if there is no need to determine the carrier frequency at the ADC output. This is true for the DRCS since the receiver only needs to recover

the information on the carrier and not the carrier itself. Nyquist is not violated for the required information bandwidth of 200kHz for GSM/EDGE systems.

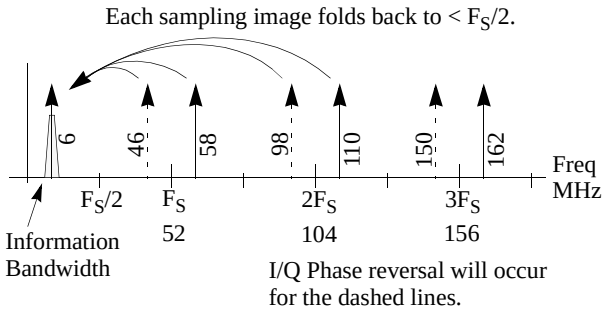


Figure 2 Sub-Sampling

Processing Gain

ADC noise performance is typically limited by thermal noise. When an ADC is specified the noise bandwidth is normally defined as the Nyquist bandwidth. This leads to an integrated noisefloor measurement of -65dB relative to full-scale (dBFS) in a 26MHz bandwidth for the CLC5957 at 52MSPS. When the CLC5957 output is filtered by the CLC5902 a much narrower bandwidth is provided at the output. This filtering process provides noise processing gain (PG) as a function of the bandwidth reduction. For the DRCS7 Evaluation Board the sample rate (F_S) is 52MSPS and the output bandwidth defaults to roughly 200kHz (±100kHz) so the processing gain should be:

$$PG = 10 \times \log \frac{BW_{OUT}}{F_S/2}$$

$$PG = 10 \times \log \frac{200kHz}{26MHz}$$

$$PG = -21.1dB$$

EQ. 1

as shown in Figure 3.

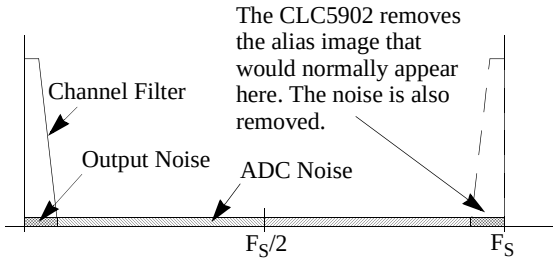


Figure 3 Processing Gain

The CLC5902 filters provide an additional 3dB of processing gain because they remove the alias image and noise near F_S. The processing gain equations then become:

$$PG = 10 \times \log \frac{BW_{OUT}}{F_S}$$

$$PG = 10 \times \log \frac{200kHz}{52MHz}$$

$$PG = -24.1dB$$

EQ. 2

The ADC output noise in a 200kHz bandwidth (after filtering by the CLC5902) will then become:

-65dBFS + (-24.1dB) = -79.1dBFS **EQ. 3**

General Description

As seen in Figure 4, the DRCS7 Board accepts analog IF inputs on a pair of SMA connectors and processes these into baseband digital waveforms. There are several analog components that condition the signal prior to sampling with a pair of ADCs. The most important of these is the DVGA, the gain control element of an AGC loop. The sampled signals are applied to the CLC5902 which performs a final mix to baseband, digitally filters the waveforms, and decimates to a lower output sample rate. An automatic gain control (AGC) processor in the CLC5902

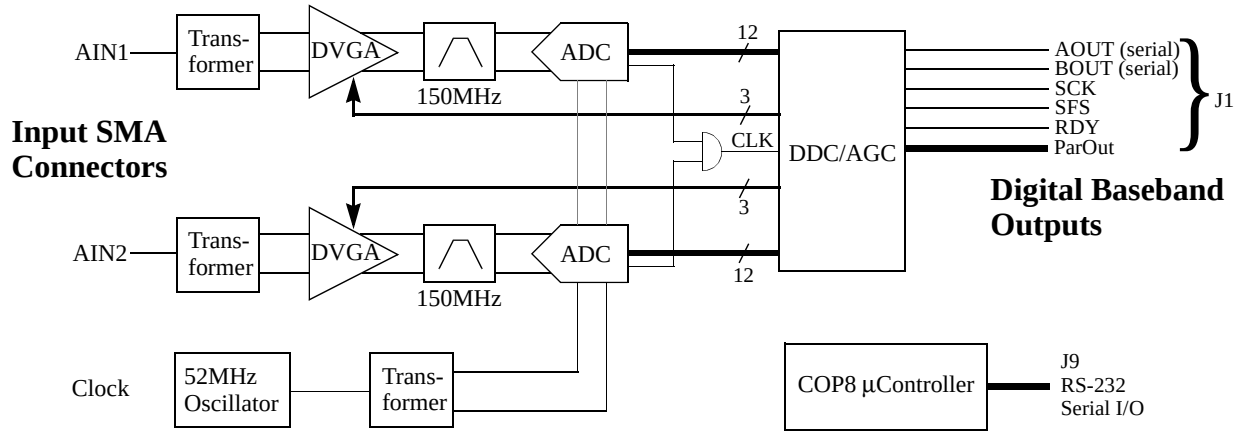


Figure 4 CLC-DRCS7-PCASM Block Diagram

directs the DVGAs to extend the dynamic range of the analog signal paths.

Note

The operation of the AGC will be transparent at the DRCS output since the CLC5902 includes circuitry to digitally compensate for the DVGA gain steps.

The DRCS7 Board is factory configured for an IF of 150MHz, a sampling frequency (F_{CK}) of 52MSPS, and an overall decimation of 192. This yields an output sample rate of 270.8KSPS which is suitable for GSM/EDGE systems. The CLC5902 features a high degree of programmability. Key parameters such as mixer frequency, decimation ratio, filter shape, AGC operation, etc. can be configured by the user.

DRCS7 Evaluation Board I/Os

Power

The DRCS7 Board requires +5V and ground which are supplied through J1. The Connector Adapter (CLC-ADAPT1-PCASM) mates with J1 and includes a terminal block for power connections. The Data Capture Board also includes a terminal block for power connections which feed through the Connector Adapter. A +5V/1A power supply is sufficient for the DRCS7 Board with the Data Capture Board. The terminal block may include a -5V position (VEE) but it is not required for the DRCS.

Clock Input

The DRCS7 Board includes a 52MHz crystal oscillator module so that an external clock source is not required. If a different sample rate is desired a +16dBm sinewave or a TTL level squarewave may be applied to the CLK input SMA. The crystal oscillator module should be removed from its socket when an external clock is used. For optimal performance a low jitter low phase noise clock must be provided (i.e. HP8644B or R&S SME-03).

The CLC5957 converts the differential input clock to a TTL clock suitable for driving the CLC5902 CK input.

At high input levels the CLC5957 ADC's SNR is limited by clock jitter. In a DRCS-based receiver the effects of clock jitter can be reduced by operating the AGC at a lower threshold. As the input signal level to the ADC decreases the degradation of the ADC's SNR will also decrease.

SNR degradation due to clock jitter only happens when the input signal is near full-scale. This large input signal will typically mask any SNR degradation that may occur. This would not be the case if more than one carrier was digitized.

IF Signal Inputs

The AIN1 and AIN2 SMA connectors accept IF signals up to +20dBm and below -100dBm. Always start with a signal at or below 0dBm, reset the DRCS7 Board, then increase the signal if desired. This allows the AGC loop to control the DVGA properly as it will in a receiver. When measuring very small signals consider using an external attenuator in addition to the level control in the signal generator. Some signal generators do not perform well at very low output levels. For optimal performance a low jitter low phase noise signal source must be used (i.e. HP8644B or R&S SME-03).

CLC5902 Serial Outputs

The default setup of the DRCS7 Board is PACKED=1, MUX_MODE=1, and FORMAT=2. These settings provide a 24-bit serial output word, a frame sync output pulse once for each I/Q pair, and the outputs for channel A and B are muxed onto the single output pin AOUT as shown in Figure 5.

Note

This is the format expected by the Data Capture Board.

The serial outputs and control signals are available at the Futurebus+ connector J1. This connector mates with the Data Capture Board through an adapter. These signals are also accessible on the DSP header for simple connection to a DSP.

In some cases it may be desirable to remove the second SFS pulse so that channel A and B can be identified. An AND gate can be placed at U12 which allows the RDY signal to mask the second SFS pulse. Figure 6 provides detailed timing information for this option.

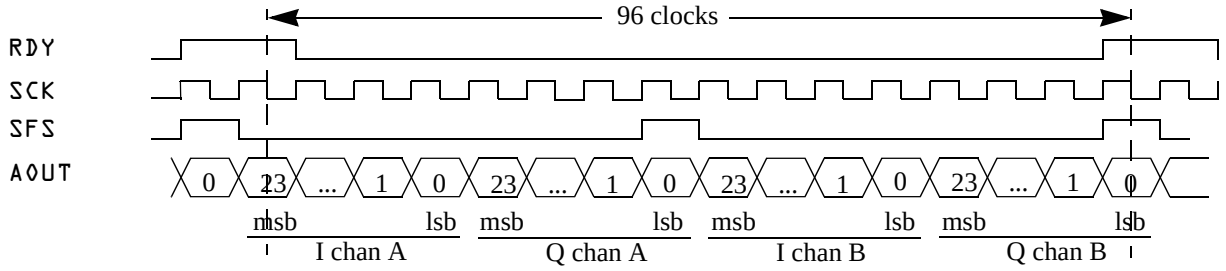


Figure 5 DRCS7 Default Serial Port Format

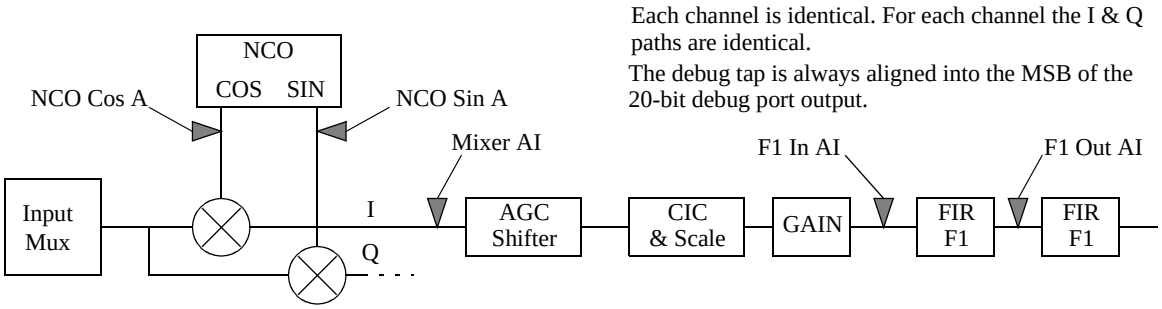
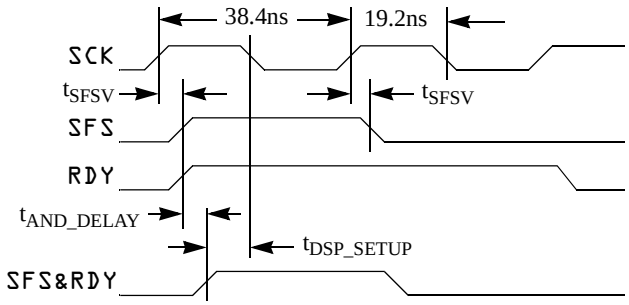


Figure 7 CLC5902 Debug Port Access Taps



$t_{SFSV} + t_{AND\_DELAY} + t_{DSP\_SETUP} \leq 19.2ns$

CK = 52MHz, SCK = CK/2

SCK_POL = RDY_POL = SFS_POL = 0

t_{SFSV} = 7ns max from CLC5902 datasheet

Figure 6 CLC5902 Serial Port Timing

Note

The trace from pin 2 to pin 4 of U12 must be cut when U12 is used.

The default serial output configuration is compatible with the TI TMS320C54X serial input. To interface to the 'C54X, set the DSP serial port in continuous mode (FSM bit set to 0) with frame ignore enabled (FIG bit set to 1). In this mode the 24-bit words may be read as 3 groups of 8 bits. The overall input stream of four 24-bit words is read as twelve 8-bit words for later reassembly by the DSP.

Additional serial port modes are discussed in the CLC5902 datasheet.

CLC5902 Parallel Output

The CLC5902 parallel output port is available on J1. It is a 16-bit port which can be mapped into the address space of a DSP. Each output component (AI, AQ, BI, & BQ) is allocated 2 registers of 16 bits. In 8-bit or 16-bit mode only a single register for each component needs to be read.

To access the data place the proper address on the three POUT_SEL lines and enable the outputs with POUT_EN. The RDY signal can be used as an interrupt to indicate new data is ready. Complete details are provided in the CLC5902 datasheet.

To facilitate testing of the parallel outputs SW1 can be used to force the state of POUT_SEL and POUT_EN.

Note

All DRCS7 Board SW1 positions must be 'OFF' if the Data Capture Board is used for parallel data capture.

CLC5902 Debug Output

In some cases it may be desirable to look at signals internal to the CLC5902. The CLC5902 debug port is tied to an internal 20-bit bus which can tap into the internal nodes shown in Figure 7. When in debug mode the DSP serial port pins are reconfigured and the serial port is no longer functional. SCK is used to clock out the debug data at the proper rate. Additional information on the debug port is provided in the CLC5902 datasheet.

The debug port can be used to observe the ADC outputs prior to processing by the CLC5902. This can be done by selecting the mixer output tap for the I component and setting the NCO frequency to zero. This setup is included in the default COP8 options.

COP8 RS-232 Serial Interface

The CLC5902 can be set to several default configurations by the COP8 micro-controller. To support more flexibility in evaluation the CLC5902 may also be completely reconfigured via an RS-232 serial port. The DRCS Control Panel software running on a PC sends commands to the COP8 serial port. The COP8 interprets these commands and programs the CLC5902 registers as required.

DRCS7 Block Interfaces

DVGA to ADC Interface (LC Noise Filter)

While the IF SAW filter allows only the desired signal to be sampled, the DVGA introduces broad-band noise at the ADC input. A simple noise filter between the DVGA and ADC removes this noise. Failure to attenuate noise from the DVGA appearing at the ADC sampling image frequencies will degrade the system performance. Figure 8 shows the response of the noise filter with respect to the sampling images.

The nominal component values for the filter provide a center frequency of 150MHz, a 3dB bandwidth of 18MHz, and an insertion loss of 0.7dB. Assuming an ADC sample rate of 52MSPS, the filter provides about 4dB of attenuation at the closest image frequency which is at 162MHz (Figure 8). More attenuation is possible by increasing the Q of the filter, but this would make the center frequency tolerance more critical and increase the group delay through the filter (the stability of the AGC loop is reduced by large group delays). More attenuation will also be achieved if the IF is moved further away from 156MHz.

To change the IF frequency of the DRCS7 Board, the noise filter components must be changed. The equations below pertain to Figure 9 and provide a means of computing the new values:

$$\omega_c = \frac{1}{\sqrt{L_1 C_T}} \qquad \textbf{EQ. 4}$$

$$\omega_{BW} = \frac{1}{R_T C_T} \qquad \textbf{EQ. 5}$$

$$G_{LC} = 1 + \frac{R_T}{Q_L} \cdot \sqrt{\frac{C_T}{L_1}} \qquad \textbf{EQ. 6}$$

$$C_T = C_{93}/2 + C_{99} + 1.5pF \qquad \textbf{EQ. 7}$$

In these equations, $C_{93} = C_{94}$, $R_T = 600 \parallel 1K = 375\Omega$, G_{LC} is the filter gain at ω_c, and Q_L is the quality factor of the inductor at ω_c.

In addition to setting the center frequency of the filter, capacitors C_{93} and C_{94} absorb the transient current that is sourced out of the ADC coincident with the sampling instant. It is recommended that C_{93} and C_{94} be no less than 20pF.

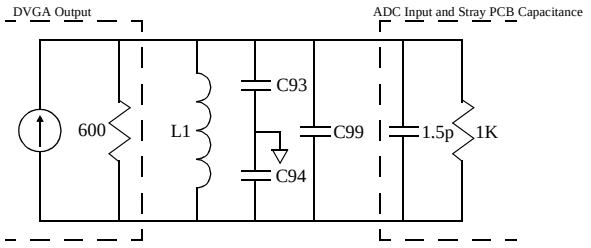


Figure 9 Noise filter components for AIN1.

It is easy to calculate a new set of filter components using a spreadsheet program set up as follows:

	A	B
1	C93, C94	0.00000000002
2	C99	0.000000000001
3	Parasitic	0.0000000000015
4		
5	Ct	=B1/2+B2+B3
6		
7	L1	0.000000033
8		
9	Fcenter	=1/(2*3.14*(B7*B5)^0.5)

Start by selecting an inductor with a relatively high Q (30-40). Next, iteratively try available capacitor values for C_{93} and C_{94}. Use C_{99} to fine-tune the result. This example uses 20pF and 1pF capacitors with a 33nH inductor for a center frequency of 247.9MHz. Once the final PCB is available the center frequency should be checked to verify the effects of PCB parasitics.

The frequency response of the noise filter can be checked at spot frequencies by observing either the CLC5902 Mixer AI or BI outputs in debug mode with the NCO set to 0 frequency and 0 phase. The tuning can be verified at the CLC5902 output by sweeping both the input frequency and the CLC5902 tuning so that they track. The test signal must be input after the IF SAW to use this method.

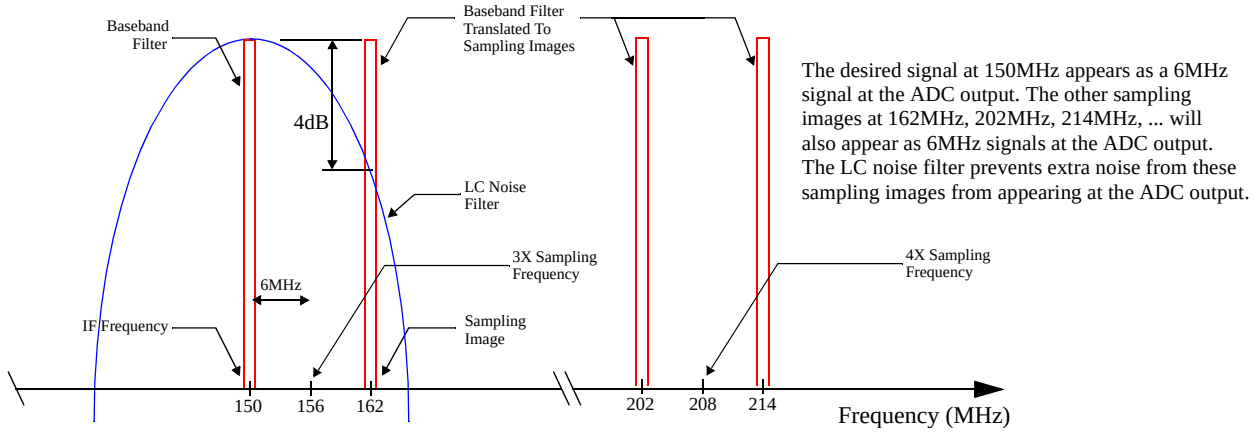


Figure 8 Illustration of the need for noise filter attenuation at the sampling images.

ADC to CLC5902 Interface

The CLC5957 ADC outputs are current limited (DATA~2.5mA, DAV~5mA) to prevent crosstalk back to the analog input. For this reason it is important to minimize the parasitic capacitance on the data outputs and the DAV signal. Excessive capacitance will degrade the ADC's SNR performance and may cause errors in the output data. A target for capacitive loading should be 5-7pF. To meet this target all power and ground planes should be removed below the ADC output pins, traces, and CLC5902 input pins. The area where the power and ground planes are removed should be the point where analog and digital planes are split. The included PCB layout on page 28 shows how this can be done.

Clocking the DRCS

When providing a clock signal for the DRCS several constraints must be observed:

1. The CLC5957 ENCODE specifications must be met,
2. The CLC5902 CK specifications must be met, and
3. The CLC5902 data input setup and hold times must be met.

The CLC5957 and CLC5902 datasheets contain all the timing parameters required to verify these conditions. Now, using the datasheet specifications, consider each of the above constraints.

CLC5957 ENCODE Requirements:

The CLC5957 ENCODE specifications require that the ENCODE signal always be high (t_P) for at least 7.1ns and low (t_M) for at least 7.1ns. The maximum time for t_P and t_M is limited by the minimum conversion rate. This requires that $1/(t_P + t_M)$ never be less than 10MHz.

With a clock rate of 52MHz (as used in the DRCS for GSM/EDGE systems) the period is 19.23ns. In this case, if t_P is reduced to 7.1ns then t_M will be 19.23ns - 7.1ns or 12.13ns. This corresponds to an acceptable duty cycle variation of 37%/63%.

CLC5902 CK Requirements:

The CLC5902 is specified to operate with a clock up to 52MHz with up to 40%/60% duty cycle variation.

CLC5902 Input Setup and Hold Requirements:

In the DRCS, the CLC5902 must be driven by two different CLC5957 ADCs. This can be accomplished by combining the DAV signals with a fast AND gate or ignoring the DAV signals and clocking the CLC5902 with an inverted version of ENCODE.

Designs with a square wave ENCODE clock normally should not use the DAV signals. When the two DAV signals are combined with an AND gate, the CLC5902 input clock (CK) duty cycle can be affected. If the duty cycle is further skewed by changes in the ENCODE clock duty cycle, the data input setup (t_{SU}) and hold (t_{HD}) times may be violated. Bypassing the CLC5957 clock buffers can eliminate setup and hold dependence on clock duty cycle.

Combining the DAV signals with an AND gate is appropriate when a clean sine wave clock is available. The sine wave will have a nearly perfect 50% duty cycle which will be converted to a square wave by the CLC5957.

Both implementations will provide better SNR performance if the CLC5957 ENCODE inputs are driven differentially. Driving ENCODE with a single-ended clock can cause common-mode noise to appear as clock jitter, possibly degrading the SNR.

ANDing the DAV Signals

When the CLC5957 DAV signals are to be used, they should be ANDed together to drive the CLC5902 CK input. This AND gate is required to provide proper operation in the event that one CLC5957 has less propagation delay than the other. Figure 10 shows detailed timing information for the ADC to CLC5902 clock interface with the AND gate. This is the approach used on the DRCS7 Evaluation Board as shown by the schematics in Figure 38, Figure 39, and Figure 40. Table 1 summarizes the parameters from the CLC5957 and CLC5902 datasheets.

The objective of the timing diagram in Figure 10 is to determine the allowable range for the AND gate delay, t_{AR}. This parameter may be calculated as shown in Equation 8.

$$t_{SU} - t_{S2} \le \boldsymbol{t_{AR}} \le t_{DAV1} + t_{H1} - t_{HD} - t_{DAV2} \qquad \textbf{EQ. 8}$$

Parameter	Symbol	Timing[a]
Pulse width high, CLC5957 ENCODE	t_P	9.615ns
Pulse width low, CLC5957 ENCODE	t_M	9.615ns
Rising ENCODE to rising DAV, CLC5957	t_{DAV1}	8.5ns
Rising ENCODE to rising DAV, CLC5957	t_{DAV2}	10.9ns
DATA setup to rising DAV, CLC5957	t_{S1}, t_{S2}	7.215ns
DATA hold after rising DAV, CLC5957	t_{H1}, t_{H2}	8.015ns
Falling ENCODE to DATA invalid, CLC5957	t_{DNV}	7.0ns
Falling ENCODE to DATA valid, CLC5957	t_{DGV}	13.0ns
AIBIN setup to rising CK, CLC5902	t_{SU}	7.0ns
AIBIN hold after rising CK, CLC5902	t_{HD}	3.0ns
AND gate rising edge delay[b]	t_{AR}	-0.215ns to 2.615ns
AND gate falling edge delay[c]	t_{AF}	t_{AR}

Table 1 ADC to CLC5902 Timing Summary

a. Clock is 52MHz, values are min/max from the CLC5957 and CLC5902 datasheets. Datasheet numbers take precedence. These numbers are only presented for convenience.
b. Refer to Equation 8.
c. t_{AF} is not critical since the data is captured on the rising edge of CK.

The results in Table 1 indicate that an AND gate with delays between -0.215ns and 2.615ns should be used. The IDT74ALVC1G08DY has a propagation delay spec of 1.2ns to 2.9ns with a 50pF load. Since the load in this case will be less than 10pF this part will meet the requirements.

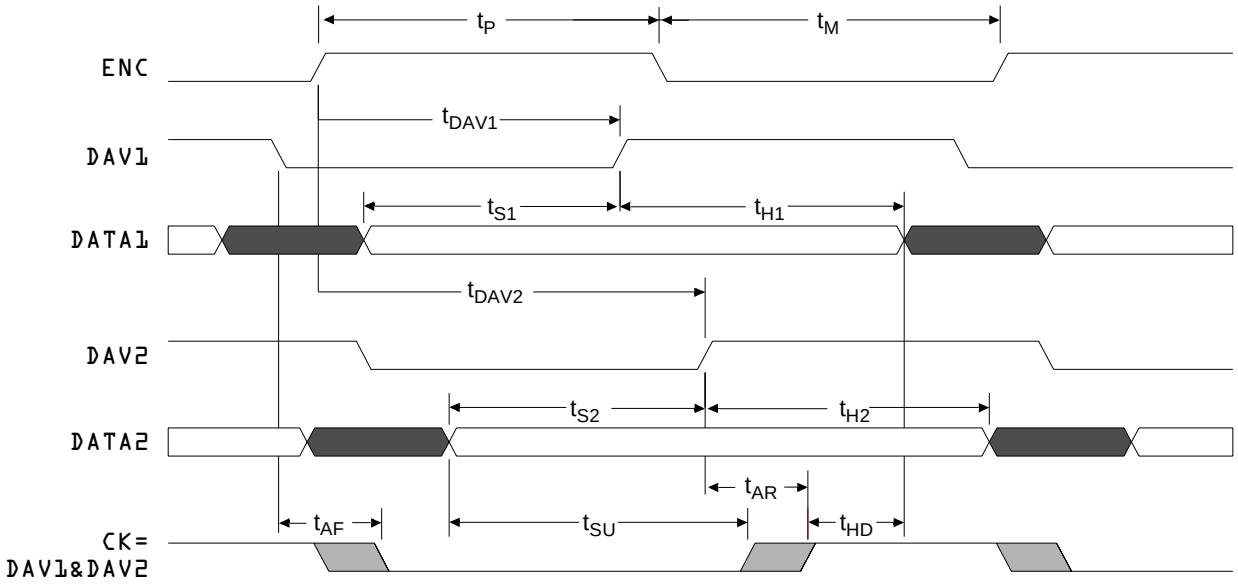


Figure 10 DRCS7 ADC to CLC5902 Clock Timing at 52MHz

If a maximum propagation delay of 2.5ns is assumed for the inverter with a 10pF load the clock duty cycle can only change a small amount. This condition allows the positive clock percentage to range from 49.5% to 60%.

In a real system, it is unlikely that the two CLC5957s will be skewed the maximum amount in opposite directions. Since the CLC5957 timing specifications are 3-sigma limits that means only 2.3 parts per thousand will be at the limit. The chance of having two parts with maximum opposite skew is 6.7 parts per million. The statistical chance of timing violations is further reduced by the inverter propagation delay distribution and the fact that most CLC5957s will be placed from the same wafer lot.

Ignoring the DAV Signals

When a square wave clock is available to drive ENCODE this same signal may be inverted to drive the CLC5902 CK input. When this is done, the duty cycle requirements are those set by the CLC5902. The CLC5902 data input setup and hold times will be independent of clock duty cycle since all timing is now relative to the falling edge of ENCODE. Figure 11 shows a single-ended clock circuit and Figure 12 shows the timing diagram for this approach.

For the IDT74ALVC1G04 inverter, t_{PDA} is the minimum propagation delay of 1.0ns and t_{PDB} is the maximum value of 3.2ns. In this case, the setup and hold times are:

$$t_{SU} = (t_P + t_M) - t_{DGV} + t_{PDA} \quad \textbf{EQ. 9}$$
$$= 19.23 - 13 + 1$$
$$= 7.23ns$$

$$t_{HD} = t_{DNV} - t_{PDB} \quad \textbf{EQ. 10}$$
$$= 7 - 3.2 = 3.8ns$$

The margins of 230ps and 800ps are not dependent on the clock duty cycle.

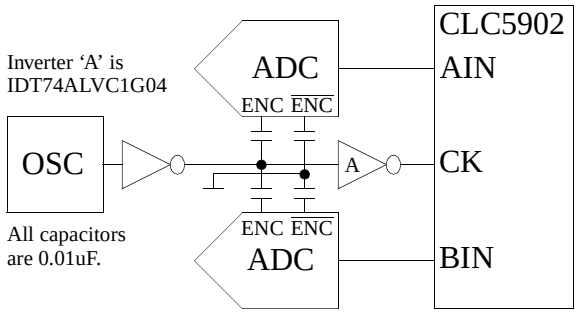


Figure 11 Single-Ended Clock Schematic

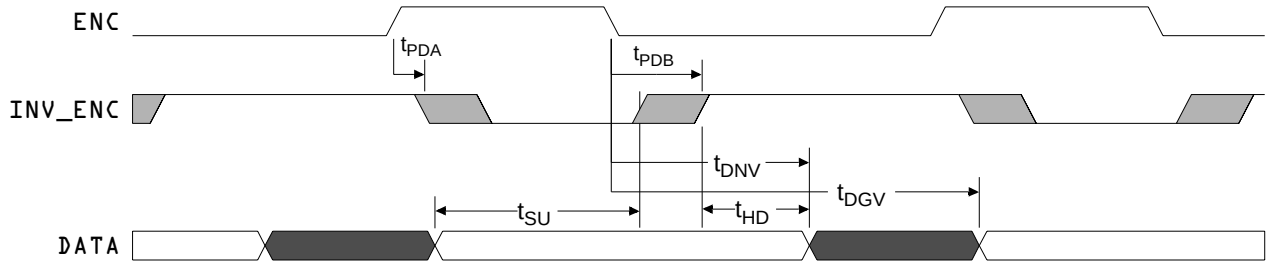


Figure 12 Inverted ENCODE Clock Timing at 52MHz

Quick Start

Initial performance measurements of the DRCS7 Evaluation Board can be obtained very quickly with the Data Capture Board and associated Matlab scripts. The equipment required to verify the DRCS performance includes:

1. DRCS7 Evaluation Board (CLC-DRCS7-PCASM),
2. Data Capture Board (CLC-CAPT-PCASM),
3. Connector Adapter (CLC-ADAPT1-PCASM, supplied with CLC-DRCS7-PCASM),
4. +5V/1A power supply,
5. Signal generator (150MHz sinewave, 0dBm),
6. PC with Windows 95, 98, or NT4 and Matlab.

To make an FFT plot of the DRCS output:

1. Install the Data Capture software from the included CDROM (this also installs the DRCS Control Panel software),
2. Connect the DRCS7 Evaluation Board to the Data Capture Board with the Connector Adapter in between,

Note

Remove the spare mating connector shipped with the connector adapter if attached.

3. Connect +5V and ground to J3 (the orange terminal block) on the Capture Board,
4. Verify that a 52MHz oscillator module is installed at Y2 (next to the `CLK` SMA connector),
5. Set all the DIP switches 'OFF" on both the DRCS7 Board and the Capture Board,
6. On the Capture Board place the *WCLK* jumper in the 'PIN120' position and the *VCCD* jumper in the '+5' position,
7. Connect a 0dBm 150MHz sinewave input signal to the `AIN1` SMA connector,
8. Connect the Capture Board J9 (serial port) to the PC serial port with the supplied cable,
9. Turn on the +5V supply,
10. Start the Capture software. The Capture Software Panel shown in Figure 13 will be displayed,

Figure 13 Capture Software Panel

11. Click the *right* mouse button over the Capture software panel (do not click over the 'Start' or '?' buttons), select 'Configure I/O' (shown in Figure 14), then select your COM port.

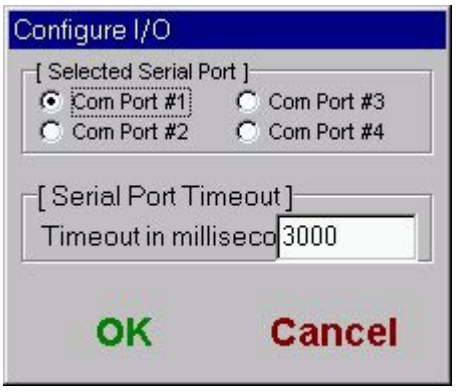


Figure 14 Capture I/O Dialog

To proceed the Capture Board must have power, a sample clock, and be connected to the proper COM port. LED1 on the Capture Board should be on. LED6 should be on about half as bright as LED1.

12. Click the right mouse button over the Capture software panel, select 'Configure Capture', then select the options shown in the 'Capture Configuration Dialog' (Figure 15).

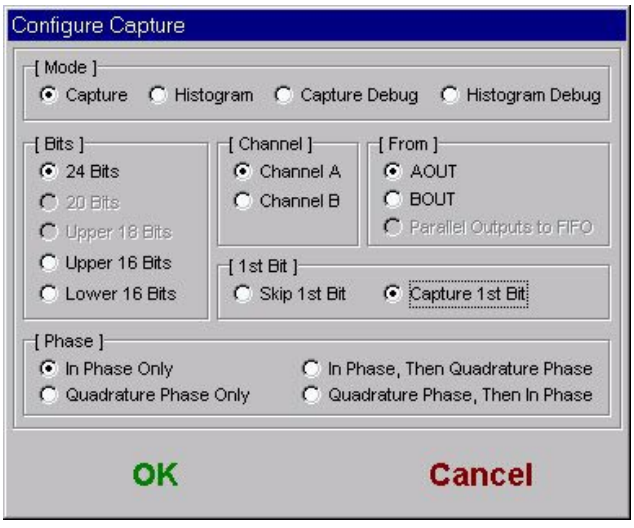


Figure 15 Capture Configuration Dialog, Serial Port

13. Now click 'Start' to capture a 32k sample record. The data will be saved in 'c:\temp\data.dat',
14. Start Matlab and add 'c:\nsc\mfiles' to the path,
15. Type 'analysis_menu' in the Matlab command window,
16. Click 'DRCS Serial' on the menu to plot an FFT (or run 'drcs_ser_fft.m' from the Matlab command line).

The resulting FFT should be similar to Figure 16, showing a single tone at about 50kHz. The measured Pinput should be about -20dB relative to full-scale (dBFS) with 0dBm at the SMA input connector.

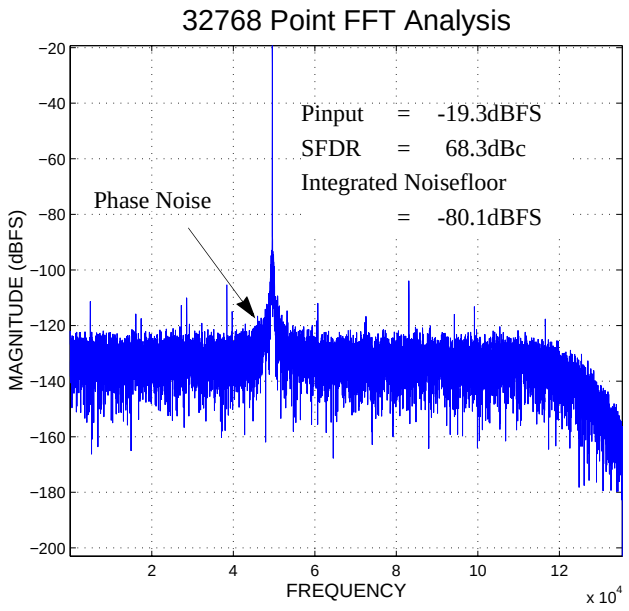


Figure 16 IF Input = 150MHz at 0dBm

Common Questions

1. What are the basic operating instructions for Matlab?

   The Matlab command window opens when Matlab is started. All Matlab commands can be directly typed into the command window or saved in a script file for repeated execution. Type '3+4' then hit enter to see Matlab display 'ans=7'. Use the menu to create a new script file (m-file): 'file->new->m-file'. Type '3+4' on line 1. Save this file as 'my_test.m' in the default location. Now type 'my_test' to see 'ans=7'. Now that my_test.m exists, simply type 'edit my_test' to load it in the editor. To repeat a command hit the up-arrow until the desired command is displayed then hit enter.

   When the DRCS & Capture software are installed all the m-files are placed in 'c:\nsc\mfiles' by default. This location should be added to the Matlab path. Use the path browser: 'file->set path'. Browse to 'c:\nsc\mfiles' then 'path->add to path' and exit the path browser. Now Matlab will be able to locate all the provided scripts.

   The command 'whos' will list all the variables and their sizes. 'Clear' will clear all the variables.

   To create a new plot type 'figure(1)' then plot the data to the figure with 'plot(data)'. Type 'zoom on, grid on' to enable zoom and draw a grid. Click and hold the left mouse button to draw a zoom box. Double-click the right mouse button to zoom full.

   Matlab includes a comprehensive set of help files. Type 'help' to get a list of available help files.

2. The tone in the FFT is not exactly 50kHz. Why?

   Since the 52MHz crystal oscillator is not locked to the signal generator, the tone in the FFT may not be exactly 50kHz. A second signal generator locked to the first can be used to clock the DRCS7 Board and remove the frequency error. Set the clock signal generator to 52MHz at +16dBm. Be sure to remove the crystal oscillator module from its socket.

3. The measured results are much worse than expected. Why?

   Observing the FFT plots in Figure 16 and Figure 17 (close-up) the tone at 50kHz may show some spreading near the noise floor. This is typically caused by a signal generator with poor phase noise performance. The phase noise will be translated into jitter which impacts the ADC sampling performance. These phase noise skirts can be so large that the measured data on the FFT plot is incorrect. An alternate FFT routine is provided to remove the effects of the phase noise by excluding the region near the fundamental tone. Click 'Alt DRCS Serial' (or run 'drcs_ser_fft_excl.m') to observe the change in both SFDR and the Integrated Noisefloor from Figure 16 to Figure 18. Editing the Matlab script 'drcs_ser_fft_excl.m' allows the exclusion region to be set to the desired value. It is ±2kHz by default.

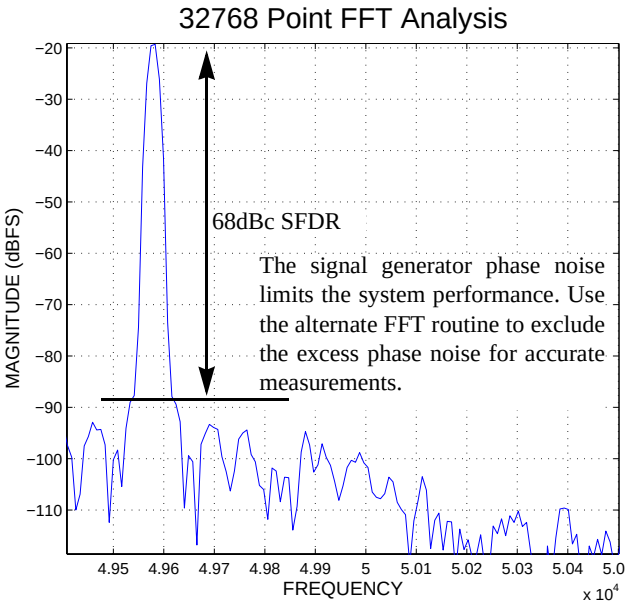


Figure 17 IF Input = 150MHz at 0dBm, Close-up

Figure 19 shows an example of an input signal with extremely poor phase noise performance.

4. Will the DRCS work with such a poor clock signal?

   Yes, this problem will not prevent the DRCS from easily recovering an EDGE signal. For full rate EDGE the 23dB C/I requirement is still met with margin. At lower signal levels jitter (from phase noise) does not significantly affect the ADC's performance. Take a look at the same signal at -80dBm (Figure 20) instead of 0dBm (Figure 19).

5. What happens when the filter coefficients are changed?

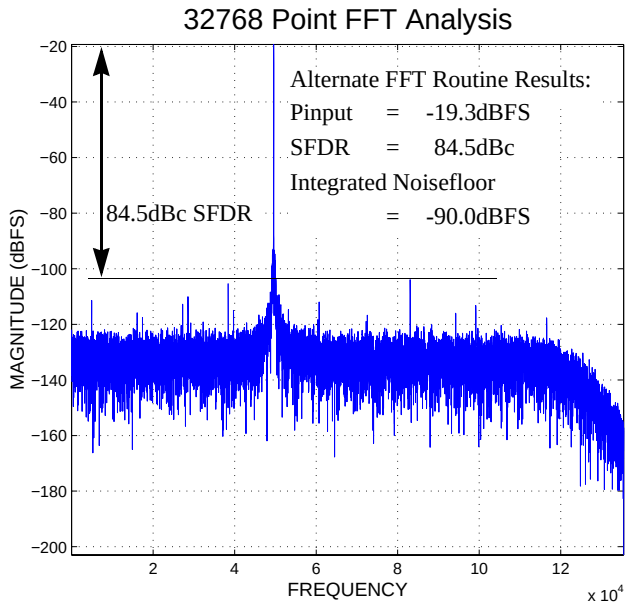


Figure 18 IF Input = 150MHz at 0dBm, Alternate FFT

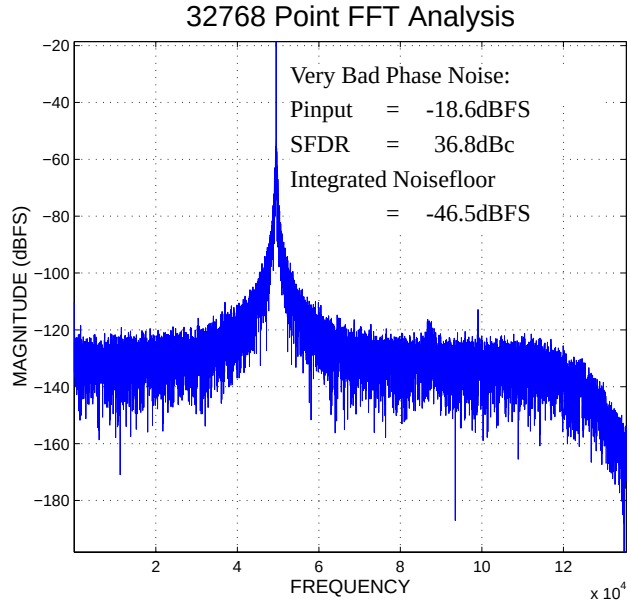


Figure 19 IF Input = 150MHz at 0dBm

The noisefloor in the FFT plots reflects the digital filter response. Changing the filter coefficients will change the shape of the noisefloor. Verify this by capturing a new data record as follows:

1. Connect the DRCS7 Board and Capture Board as described in the Quick Start section on page 9,
2. Turn on the power and apply 150MHz at -80dBm to the AIN1 connector,
3. Start Matlab and the Capture software,
4. Configure the Capture software as in Figure 15,
5. On the DRCS7 Board turn SW2-4 & SW2-8 ‘ON’,
6. Press the DRCS7 RESET button (LEDs should alternate),

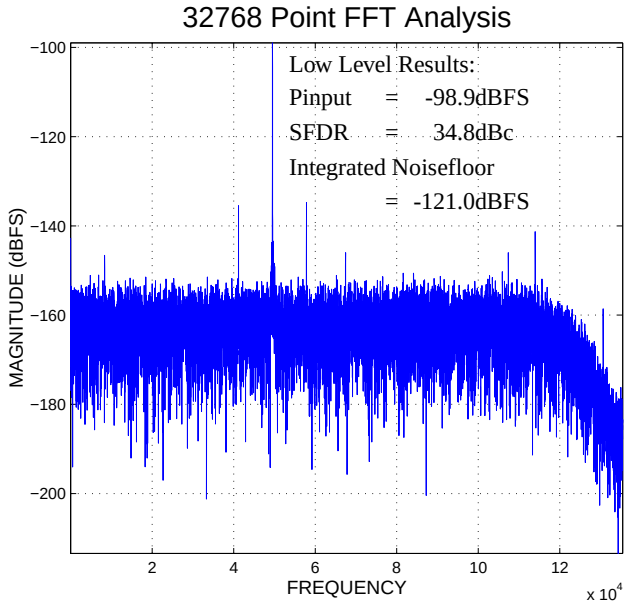


Figure 20 IF Input = 150MHz at -80dBm, Alternate FFT

7. Capture new data and plot an FFT.

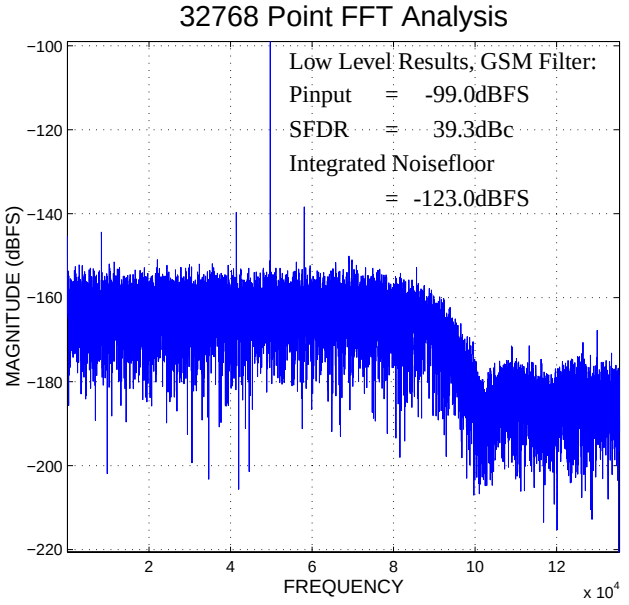


Figure 21 IF Input = 150MHz at -80dBm, Alternate FFT

Notice in Figure 21 that the integrated noisefloor improved by 2dB over Figure 20. This is because the slightly reduced bandwidth increased the processing gain (see the processing gain discussion on page 3).

6. How are the two sets of filter coefficients different?

The STD coefficients are optimized for a narrow transition-band (about 50kHz) with a flat pass-band and stop-band response. The stop-band rejection is about -80dBFS . The -3dBFS point is at 119kHz placing the filter bandwidth at 88% of the output sample rate (119kHz * 2)/270.833kHz.

The GSM coefficients are optimized to meet the GSM blocking test requirements. These filters sacrifice the narrow transition-band response of the STD filters for an ultimate stop-band rejection of -105dBFS beyond 800kHz. The -3dBFS point is at 87kHz placing the filter bandwidth at 64% of the output sample rate. The CLC5902 can meet the GSM-900 channel filter requirements totally in the digital domain with these filter coefficients.

7. Which filter coefficients should be used for GSM/EDGE systems?

   Since there is a SAW filter in front of the ADC either set of coefficients may be used. Using the STD set may make it easier to recover the signal since it provides a little wider bandwidth.

8. Why are the F1 coefficients included with the DRCS Control Panel software and the COP8 configuration file different than those in the CLC5902 datasheet?

   These coefficients have been uniformly scaled to create +4dB of gain. This compensates for the error in the SCALE and CIC filter combination when the CIC decimation is not a power of two. These new coefficients are optimized for GSM/EDGE systems.

9. What if SW2-4 and SW2-8 are not set the same?

   SW2-4 sets the decimation and SW2-8 selects the filter coefficients. Both must be either 'OFF' for the STD coefficients or 'ON' for the GSM coefficients. If they are not the same the tone in the FFT plot may show up at the wrong frequency or the rolloff from the filter will not be observed.

10. Why does the FFT plot look like Figure 22?

    In the Capture software, make sure that 'Capture 1st Bit' is checked. This option controls the deserialization of the DRCS output. For some combinations of output and decimation this setting may change. The DRCS Control Panel software will tell you how to set this option on the 'Output' tab (see page 15).

11. Why is the default tuning at 150.05MHz?

    An input signal at 150.0MHz can be easily generated by driving a 150MHz bandpass filter with a 50MHz crystal oscillator. Only the third harmonic is passed by the filter providing a low-jitter test signal. Tuning to 150.05MHz places the 150MHz signal at 50kHz in the DRCS output. Adding a variable attenuator allows a wide range of measurements to be made without an expensive synthesized signal generator.

12. Can the ADC output be observed?

    Yes. The CLC5902 debug output allows the complex mixer outputs to be observed. When the NCO is set to 0Hz the ADC output will be present at the I output. The Q output will be zero unless a phase offset is introduced.

13. What if a scope is to be used to look at the ADC digital outputs?

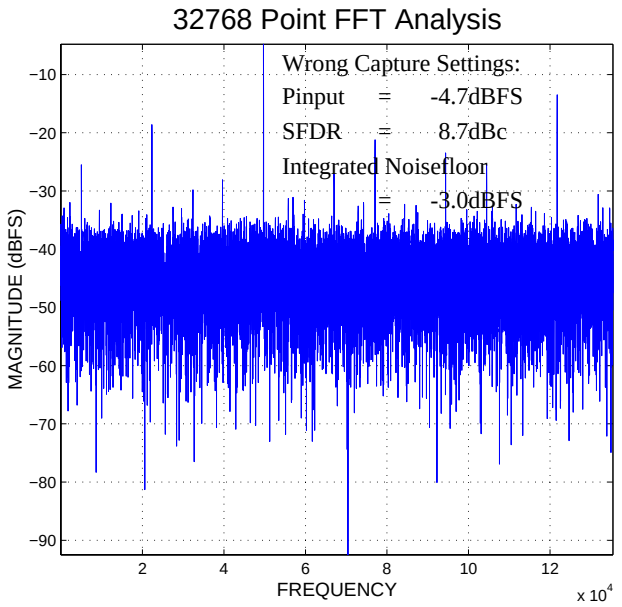


Figure 22 IF Input = 150MHz at 0dBm, Bad Alignment

   Make a special scope probe by soldering a 1K ohm resistor to the center of a BNC connector. Add a short ground clip to the outer conductor. Now plug the BNC into a 50 ohm cable to the scope and set the scope to 50 ohm input mode. This method will provide accurate results since there is very little parasitic capacitance.

14. How can the AGC operation be verified?

    To verify the AGC operation both the ADC output and the CLC5902 output can be compared. The ADC output will reveal the 6dB steps caused by the DVGA. The CLC5902 output will be linear since the 6dB steps are precisely compensated in both amplitude and time.

    In normal operation the AGC keeps the ADC input in the optimal range throughout the TDMA burst. The AGC will adjust the DVGA at the beginning and end of each burst and perhaps during a fade. This is true for GSM since the modulation is of a constant amplitude.

    Observing an AM modulated carrier through the debug port allows the steps in the ADC output to be observed. Figure 23 shows the ADC output with an AM modulated input signal (3kHz modulation at 150MHz IF, -15dBFS threshold, 12dB deadband, 1.5us tc).

    Changing only the modulation frequency (300Hz) and looking at the CLC5902 (DDC) output shows the reconstructed waveform (Figure 24).

    When receiving an EDGE signal the AGC must properly reconstruct the AM content of the modulation. The precise time-alignment of the compensation circuitry enables EDGE data recovery with no loss in performance. In some cases the AGC operation will

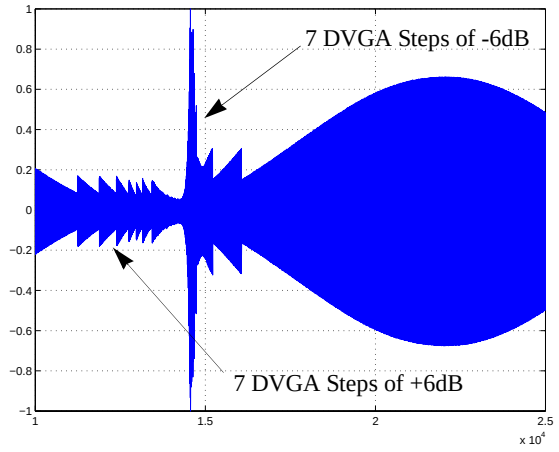


Figure 23 AM Modulation, 150MHz IF, ADC Output

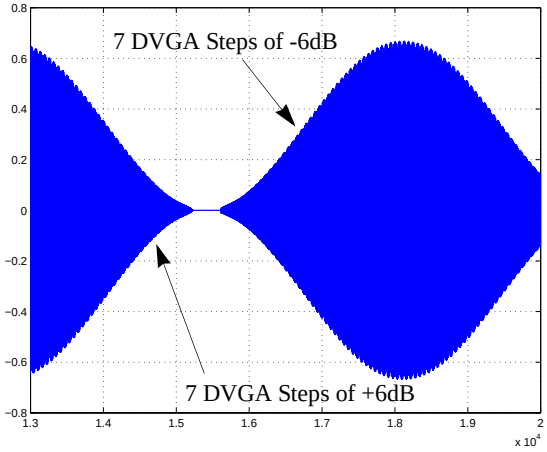


Figure 24 AM Modulation, 150MHz IF, DDC Output

increase the noisefloor slightly but since this only happens at high signal levels it does not impact the receiver's performance.

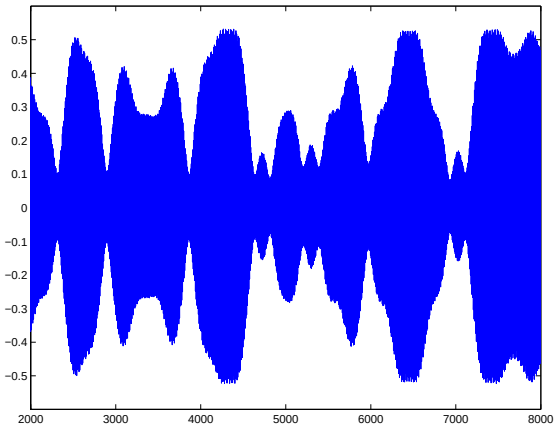


Figure 25 EDGE Modulation, 150MHz IF, ADC Output, AGC Disabled (DVGA fixed at +6dB)

Figure 25 shows the ADC output with an EDGE modulated 150MHz IF input. The DVGA is set to a fixed gain of +6dB. The same signal (skewed in time) with the AGC enabled is shown in Figure 26. A symbol-

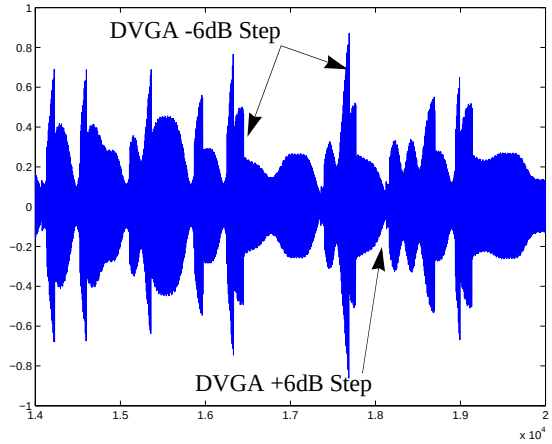


Figure 26 EDGE Modulation, 150MHz IF, ADC Output, AGC Enabled

by-symbol comparison of these two signals at the CLC5902 output (baseband I component) is shown in Figure 27. This figure demonstrates the high degree of

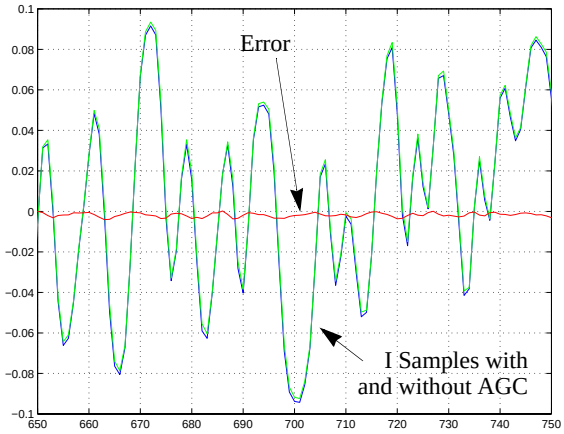


Figure 27 EDGE Modulation, Baseband I Component, AGC Fixed and AGC Enabled Compared

linearity achieved by the CLC5902/CLC5526 AGC circuitry.

15. How can the various evaluation boards be interconnected?

    Refer to the Evaluation Board Interoperability User's Guide at www.national.com under the Wireless Infrastructure Product Site for this information.

16. When the CLC5902 is in 16-bit output mode all of the serial output bits are zero. Is something broken?

    The theoretical noisefloor for a 16-bit digital word is about -98dBFS. The output noisefloor of the DRCS7 Board is about -121dBFS for the default setup. A signal must be applied to bring the output above -98dBFS before the serial output will change.

DRCS Control Panel Software

The DRCS Control Panel (*drcscp.exe*) requires Windows 95/98/NT and a free serial port to operate. Run *setup.exe* from the CD ROM to copy the appropriate files to your hard drive and build the necessary directory structure. Run *drcscp.exe* to start the program. To configure the COM port, choose **Configure I/O** from the **File** menu.

The DRCS Control Panel is a user interface which allows the CLC5902 configuration registers to be programmed from a PC. All register settings are controlled from the four tabs on the left. The **Registers** page (Figure 28) allows you to view a summary of the register values that are down-loaded to the CLC5902.

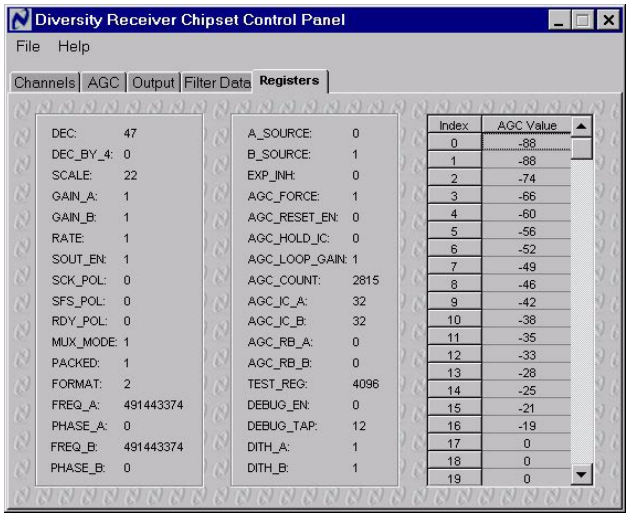


Figure 28 Registers Page

Note

The DRCS Control Panel software can only write to the CLC5902 registers. The software cannot read the CLC5902 register values.

Except for the **Registers** page, each page has a **Send Page** or **Send** button. When pressed, the register values associated with that page are down-loaded to the CLC5902. In addition, a **Send All Data** command is available under the **File** menu.

Note

The Send buttons only send the data for their own pages.

The configuration data entered into the various pages can be saved to a *.dcp* configuration file so they can be reloaded later. The file is ASCII and has one line for each byte that is written to the CLC5902. The first column is the address and the second is the data. Both are in hex format. This hex data can be copied and used in the final system to simplify the development process. The **Save Configuration** and **Load Configuration** commands can be found under the **File** menu.

When you start the DRCS Control Panel, it will load the last used *.dcp* file within the data subdirectory (c:\nsc\data). If you have not yet created one, it will look for *default.dcp*. If *default.dcp* is not found, it will use a set of hard-coded defaults for everything except FIR Filters F1 and F2. For the filters, the program will search for *default.f1* and *default.f2*. If they are not found, zeros will be loaded for the coefficients.

The data entry fields are designed to allow values to be entered using pulldown menus or edit boxes in familiar engineering terms, rather than the integer values that are required by the CLC5902. The engineering values are converted to the appropriate integer values and appear on the **Registers** page. For example, when -150.05 is entered into **Freq**, **Channel A**, the **Registers** page displays the value 491443374 for **FREQ_A** (Figure 28). When the mouse is held over a data entry field, a balloon is displayed which describes the function. If a value is entered that is outside the valid range, a warning is displayed.

For the most part, the data entry fields are intuitive given an understanding of the CLC5902 data sheet. A few exceptions are noted below:

Channels Page

Freq is the frequency of the NCO. You can either enter the IF frequency at the ADC input or the aliased frequency at the ADC output. To down-convert without a phase inversion, use the plot in Figure 2. The signals with dashed lines should be entered with a negative sign. For example, an IF frequency of 150.05MHz requires an entry of -150.05 for no phase inversion. An alternative is to recognize that 150.05MHz aliases to -5.95MHz when **FCK** is 52MHz and, for no phase inversion, enter +5.95. **FCK** refers to the sample rate of the DRCS7 Board, which has a factory default of 52MHz.

`Scale` refers to the bit shift prior to the CIC filter (Figure 50). **Scale (Calculated)** is calculated by the program and is the value required of `Scale` to maintain the gain of the DDC up to and including the CIC filter to unity or just below. It changes when **CIC Decimation** changes. **Scale Adjust** is a bit shift value added to `Scale` prior to down-loading to the CLC5902. You can enter either a positive or negative value with the restriction that **Scale Adjust** + **Scale (Calculated)** fall within the range of 0 to +44 inclusive. A warning is issued for values entered outside this range.

Gain refers to the bit shift after the CIC filter (Figure 50).

AGC Page

The popup menus for initial conditions and gains refer to the gain of the DVGA. The loop dynamics for the AGC are set in the lower left box. Press the Calculate button after entering values for **Threshold**, **Deadband**, and **Time Constant** and the AGC lookup table values and `AGC_LOOP_GAIN` are computed.

Output Page

SCK Rate must be selected low enough to allow all serial bits to exit within one output sample period. If there is not enough time to transmit all the serial data an error message will be displayed. See the CLC5902 data sheet for further discussion.

The proper setting of the '1st Bit' option of the Capture software will be shown on the **Output** page (Figure 29).

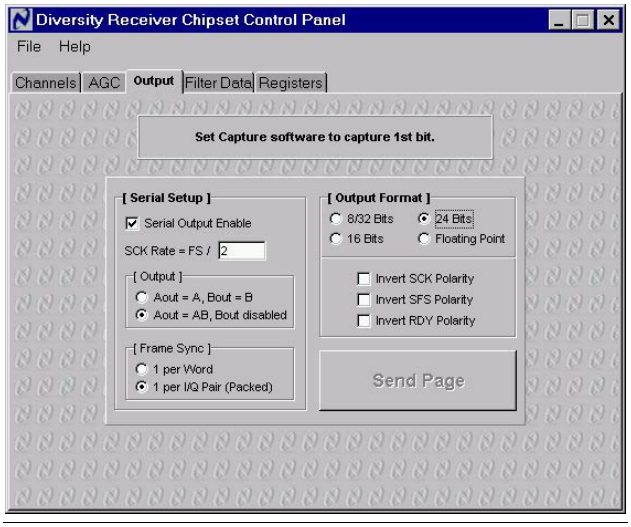


Figure 29 Output Page

Filter Data Page

The coefficient values for each of the symmetric FIR filters can be manually entered or loaded from an ASCII text file using the **Load** button. The file must have a *.f1* extension for **FIR Filter 1** and a *.f2* extension for **FIR Filter 2**. The file format is one signed integer coefficient per line and the number of lines must equal the number of unique coefficients. Also, there must be no blank space before the values in the files. Open one of the default coefficient files (c:\nsc\data\default.f1) in a text editor to see the format.

Serial Communications

There is no handshaking between the DRCS7 Board and the PC. If the system is operating correctly, all the LEDs will light during transmission and only LED1 will remain lit at the completion of transmission. If the transmit sequence is upset, reset the DRCS7 Board and re-send.

Control Panel Software Questions

1. Loading new filter coefficients did not change the response as expected. Why?

   If the new filter coefficients require a different decimation value it must also be sent to the DRCS7 Board.

2. What happens to the default configuration loaded by the COP8 when new data is sent?

   When the DRCS Control Panel sends data to the DRCS7 Board the new data replaces any existing data. Only the data for a single page is updated unless a **Send All Data** command is issued.

3. Is there any non-volatile storage on the DRCS7 Board?

   Only in the COP8 EPROM. No user-accessible non-volatile storage is available.

Default Configuration and SW2 Settings

The CLC-DRCS7-PCASM is configured for 52MHz operation. A 52MHz crystal oscillator module is included so that only one signal generator is required for evaluation.

Table 2 describes the tuning frequencies and filter sets selected by SW2 with a 52MHz clock. Additional SW2 settings (positions 8, 7, 6, & 5) are shown in Table 3. The Table 3 parameters operate independently from the Table 2 parameters except for SW2 position 8.

Config Number	SW2 (87654321)	Channel A/B Tuning	CIC/F1*F2 Decimation[a]	Filter Set
0	0XXX0000	-150.05MHz -150.05MHz	48/4	STD
1	0XXX0001	+10.70MHz +10.70MHz	48/4	STD
2	0XXX0010	-199.00MHz -199.00MHz	48/4	STD
3	0XXX0011	-246.00MHz -246.00MHz	48/4	STD
4[b]	0XXX0100	-150.05MHz -150.05MHz	24/4	STD
5[c]	0XXX0101	0.00 0.00	N/A	N/A
6[d]	0XXX0110	0.00 0.00	N/A	N/A
7[e]	1XXX0111	+10.00MHz +7.50MHz	24/8	GSM
8	1XXX1000	-150.05MHz -150.05MHz	24/8	GSM
9	1XXX1001	+10.70MHz +10.70MHz	24/8	GSM
10	1XXX1010	-199.00MHz -199.00MHz	24/8	GSM
11	1XXX1011	-246.00MHz -246.00MHz	24/8	GSM
12[f]	1XXX1100	-150.05MHz -150.05MHz	12/8	GSM

Table 2 SW2 Default Configurations

a. This column shows the CIC decimation and the F1 decimation * F2 decimation. All cases provide a total decimation of 192 for GSM/EDGE systems (270.833ksps output) except Config 4 & 12 which decimate by 96 (541.66ksps).
b. 2x Oversampled Outputs (541.66ksps)
c. Mixer AI Debug
d. Mixer BI Debug
e. EXP_INH=1, AIN drives both channels
f. 2x Oversampled Outputs (541.66ksps)

The complete COP8 programming tables are available in the file c:\nsc\data\drcs7config_013100.txt after the DRCS Control Panel software is installed.

Function	SW2	0	1
FIR Coefficients[a]	8	STD	GSM
AGC Dynamics[b] (Threshold/Deadband)	7	-12dBFS/ 12dB	-15dBFS/ 9dB
AGC Mode	6	Run	Stop
NCO Dither	5	On	Off

Table 3 Additional SW2 settings

a. SW2-4 and SW2-8 should always be in the same state.
b. Both settings have a 1.5µsec time constant.

Note

The default LC noise filter on the DRCS7 Board has an 18MHz bandwidth centered at 150MHz. Some of the SW2 tuning options will require modification of the LC filter to prevent attenuation of the desired signal.

Table 4 gives the configuration register values for each of the AGC modes associated with SW2 position 6 as mentioned in Table 3.

	SW2 Switch Position 6 Settings	
Register Name	0 (Run)	1 (Stop)
AGC_HOLD_IC	0	0
AGC_RESET_EN	0	0
AGC_FORCE	1	0
EXP_INH	0	0
AGC_COUNT	2815	2815
AGC_IC_A/B	32	32

Table 4 Register values corresponding to SW2 switch position 6.

Any of these default configurations can be modified by using the DRCS Control Panel software. See the DRCS Control Panel Software section on page 14.

Data Capture Board Settings

The Data Capture Board and companion software provide the ability to capture data from the DRCS7 Board as well as a variety of analog-to-digital converter products. When evaluating the DRCS7 Board, configure the Data Capture Board like this:

- DIP switches all ‘OFF”
- ‘WCLK’ jumper = ‘Pin120’
- ‘VCCD’ jumper = ‘+5V’

Figure 30 provides a quick reference for the Data Capture software configuration options.

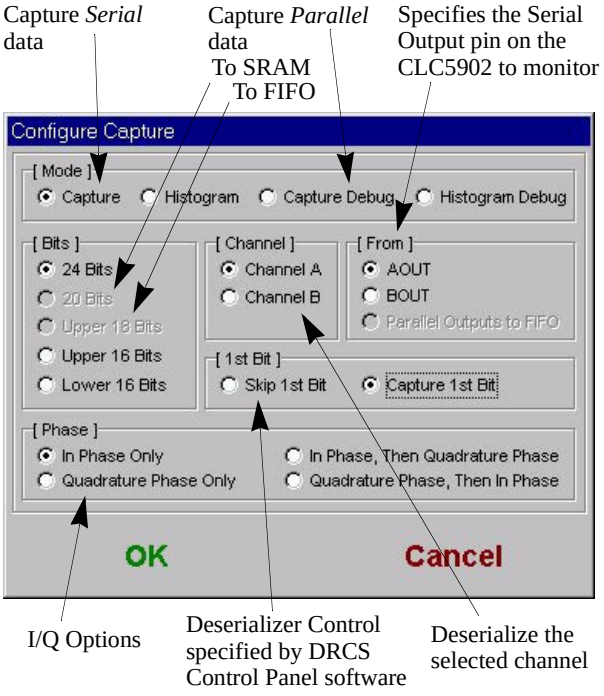


Figure 30 Capture Software Quick Reference

In-Depth Operation

This procedure will verify proper operation of the DRCS7 Board and Data Capture Board. Initial operation is covered in the Quick Start section on page 9.

If a Data Capture Board is not available, an alternate method of saving the data to a file must be used. The default output format for the DRCS7 Evaluation Board is shown in Figure 5. If the data is stored in a two’s complement integer format the supplied Matlab scripts may still be used to process it.

The sequence below requires an unmodulated sine wave source (i.e. HP8644B or R&S SME-03) to generate the input signal.

The DRCS Control Panel software will not be used until the first tests are successfully completed.

1. If you have not already done so, install the DRCS Control Panel and Data Capture Board software.
2. Connect +5V to VCC and ground to GND of connector J3 (the orange terminal block) on the Data Capture Board. When the boards are connected together in the next step, these connections will power both boards. Note that VEE is not required because neither board needs a negative power supply.
3. Connect J1 of the DRCS7 Board to J1 of the Data Capture Board with the connector adapter (CLC-ADAPT1-PCASM) in between. Be sure to remove the spare mating DIN connector if one is attached.

4. Connect a serial cable from the PC to J9 on the Data Capture Board.
5. If two serial ports are available on the PC, connect the other to J9 of the DRCS7 Board. If not, the single port must be shared.
6. Make sure that all DIP switches on both boards are set to off.
7. Turn on the power supply.
8. Start the DRCS Control Panel and Data Capture Board software.
9. Configure the COM ports for the DRCS Control Panel and Data Capture Board software. The COM port setup for the DRCS Control Panel is located under **File**, **Configure I/O**. The COM port setup for the Data Capture Board software is accessed by right-mouse-button clicking anywhere on the program window and selecting **Configure I/O**. Note that power must be applied to the Data Capture Board, the clock must be present, and the serial cable must be connected in order for the software to accept the COM port configuration.
10. Connect a -10dBm sinewave at 150.00MHz to the DRCS7 Board `AIN1` input.

The DVGA should servo to a gain of either +6dB (`AGAIN`=3) or +12dB (`AGAIN`=4) and the ADC should be operating at a level of -10dBFS or -6dBFS. Because `EXP_INH` is not asserted for this configuration, the DDC output (which will be observed below) should be at -28dBFS . This can be computed from the gain equations presented in the Appendix (page 32) and the register data provided in the **Registers** page of the DRCS Control Panel.

The first measurement will be to use the debug mode of the CLC5902 to probe the output of the ADC.

11. Set SW2 on the DRCS7 Board to '00000101' (87654321) then press reset. This selects the Mixer AI debug output and sets the NCO to 0Hz.

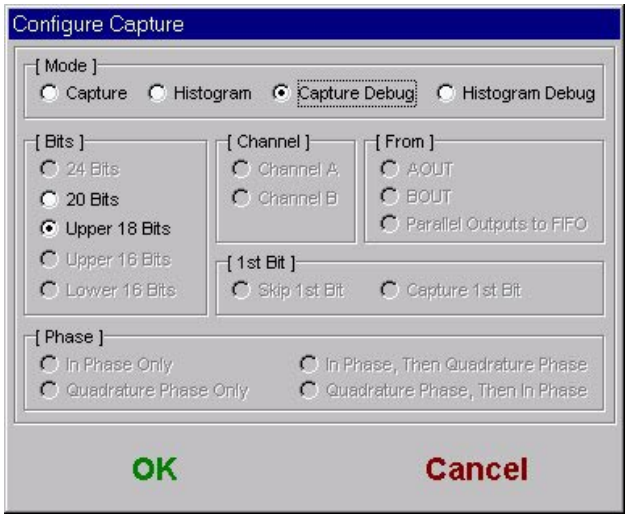


Figure 31 Capture Configuration Dialog, Debug Port

12. Use the right mouse button to access the **Configure Capture** screen of the Data Capture Board software and choose **Capture Debug** within the **Mode** box. Then choose **Upper 18 Bits** within the **Bits** box. Press **OK**. The screen should appear as in Figure 31.
13. Press **Start** on the front panel of the Data Capture software. When the completion bar reaches 100%, the captured data will be written to the file C:\TEMP\DATA.DAT.

If the TEMP directory did not previously exist, the software will create it. You can also specify a different file name and directory by right-mouse-button-clicking on the Data Capture Board software window and choosing the **Change Data File** command. Keep in mind that the Matlab scripts will look for the data in the default location.

The values in DATA.DAT represent 24-bit 2's complement integers. When **Mixer AI** is selected, only the upper 15 bits are non-zero. These numbers can be converted to signed fractional values and plotted by running the Matlab script 'plot_twos.m'. Verify that the waveform is sinusoidal.

Verify that the amplitude is correct by plotting an FFT. Either select 'DRCS Debug' from the 'analysis_menu.m' script or run 'drcs_par_fft.m'. The 'Pinput' shown in the upper right should report either -10dBFS or -6dBFS and there should be a tone at 150MHz-(3*52MHz) = -6MHz.

The next measurement will observe the output of the DDC.

14. Set all the DRCS7 Board SW2 DIP switches to 'OFF' and press reset.
15. Choose **Capture** within the **Mode** box of the **Configure Capture** screen of the Data Capture Board software. Then choose **24 Bits** within the **Bits** box and **Capture 1st Bit** within the **1st Bit** box. Finally, choose **Channel A** from the **Channel** box and press **OK**. The screen should appear as in Figure 15 (see page 9).
16. Click **Start** on the front panel of the Data Capture Board software window.

The values in the file again represent 24-bit 2's complement integers except now all 24 bits are non-zero. Use the MATLAB script 'plot_twos.m' (Plot Twos from the analysis menu) to convert the data to signed fractional values and plot them.

Note

Regardless of the true width of the word being captured, the Data Capture Board will always write 24-bit, 2's complement numbers to DATA.DAT. The only exception to this is when probing AGC CIC A+B in which case each number represents two appended 9 bit numbers.

Verify with an FFT that the output is -28dBFS at frequency 150.00MHz-150.05MHz = -0.05MHz. Use the

'DRCS Serial FFT' menu option or run 'drcs_ser_fft.m' to plot the FFT. A slight frequency offset may exist due to variations in the frequency of the on-board 52MHz crystal oscillator. Note that the output sample rate is 52MHz/192 = 270.8KHz. The FFT will show the CLC5902's filter bandwidth reflected in the shape of the noise floor.

If the signal source causes excessive phase noise at the base of the fundamental tone in the FFT the measured data will be wrong. The routine 'drcs_ser_fft_excl.m' (Alt DRCS Serial from the analysis menu) allows the data within ±2kHz to be replaced by the average noise floor value. This will allow correct measurements to be made. The exclusion bandwidth can be set in the script. This script must be used to verify the proper noise processing gain.

17. Repeat steps 10 through 13 for input AIN2 replacing all occurrences of **Channel A** with **Channel B**. In step 11 set SW2 to '00000110'.

Next the DRCS Control Panel software and the serial interface will be verified.

18. Press reset on the DRCS7 Board.
19. On the **Channels** page of the DRCS Control Panel, enter 0 for **Freq** within the **Channel A** box to set the frequency of the channel A NCO to zero. Also check **Debug Enabled** and select **Mixer AI** from the **Probe at** pulldown menu within the **Common** box. The screen should appear as in Figure 32. Click on the **Send Page** button. Immediately following this, a data transfer indicator box will appear on the monitor and all the LEDs on the DRCS7 Board will light momentarily.

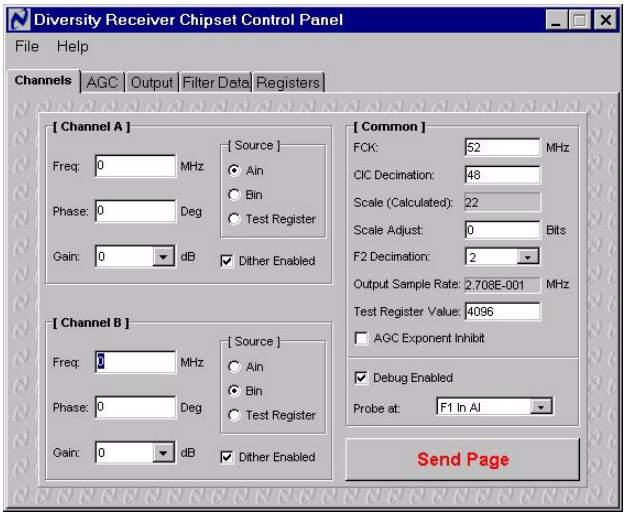


Figure 32 DRCS Channel Configuration, Debug Output

Now repeat steps 12 and 13 and review the results as before.

20. On the **Channels** page of the DRCS Control Panel, enter -150.05 for **Freq** of **Channel A**, uncheck **Debug Enabled**. The screen should appear as in Figure 33. Click on the **Send Page** button.

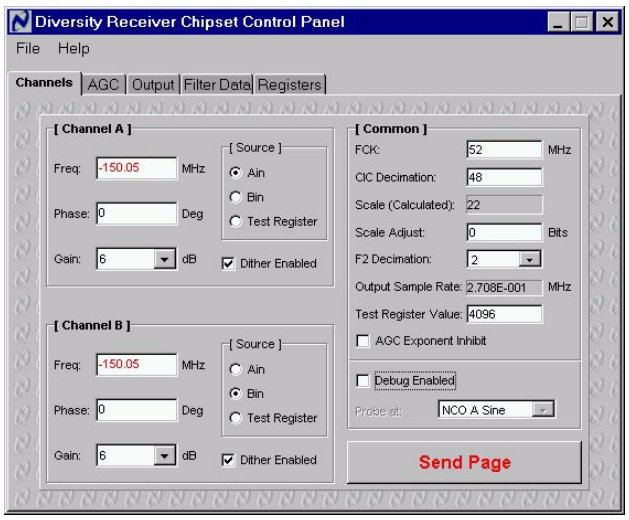


Figure 33 DRCS Channel Configuration, Serial Output

Repeat steps 15 and 16 and review the results as before. Changing the frequency with the DRCS Control Panel, capturing more data, and performing an FFT should cause the output tone on the FFT to move the same amount.

This completes the verification of the board operation.

DDC Large-Signal Nonlinearity Exercise

This exercise is intended to illustrate the two types of large-signal nonlinearity that can be encountered when the CLC5902 is incorrectly configured. Both can be observed at the input of filter F1. The same equipment is used as in the In-Depth Operation section on page 16.

1. Connect a -10dBm sinewave at 150.000MHz to the DRCS7 Board `AIN1` input.
2. Load *default.dcp* by choosing **Load Configuration** from the **File** menu of the DRCS Control Panel.
3. On the **Channels** page, enter -150.005 (5kHz offset) for **Freq** within the **Channel A** box and enter 6 for **Scale Adjust** within the **Common** box. Also check **Debug Enabled**, select **F1 In AI** from the **Probe at** pulldown menu, and set **Channel Gain**s to 0. The screen should look like Figure 34. Click on the **Send Page** button.
4. On the **Configure Capture** screen of the Data Capture Board software, choose **Capture Debug** within the **Mode** box and **18 Bits** from the **Bits** box (see Figure 31). Click on **OK**.
5. Press **Start** on the front panel of the Data Capture Board software window.

As before, the values in DATA.DAT represent 24-bit 2's complement integers and only the upper 18 bits are non-zero. Use the MATLAB script 'plot_twos.m' (Plot Twos from the analysis menu) to convert the data to signed fractional values and plot them. Zoom in on the first 300 points to see something similar to Figure 35. This distortion is caused by overflow in the CIC filter due to `SCALE` being set too large. This overflow cannot be sensed and the only way to avoid it is by making sure that `SCALE` is

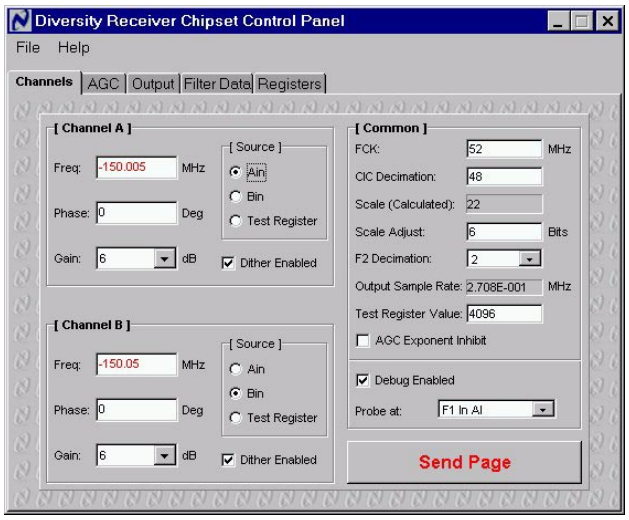


Figure 34 DRCS Channel Configuration, CIC Rollover

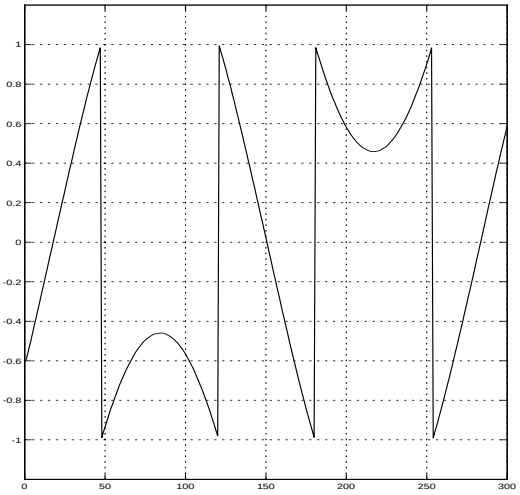


Figure 35 CIC Overflow Distortion

set consistent with the chosen CIC decimation value so that the CIC output is less than full scale. Figure 35 may not look exactly the same as yours due to the frequency error between the on-board clock oscillator and the input source. The important characteristic of the distortion is that the positive sinusoid peaks have been translated to negative values and the negative peaks to positive values.

6. Go back to the **Channels** page of the DRCS Control Panel and change **Scale Adjust** back to 0. Next, select **36dB** from the **Gain** pulldown menu in the **Channel A** box. The screen should look like Figure 36. Click on **Send Page**.

7. Press **Start** on the front panel of the Data Capture Board software window.

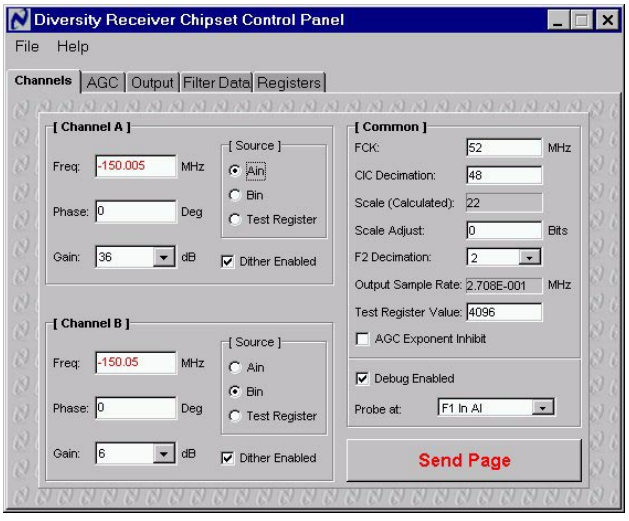


Figure 36 DRCS Channel Configuration, Saturation

Use ‘plot_twos.m’ (Plot Twos from the analysis menu) to convert the data to signed fractional values and plot them. Zoom in on the first 300 points. You should see the clipping as shown in Figure 37. This represents the type of nonlinearity at all stages of the DDC except for the CIC filter.

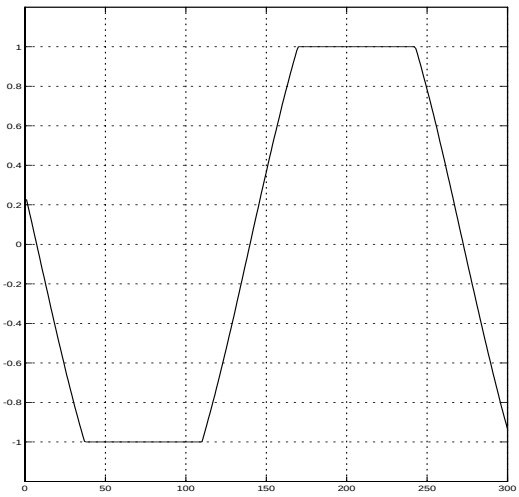


Figure 37 Datapath Saturation at the F1 Input

Connector Pinouts

Table 5 describes the Futurebus+ connector (J1) pinouts on the DRCS7 Board. Relevant signal names have been overlaid on the generic pin assignments in Table 5. Unused pins are grayed-out. These pins are reserved for future use.

Power is supplied through J1. If the Data Capture Board is connected to J1, power should be connected to J3 (the orange terminal block) on the Data Capture Board.

	A	B	C	D
1	TRST	DataB0	GND	DataA0
2	TCK	DataB1	Config0	DataA1
3	TMS	DataB2	GND	DataA2
4	TDO	DataB3	Config1	DataA3
5	TDI	DataB4	GND	DataA4
6	GND	DataB5	Config2	DataA5
7	SPI_CK	DataB6	GND	DataA6
8	SPI_CS	DataB7	Config3	DataA7
9	SPI_DO	DataB8	GND	POUT[0]
10	SPI_DI	DataB9	Config4	POUT[1]
11	GND	DataB10	GND	POUT[2]
12	SCK_OUT	DataB11	Config5	POUT[3]
13	SFS_OUT	DataB12	GND	POUT[4]
14	RDY_OUT	DataB13	Config6	POUT[5]
15	AOUT	DataB14	GND	POUT[6]
16	BOUT	DataB15	Config7	POUT[7]
17	GND	DataB16	GND	POUT[8]
18	SCK_IN	DataB17	Config8	POUT[9]
19	SFS_IN	DataB18	GND	POUT[10]
20	SRDY_IN	DataB19	Config9	POUT[11]
21	SD_INA	DataB20	GND	POUT[12]
22	SD_INB	DataB21	Config10	POUT[13]
23	GND	DataB22	GND	POUT[14]
24	NRST	DataB23	Config11	POUT[15]
25	5V	5V	5V	5V
26	5V	ClkB	5V	SCK
27	GND	GND	GND	GND
28	GND	GND	3.3V	3.3V
29	POUT_SEL[2]	$\overline{\text{POUT\_EN}}$	2.5V	2.5V
30	POUT_SEL[0]	POUT_SEL[1]	-5V	-5V

Table 5 FutureBus+ Connector J1 pinout

Table 6 describes 10-pin JTAG header and 16-pin DSP header pinouts. The schematic in Figure 41 provides the pinout for J9, a female DB-9 used to connect the standard RS-232 serial cable from the PC.

Pin	JTAG	DSP
1	TCK	N/C
2	GND	GND
3	TDO	SCK
4	VCC	GND
5	TMS	BFSR
6	N/C	GND
7	$\overline{\text{TRST}}$	BDR
8	$\overline{\text{SCAN\_EN}}$	GND
9	TDI	GND
10	GND	GND
11		N/C
12		GND
13		N/C
14		GND
15		N/C
16		GND

Table 6 JTAG and DSP header pinouts

Operation with a 13MHz Reference

The advantages of operating the DRCS at 52MHz make it worthwhile to do so even in a 13MHz system. This can be done by either of these two methods:

1. Replace the system oscillator with a 52MHz unit and divide down to 13MHz. This is probably the lowest cost alternative since only one VCXO is required. Keep in mind that the phase noise of the 52MHz VCXO will also be divided down.
2. Phase-lock a 52MHz VCXO to the 13MHz clock. This approach requires more additional components but has the least impact on existing circuitry. A circuit that can be used for this purpose is shown in Figure 43.

Schematics

Figure 38, Figure 39, Figure 40, and Figure 41 are the CLC-DRCS7-PCASM schematics. Figure 42 is the Connector Adapter (CLC-ADAPT1-PCASM) schematic.

Reference Design

The schematic for a complete reference design is provided in Figure 44. This circuit is the same as the DRCS7 Evaluation Board without the COP8 and its associated components. In this example the LC filter is tuned to 71MHz and must be re-tuned to the appropriate value.

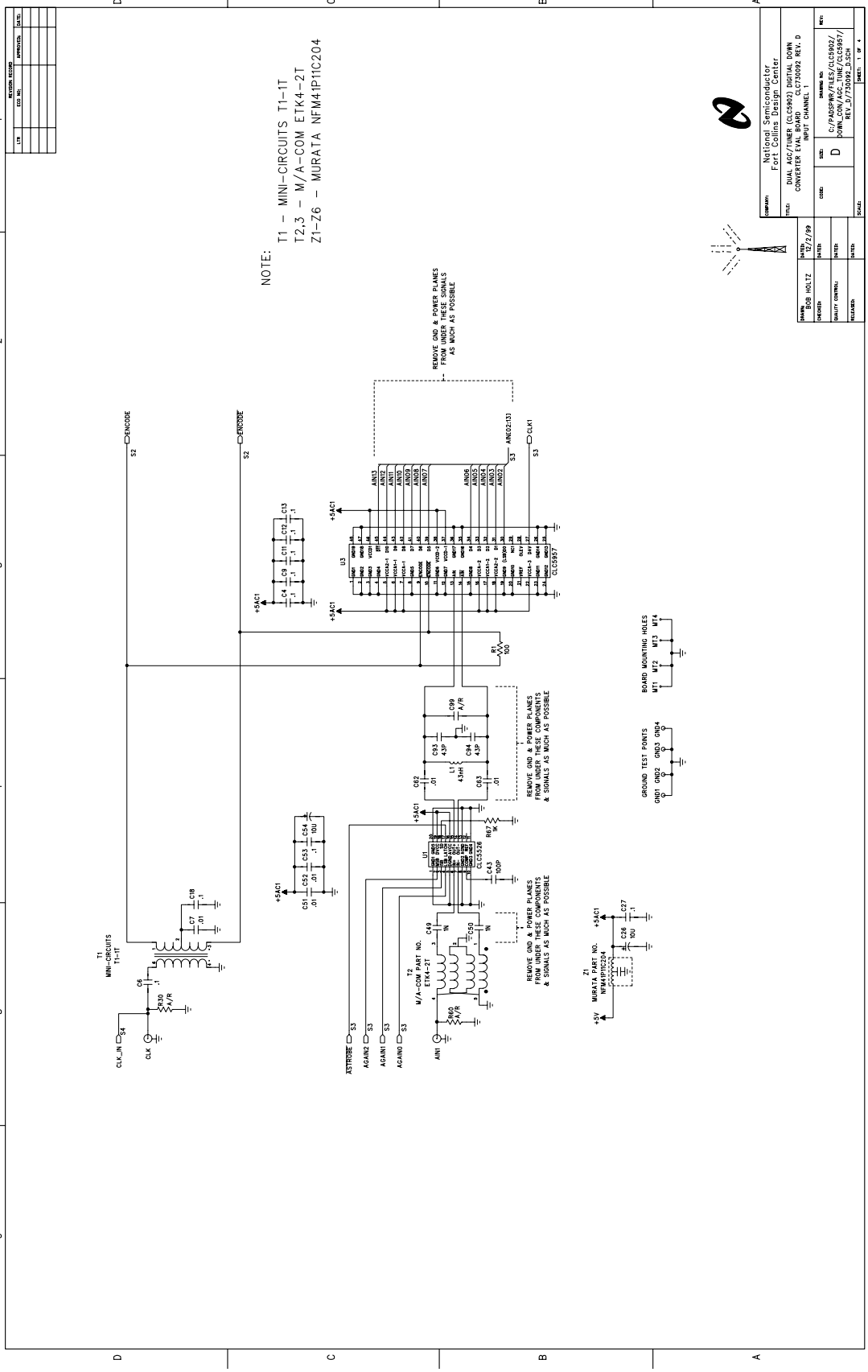


Figure 38 ADC Input AIN1

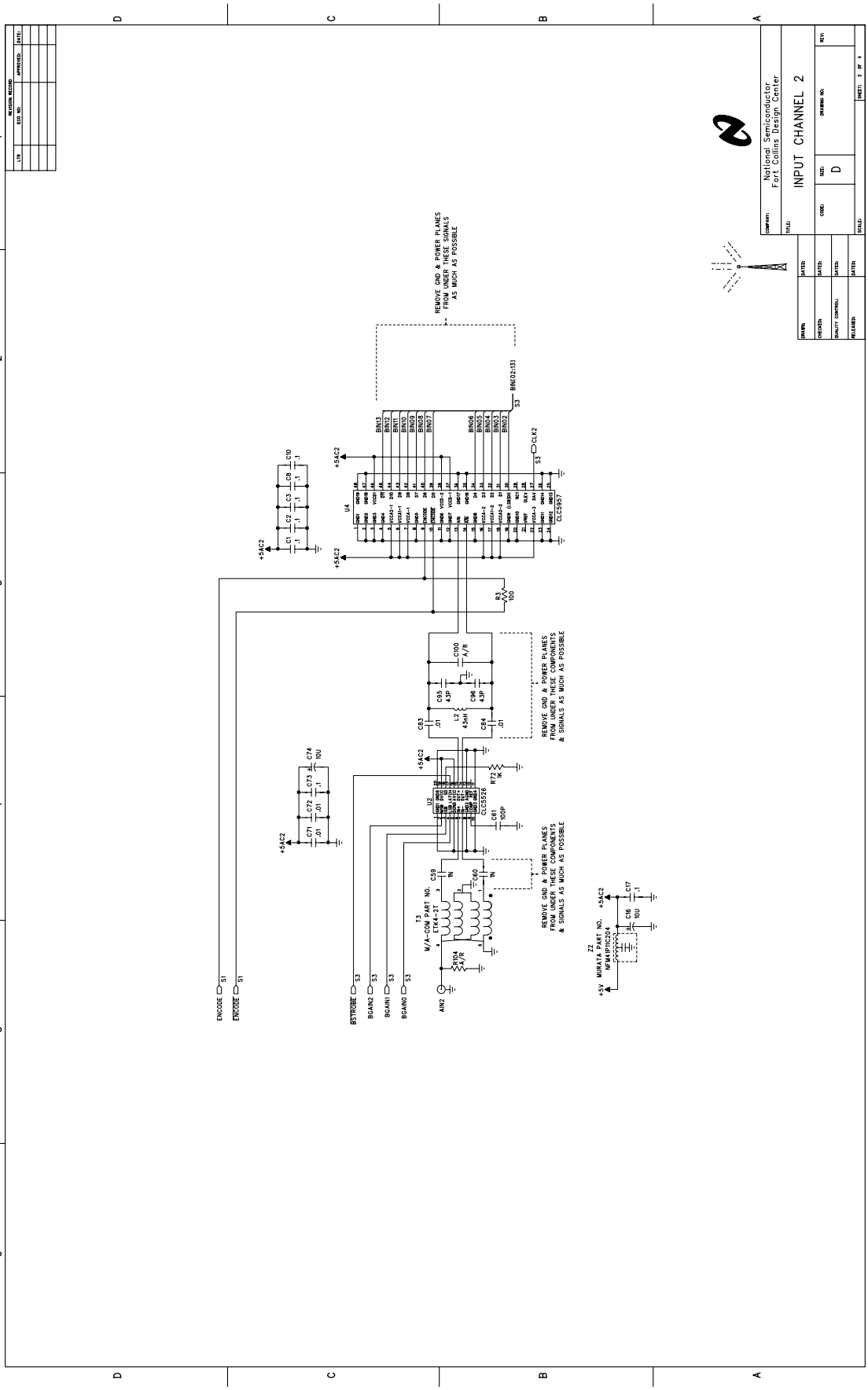


Figure 39 ADC Input AIN2

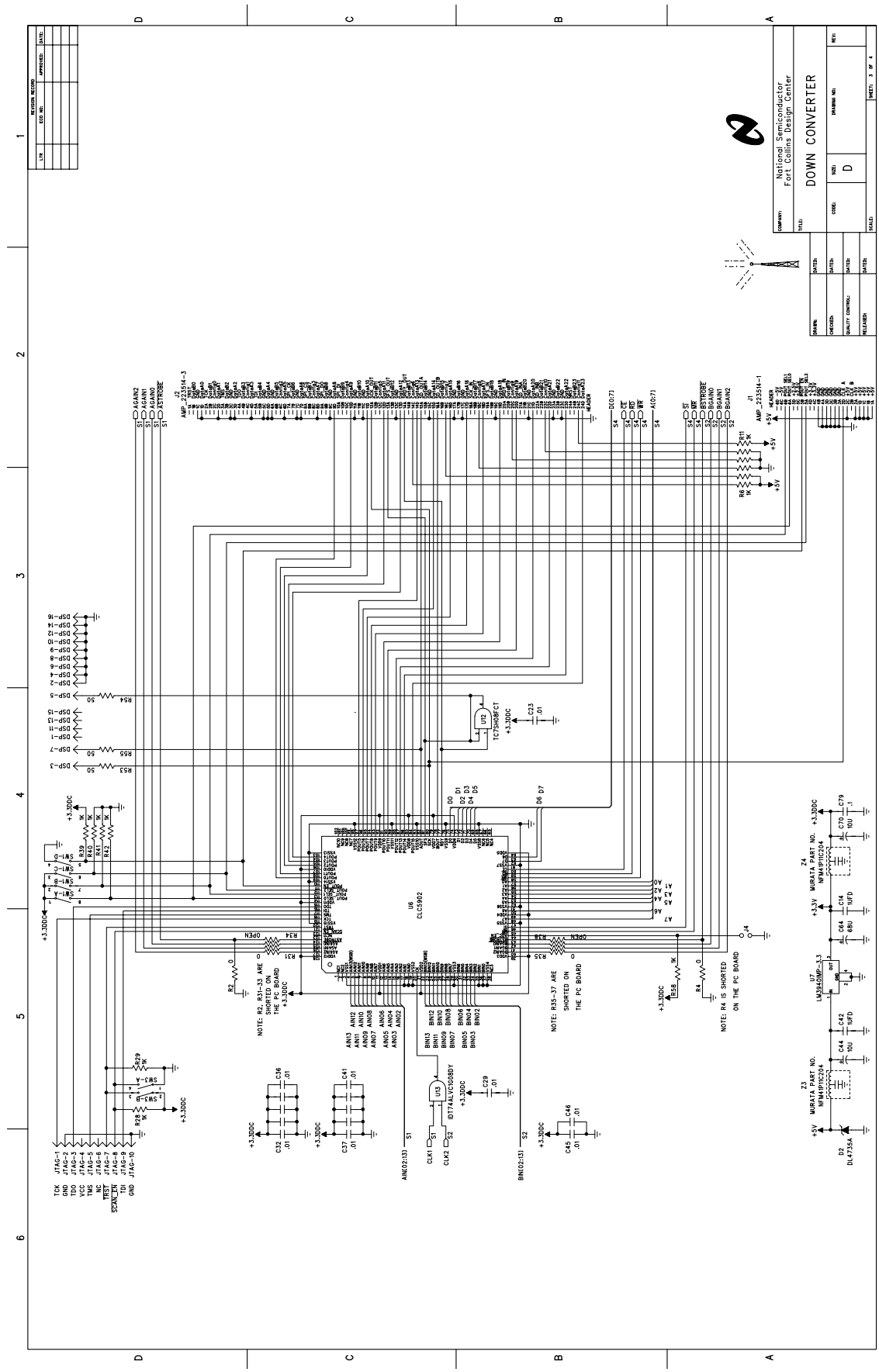


Figure 40 CLC5902 Dual Digital Tuner/AGC

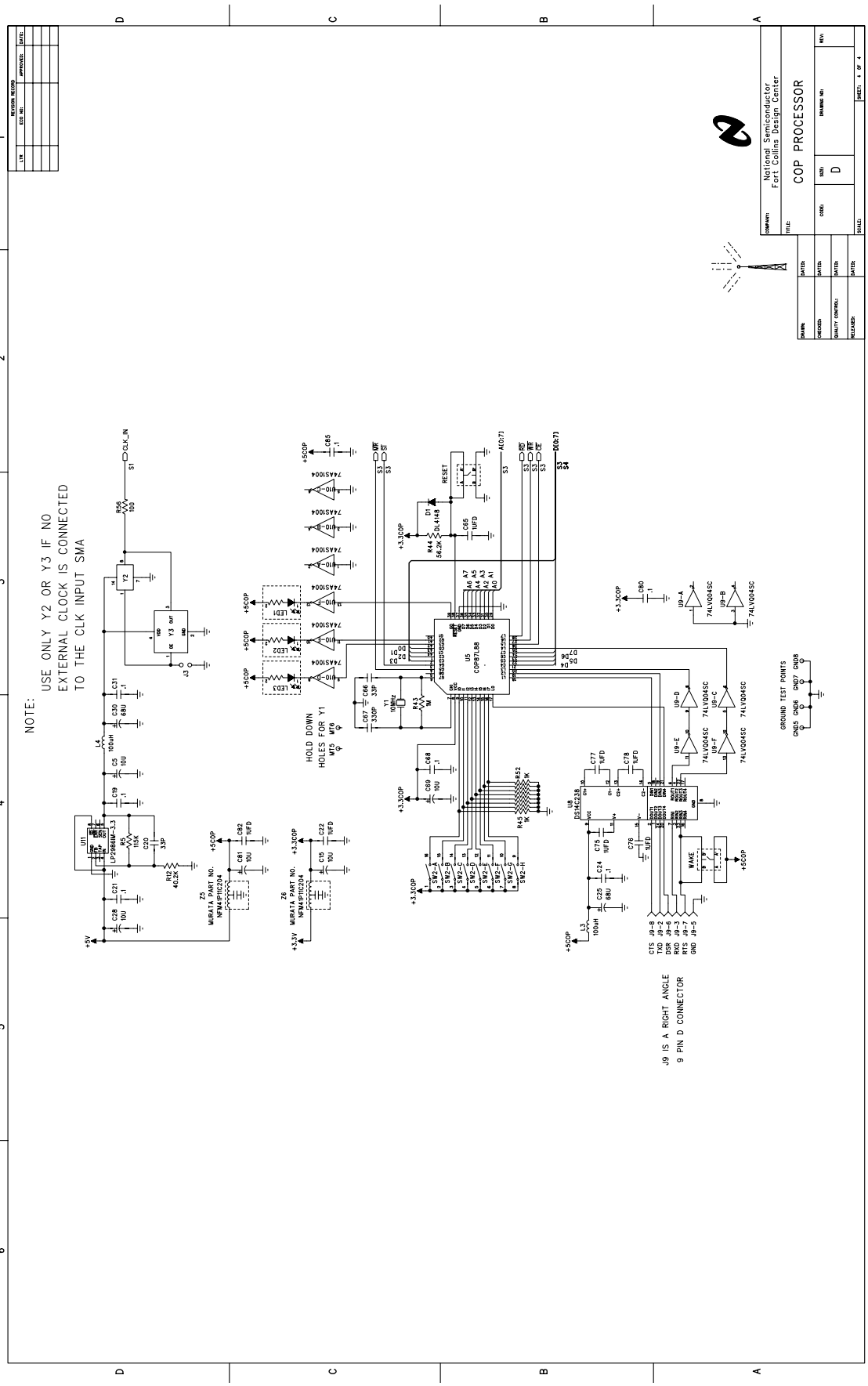


Figure 41 COP8 Microprocessor

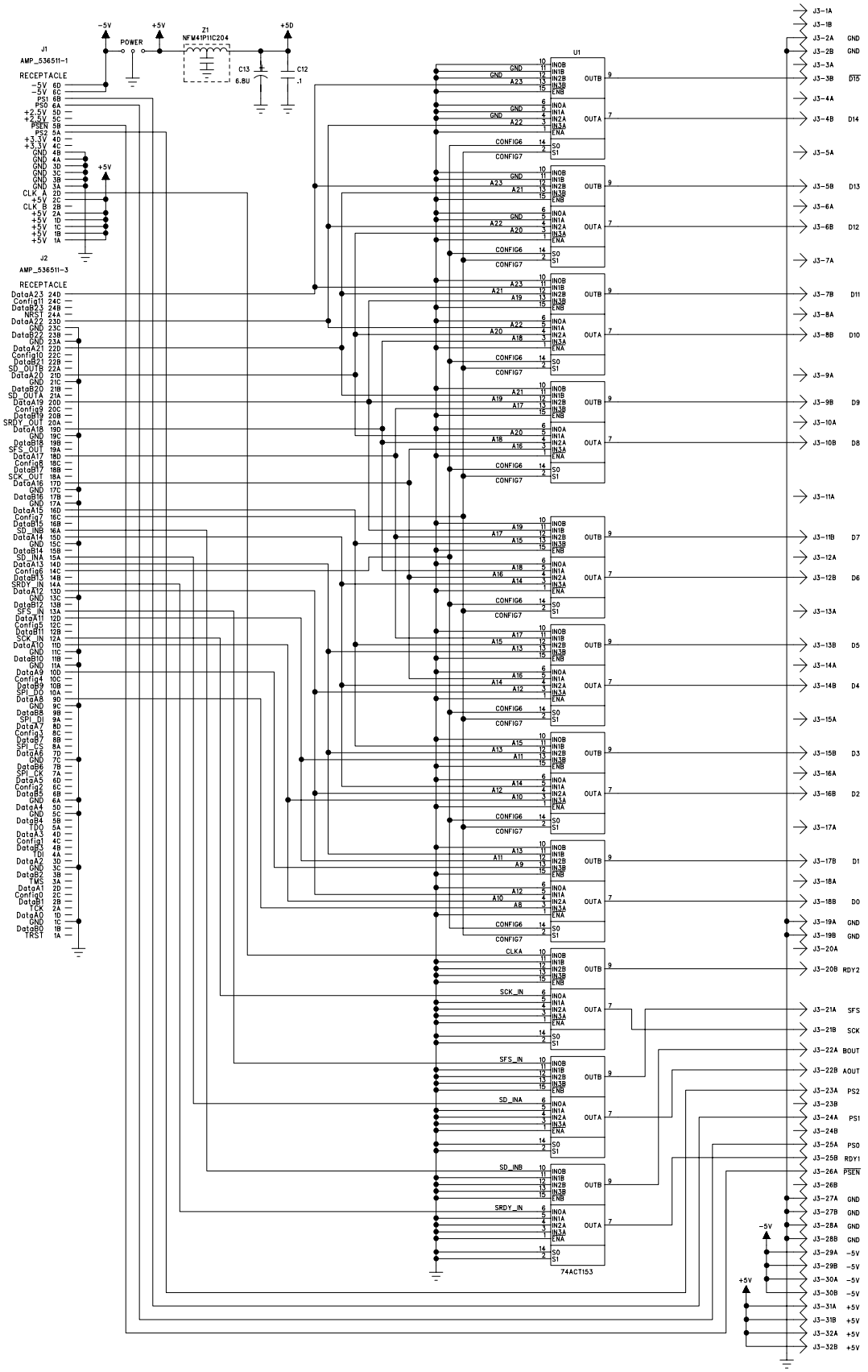


Figure 42 Connector Adapter (CLC-ADAPT1-PCASM)

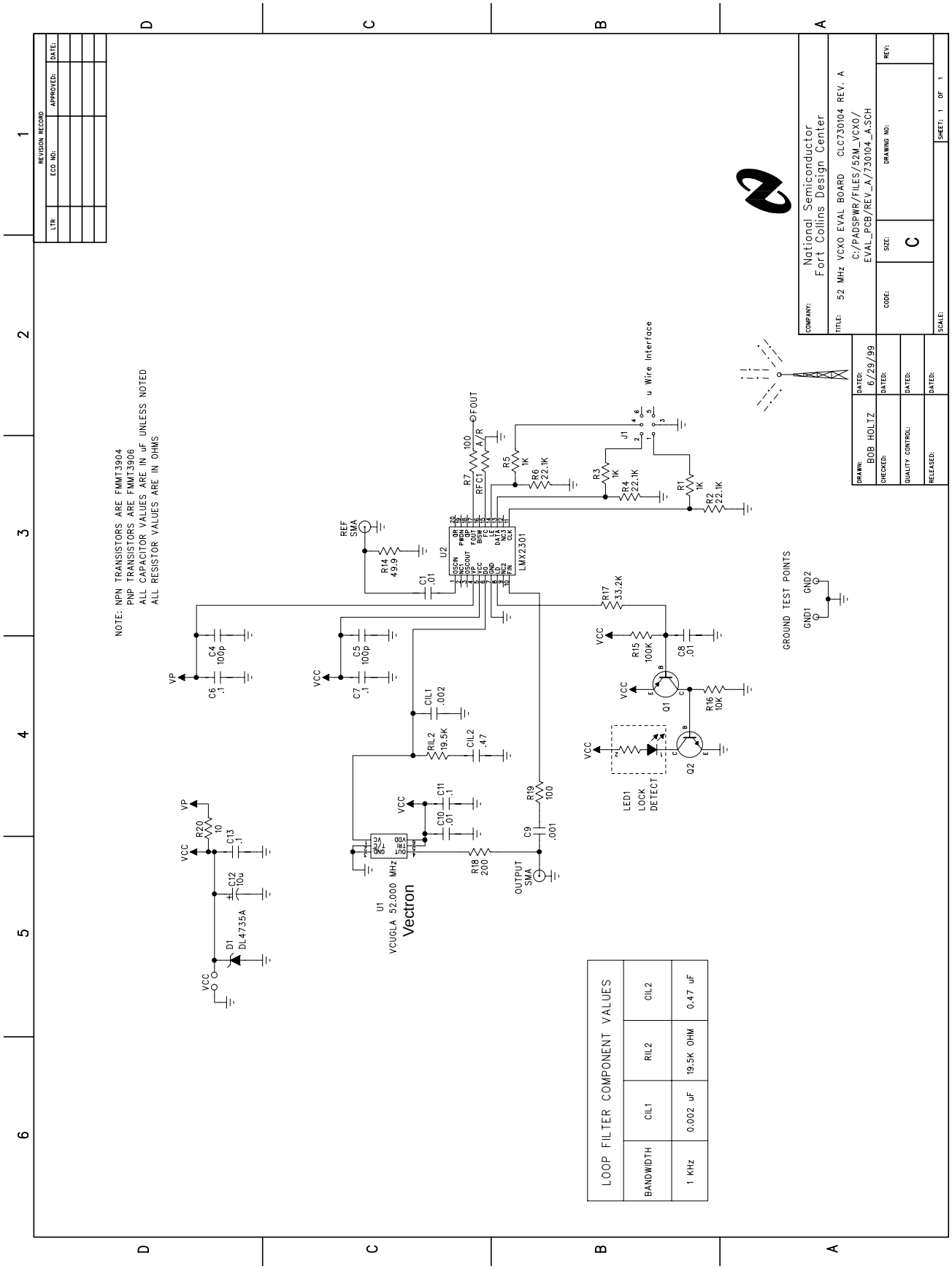


Figure 43 Circuit for a 52MHz VCXO Locked to a 13MHz Reference

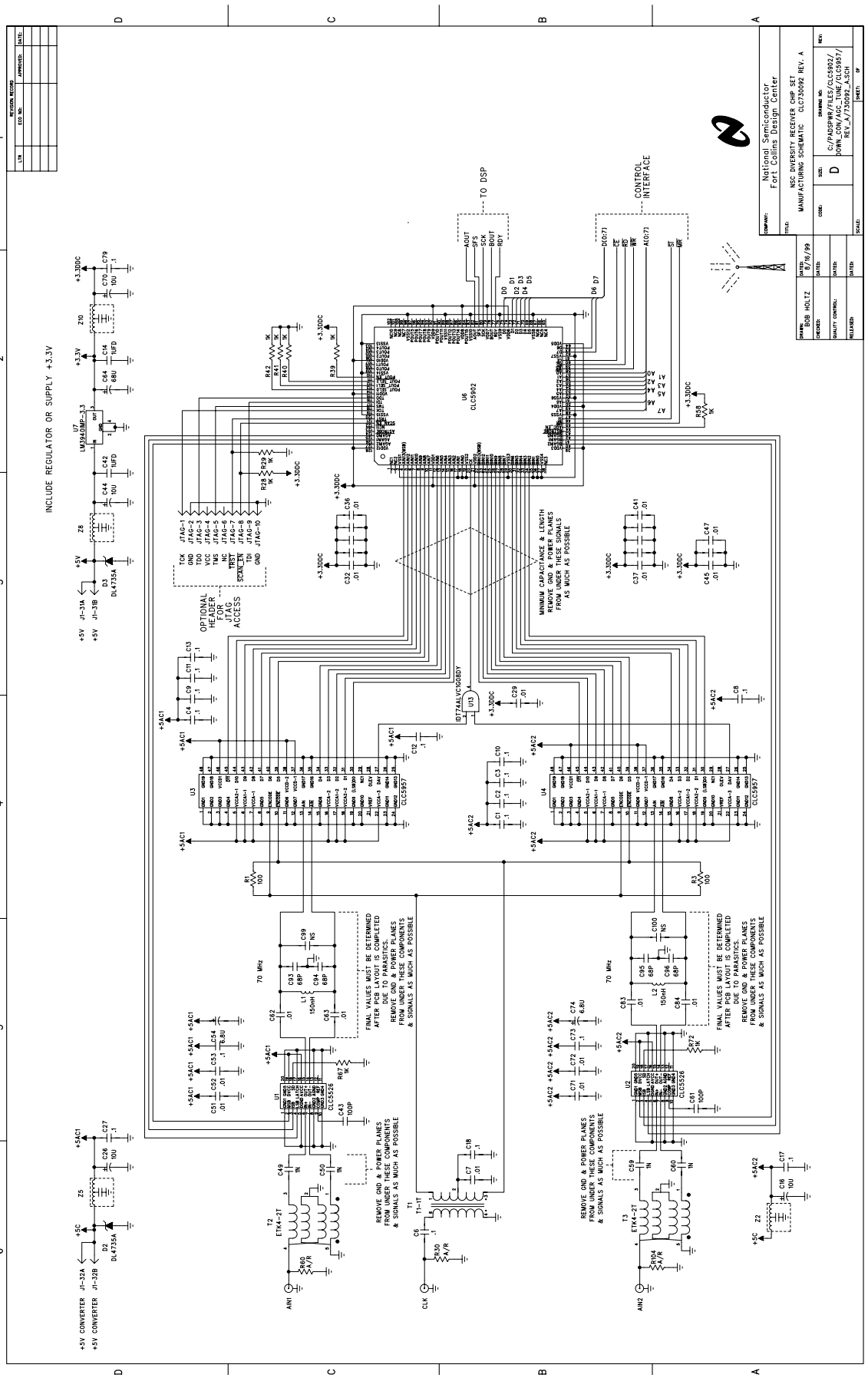


Figure 44 DRCS Reference Design

PC Board Layout

Silk screen parts placement drawings are shown below. The complete board layout package can also be provided. Primary areas of concern are the analog inputs to the ADC and the ADC digital outputs.

Care has been exercised to prevent ground loops and noise coupling on the circuit board at the inputs. Noise coupling is reduced by aligning the split between analog and digital planes across all layers.

The ADC outputs have been kept as short as possible to minimize capacitive loading. The internal ground plane has been removed under these traces to reduce the parasitic capacitance. Higher capacitance values will load the ADC output drivers causing additional noise on the internal analog signals. This will degrade the ADC performance. Analog and digital grounds have been star (common-point) connected to minimize crosstalk. The supplies have series inductors for each section to provide extra isolation.

Figure 45, Figure 46, Figure 47, and Figure 48 show the DRCS7 Board parts placement and PC board layers. PCB layout tips are annotated on the plots.

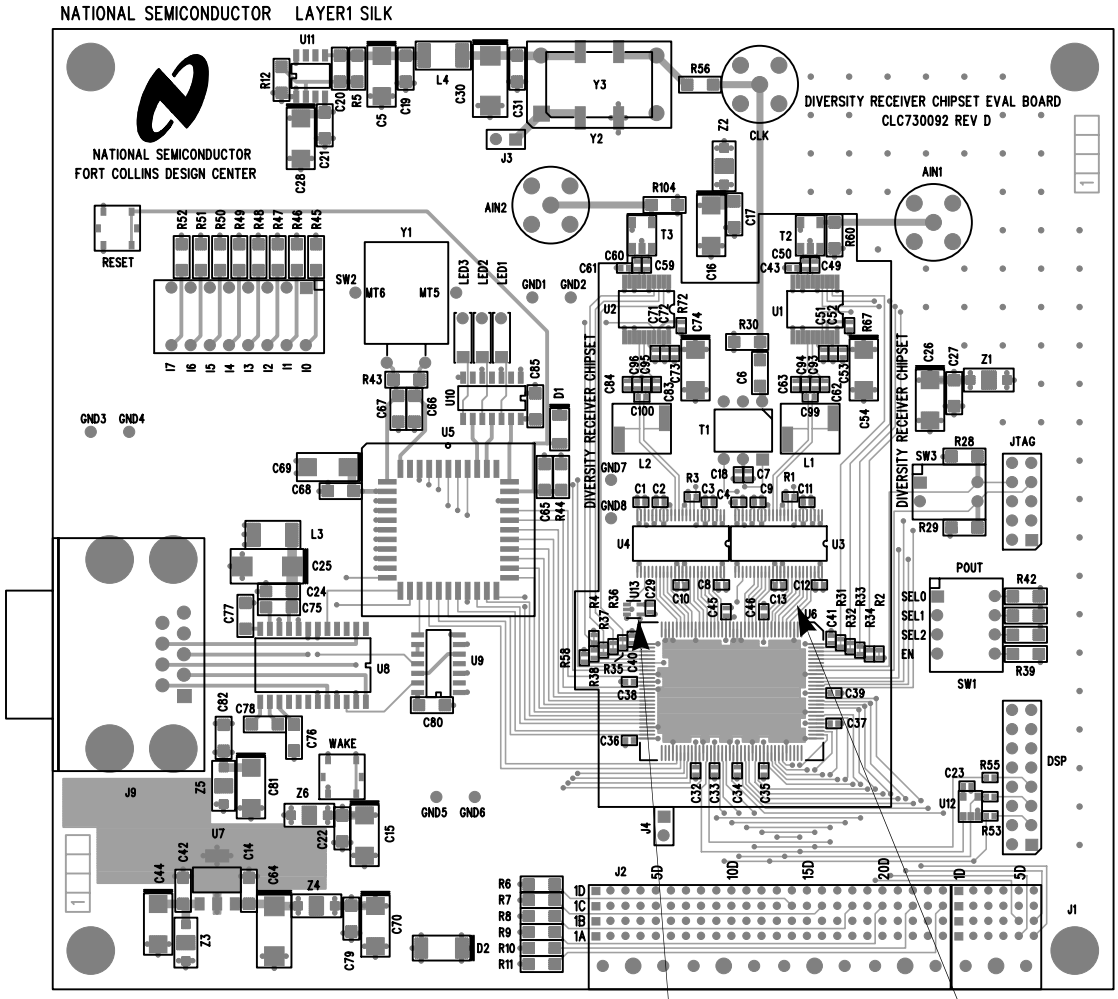


Figure 45 DRCS7 Board layout, Top, L1 + Silk

AND gate for the 2 DAV clock signals.

Keep these traces to the minimum length possible.

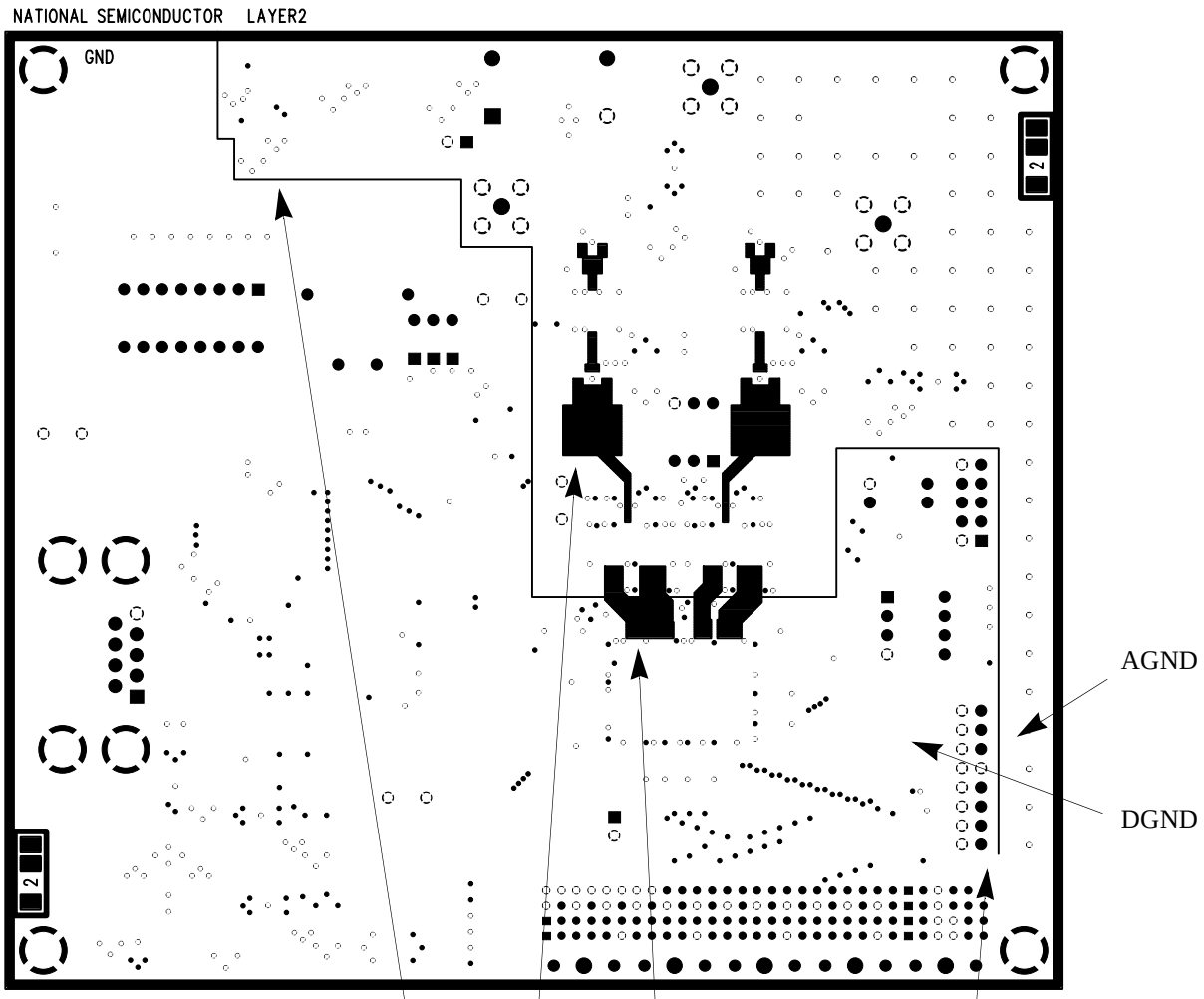


Figure 46 DRCS7 Board layout, GND, L2

Line up split between analog and digital planes across all layers.

Minimize parasitics at the LC filter since these are high-impedance nodes.

Minimize capacitive loading on the ADC output by removing power and ground planes.

Common-point ground where the analog and digital planes join.

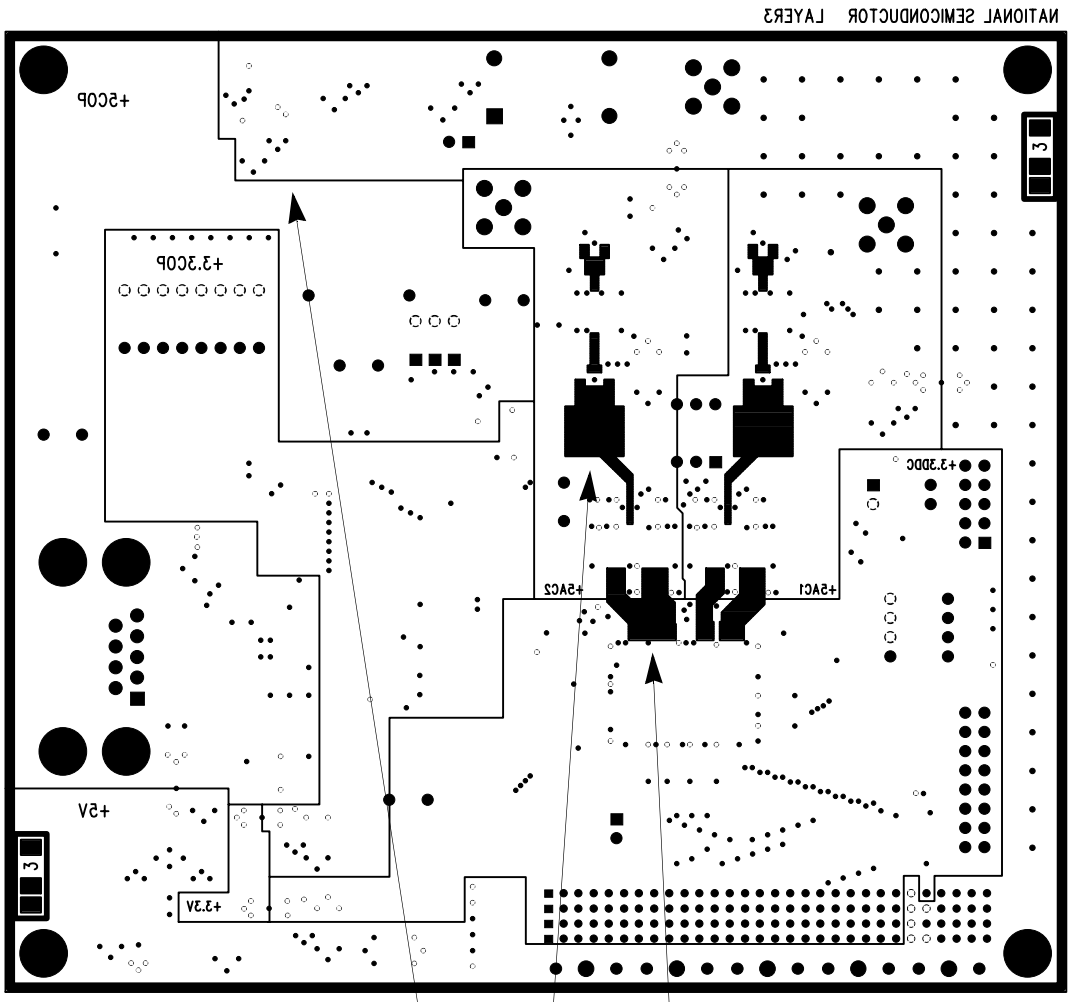


Figure 47 DRCS7 Board layout, Power, L3

Line up split between analog and digital planes across all layers.

Minimize parasitics at the LC filter since these are high-impedance nodes.

Minimize capacitive loading on the ADC output by removing power and ground planes.

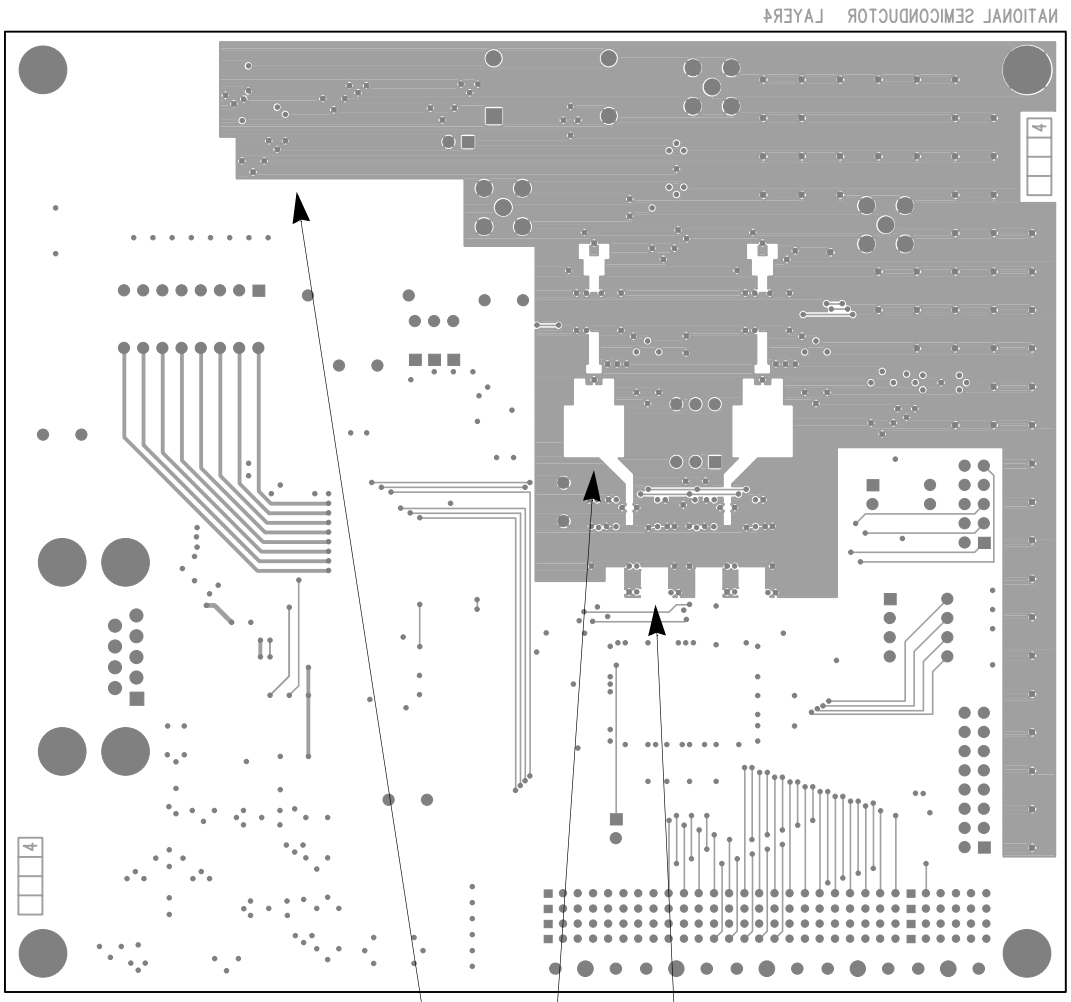


Figure 48 DRCS7 Board layout, Bottom, L4

Line up split between analog
and digital planes across all layers.

Minimize parasitics at
the LC filter since these
are high-impedance nodes.

Minimize capacitive loading
on the ADC output by removing
power and ground planes.

Appendix

Input Circuit and Signal Levels

The AIN1 and AIN2 IF inputs are transformer coupled into the DVGA inputs. The transformers convert the single-ended input signal to differential and match the 200Ω input of the DVGAs to the 50Ω input connectors. They have a voltage gain of 2:

$$G_{XFMR} = 2 \quad \textbf{(EQ. 11)}$$

In a production system, the transformer might be replaced by an IF SAW with differential output drive capability.

With the DVGA set to maximum gain (+30dB), the total analog gain from the input connector to the ADC is 33.8dB and an input level of -23.8dBm will drive a full-scale input at the ADC. With the DVGA set to minimum gain (-12dB), the total analog gain is -8.3dB and a +18.3dBm input level is required to drive the ADC to full scale. Typically, the AGC reference level will be set such that the ADC will never see full scale and the lowest gain setting of the DVGA will not be used.

The total gain of the DRCS7 Board, including both the analog and digital parts is best described by the equation,

$$G_{TOTAL} = G_{XFMR}G_{DVGA}G_{LC}G_{DDC}, \quad \textbf{(EQ. 12)}$$

where the first term has already been introduced and the others will be in subsequent sections of this manual.

DVGA

The DVGA is a 350MHz amplifier that has a digitally-controlled voltage gain range from -12 to +30dB in 6dB steps. It has a 3rd-order output intercept point of 24dB at 150MHz and an output noise spectral density of $69 nV/\sqrt{Hz}$. At 150MHz, the data sheet plots place the maximum gain at about 28.5dB or,

$$G_{DVGA} = (0.21) \cdot 2^{AGAIN}, \quad \textbf{(EQ. 13)}$$

where *AGAIN* is the 3-bit data word into the DVGA digital input of channel A. Refer to the CLC5526 data sheet for further details.

The DVGA, in conjunction with the DDC/AGC, forms an automatic leveling loop that compresses the dynamic range of the input IF signal prior to sampling by the ADC. By doing so, it extends the dynamic range of the ADC by as much as 42dB. The loop dynamics and threshold of the AGC are set by programming the control registers within the CLC5902. It is also possible to inhibit the loop and force specific DVGA gain values.

ADC

The ADC is a 12 bit, wideband converter capable of inputs as high as 300MHz at sample rates of 70MSPS. The SNR for an input 3dB below the full scale input of $2V_{PP}$ differential is 62dBFS at an IF frequency in the range of 150MHz. For levels much below this, however, the SNR improves to 68dBFS (or, $55 nV/\sqrt{Hz}$ at 52MSPS). This behavior is due to the fact that the large-signal, high-frequency SNR is dominated by clock jitter.

GSM systems typically require no more than 9dB of SNR (C/I) which can be achieved at input levels of 59dB below full scale. EDGE systems typically require 23dB SNR for full rate operation. This requirement can be met with an input signal at -45dBFS, still low enough to minimize the effects of clock jitter.

The ADC acts as though it were a 68dB device for these systems (Figure 49). The digital filters following the ADC provide processing gain that improve further upon this by 24dB (factory default configuration, 200kHz output BW). Assuming that a single sampling image interferes at a level of -4dB (Figure 8), the total noise voltage density at the ADC input is,

$$\sqrt{55^2 + 69^2(1 + 10^{-4/10})} = 98 nV/\sqrt{Hz}. \quad \textbf{(EQ. 14)}$$

When this is referred through the 33.8dB maximum gain to the input connector, this yields a 13dB noise figure for the DRCS7 Board.

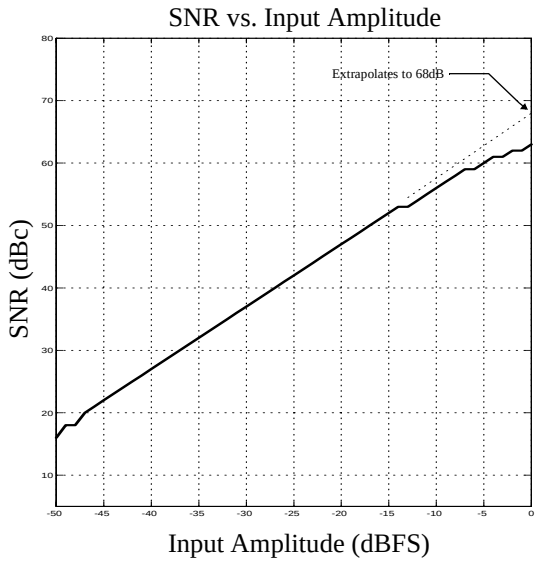


Figure 49 CLC5957 SNR Extrapolates to 68dBFS

DDC

The ADC outputs feed into the two channel DDC/AGC. This part consists of two down converter channels (DDC) and automatic gain control (AGC) loops. The DDC performs the final mix to baseband and baseband filtering (see Figure 50).

The NCO can tune across the full Nyquist band with 32 bit precision. With phase dither enabled, the spurious performance is -101dBc or better and SNR is 84dBFS. The frequency and phase of the two channels are completely independent. In addition, the phase dither of the two are uncorrelated.

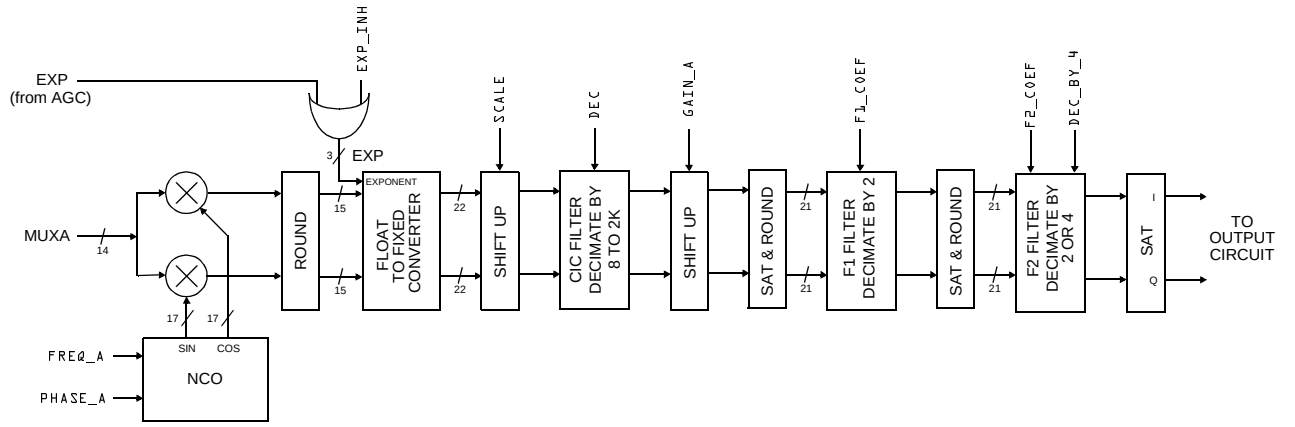


Figure 50 CLC5902 Digital Down Converter, Channel A

The baseband filtering is performed by a cascade of three decimating FIR filters. The overall decimation ratio can be programmed from 8 to 16,384. The two final filters feature 21 and 63 user-programmable taps, respectively. A set of tap coefficients are published in the CLC5902 data sheet which provide adequate filtering to meet the GSM blocker and interferer requirements. The frequency response for these filters at a sample rate of 52MSPS is shown in Figure 51.

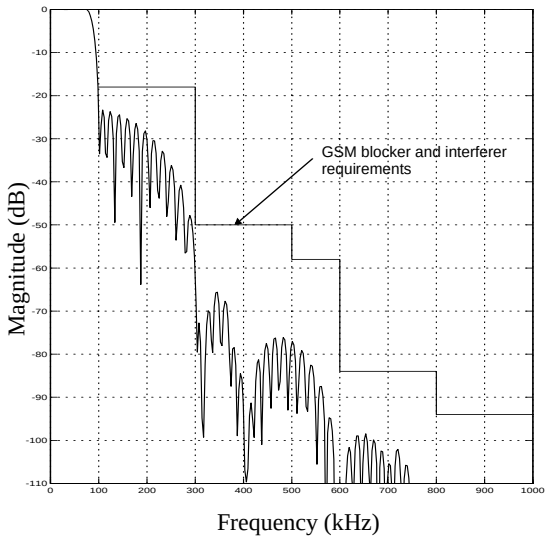


Figure 51 Frequency Response of GSM Filter Set

Although the ADC combined with the processing gain of the digital filters provides 92dB of instantaneous SNR, this is not enough to meet the requirements of the GSM900 specification without some analog filtering to attenuate the blocker. Nonetheless, the digital filters can be used to relax the requirements on the analog filter. In particular, the digital filters can meet the reference interference level of *ETSI GSM 05.05 paragraph 6.3* without any assistance from the analog filter. Further, the blocker performance of *ETSI GSM 05.05 paragraph 5.1* can be met with only minor assistance from the analog filter.

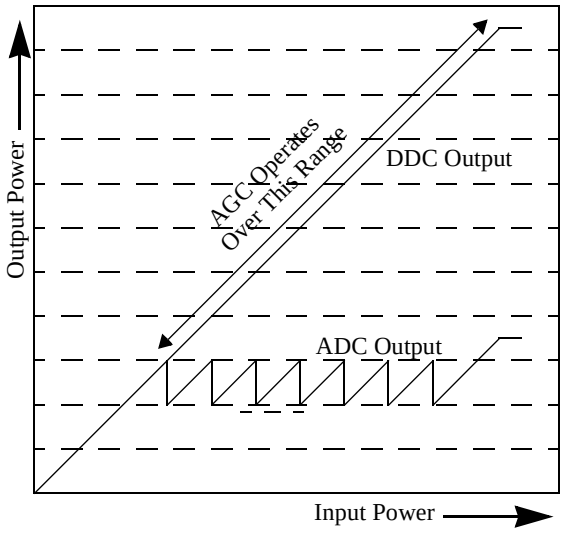


Figure 52 ADC and DDC Output Level vs. Input Level

The FLOAT TO FIXED CONVERTER within the DDC will match any change in gain by the DVGA with a compensating digital gain change. It does this by treating the complement of the DVGA control word as an exponent to the ADC output. The overall effect of this is to make the DRCS7 Board appear as a fixed gain channel with extremely large dynamic range as shown in Figure 52. This mode can also be inhibited by asserting `EXP_INH`. An expression for the gain through the DDC channel A is,

$$G_{DDC} = \frac{1}{2}(DEC+1)^4 \cdot 2^{[SCALE-44-AGAIN\cdot(1-EXP\_INH)]} \cdot 2^{GAIN} \cdot G_{F1} \cdot G_{F2} \quad \text{, (EQ. 15)}$$

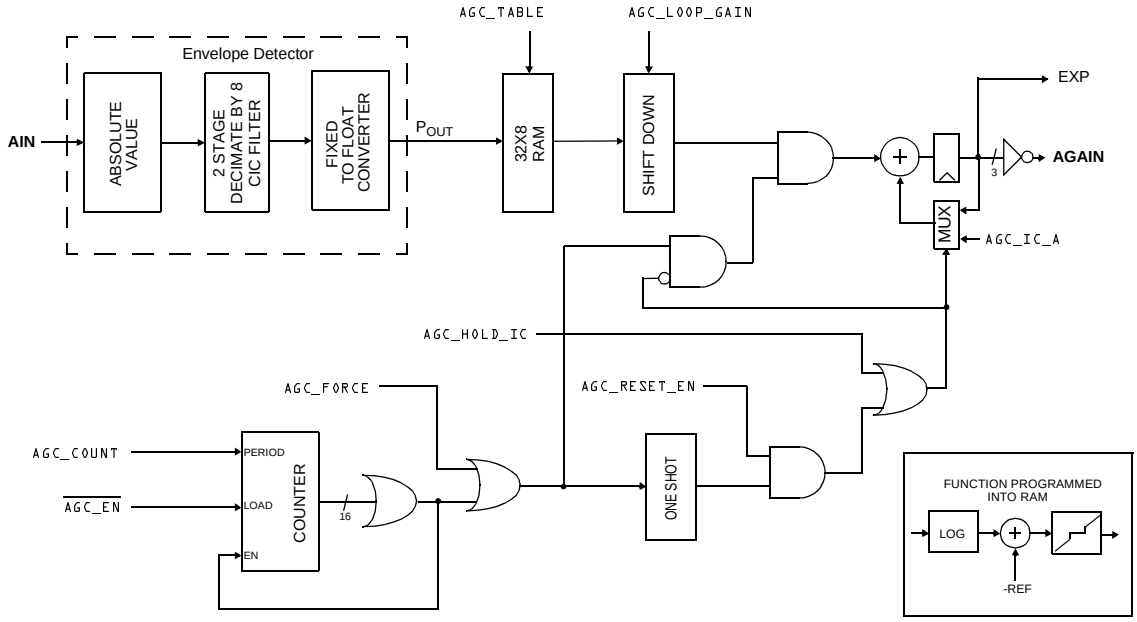


Figure 53 AGC Circuit, Channel A

$$G_{F1} = \frac{\sum_{i=1}^{21} h_1(i)}{2^{16}}, \qquad \textbf{(EQ. 16)}$$

$$G_{F2} = \frac{\sum_{i=1}^{63} h_2(i)}{2^{16}}. \qquad \textbf{(EQ. 17)}$$

The numerators of G_{F1} and G_{F2} equal the sums of the impulse response coefficients of F1 and F2, respectively. For the STD and GSM sets, G_{F1} and G_{F2} are nearly equal to unity. Observe that the *AGAIN* term in (EQ. 15) is cancelled by the corresponding term appearing in (EQ. 13) so that the entire gain of the DRCS7 Board is independent of the DVGA setting when `EXP_INH=0`. The $\frac{1}{2}$ appearing in (EQ. 15) is the result of the 6dB conversion loss in the mixer.

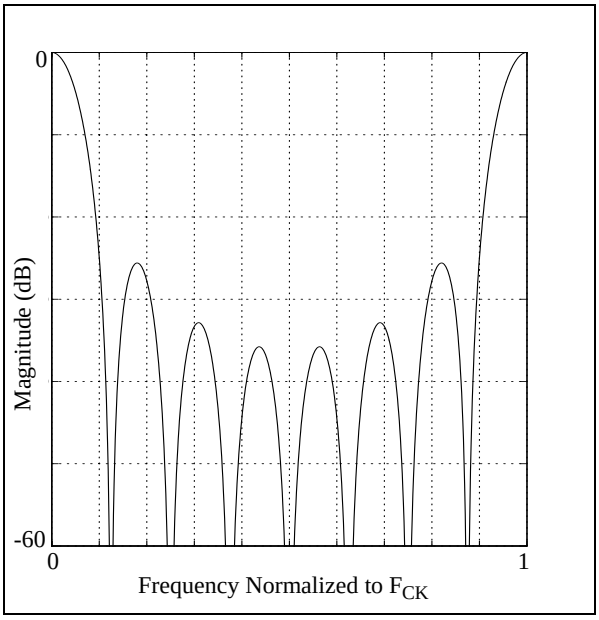


Figure 54 Response of Envelope Detector Filter

AGC

The AGC loop for channel A is shown in Figure 53. Each channel has its own loop. The ADC output power is measured with an envelope detector and used to adjust the DVGA gain. Envelope detection is performed by an absolute value circuit followed by a lowpass filter whose response is shown in Figure 54. The filtered signal is used to address a lookup table which generates an error signal based on the programmed threshold, deadband, and loop time constant targets. This error is integrated to produce the 3 bit control signal for the DVGA. Integrator gain is programmable via the shifter preceding it to allow loop time constants that can be varied by factors of 2. Fractional control of time constant can be achieved by altering the slope of the transfer function stored within the lookup table.

In the course of measuring ADC power, the absolute value block within the envelope detector also generates a second harmonic of the aliased IF frequency. For example, an IF of 150MHz aliases to -6MHz at the ADC output when the sample rate is 52MHz. The absolute value block produces from this a dc term and a second harmonic at -12MHz, the latter of which is rejected by the low pass filter. If the alias frequency is too low, though, its second harmonic will fall within the passband of the filter and a clean power detection will not occur. This problem can be avoided by choos-

ing the IF and sample rates such that the alias frequency magnitude is greater than $F_{CK}/16$.

The user interface software makes programming of the AGC very easy. The user need only specify the loop time constant, reference, and deadband. The lookup table values and shifter values can then be computed. As shown in Figure 55, deadband in excess of 6dB shows up as hysteresis. Hysteresis will eliminate excessive DVGA gain changes caused by the input signal level dwelling at a transition point.

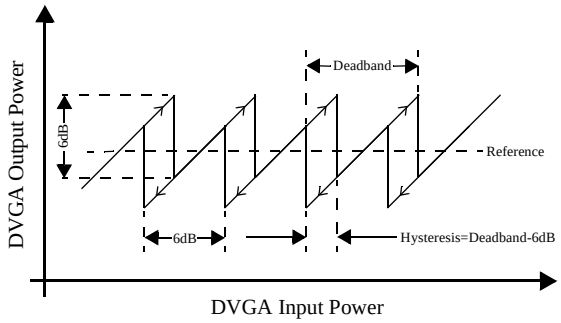


Figure 55 Relationship between deadband and hysteresis

The AGC has several operating modes. The simplest is the free-run mode where the loop is closed continuously and the DVGA gain setting is constantly updated in response to the signal level applied to the board. This mode is easiest to use and is suitable for most applications. The default configuration of the DRCS7 Board and user software is for this mode. The other mode is a gated mode and is useful, for example, in TDMA systems when one wishes the AGC to be active only during the power ramp up. In this mode, the loop is active when the gate signal is applied and then opens when the gate is removed. The gate signal can be an external pulse whose width defines the AGC active period. Alternatively, the gate can be an edge which starts a counter within the DDC/AGC. The AGC active period is then the time it takes for the counter to reach its terminal value. By using the configuration registers, it is possible to write the initial gain condition of the loop into the integrator and also to read the final gain value from this integrator. Consult the CLC5902 data sheet for further details.

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