National Semiconductor

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CLC-DRCS-PCASM
DRCS Evaluation Board User's Guide

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Overview

The DRCS Evaluation Board (CLC-DRCS-PCASM) is designed to support simple and effective evaluation of the Diversity Receiver Chipset (DRCS). This chipset consists of the CLC5956 Analog-to-Digital Converter (ADC), the CLC5526 Digital Variable Gain Amplifier (DVGA), and the CLC5902 Dual Digital Tuner/AGC. The CLC5902 performs digital down conversion (DDC) and automatic gain control (AGC) with digital accuracy and repeatability.

The DRCS Board accepts narrowband signals at IF frequencies up to 300MHz (the LC noise filter must be retuned from the 150MHz factory setup) and outputs quadrature baseband signals in a digital format. There are two complete signal paths from the two input connectors to the Channel A and Channel B digital outputs.

The configuration of the DDC/AGC is controlled by a COP8 µController which loads one of several default configurations at power up. The default configuration is selected using DIP switch SW2. These configurations can also be modified with the DRCS Control Panel software (*drcscp.exe*) provided with the DRCS Board that runs under Windows® 95/98/NT.

Also available is a Data Capture Board (CLC-CAPT-PCASM) and accompanying software (*capture.exe*) that mates with the evaluation board and enables the user to transfer data from the DDC/AGC output, over the serial port of a PC and into a file.

This document describes in detail the DRCS Board, DRCS Control Panel software, and how to use it.

Required Evaluation Items

- DRCS Board (CLC-DRCS-PCASM)
- +5V power supply
- Signal generator
- DRCS Control Panel software (*drcscp.exe*)
- PC running Windows® 95/98/NT
- One PC serial port

Suggested Evaluation Items

- Data Capture Board (CLC-CAPT-PCASM)
- Data Capture Board software (*capture.exe*)
- Data Capture Board User's Guide
- Second PC serial port
- Matlab® software or other data analysis software

Reference Documents

- CLC5956 data sheet
- CLC5526 data sheet
- CLC5902 data sheet

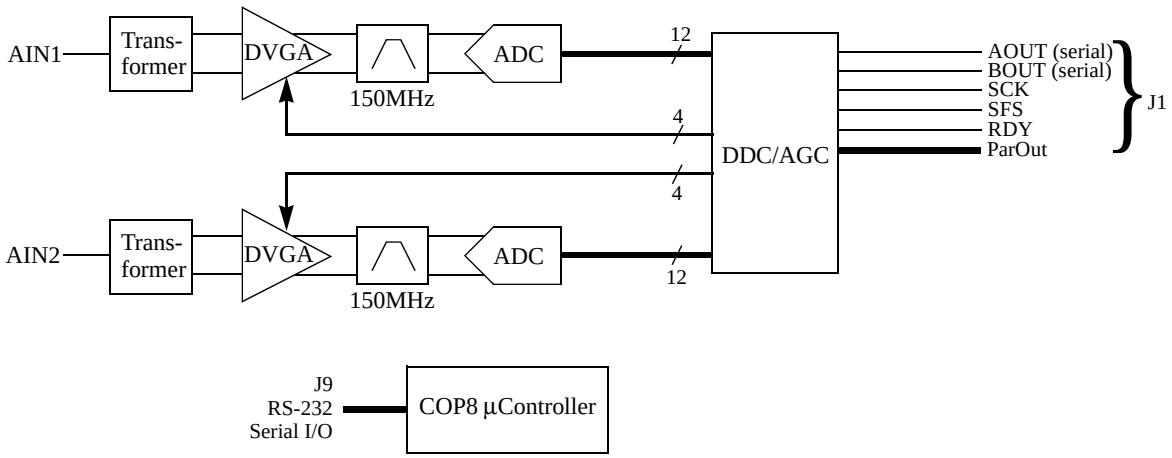

Figure 1 CLC-DRCS-PCASM Block Diagram

General Description

As seen in Figure 1, the DRCS Board accepts analog IF inputs on a pair of SMA connectors and processes these into baseband digital waveforms. There are several analog components that condition the signal prior to sampling with a pair of ADCs. The most important of these is the DVGA which is the gain control element of an AGC loop. The sampled signals are applied to a two channel digital down converter (DDC) that performs a final mix to baseband, digitally filters the waveforms, and decimates to a lower output sample rate. On-board automatic gain control (AGC) loops operate in conjunction with the DVGAs to extend the dynamic range of the analog signal paths.

The DRCS Board is factory configured for an IF of 150MHz, a sampling frequency (F_{CK}) of 52MSPS, and an overall decimation of 192. This yields an output sample rate of 270.8KSPS. The DDC/AGC features a high degree of programmability so that key parameters such as mixer frequency, decimation ratio, filter shape, etc. can be configured by the user.

The individual elements of the DRCS Board are discussed in the following paragraphs.

Input Circuit and Signal Levels

The AIN1 and AIN2 IF inputs are transformer coupled into the DVGA inputs. The transformers are included to interface with the differential analog components which follow. They also match the 200Ω input of the DVGAs to the 50Ω input connectors and provide a voltage gain of 2:

$$G_{XFMR} = 2 \qquad \textbf{(EQ. 1)}$$

In a production system, the transformer might be replaced by an IF SAW which also has differential output drive capability. Please observe from the schematic diagrams that the transformer introduces a dc short from the input connector to ground.

With the DVGA set to maximum gain, the total analog gain from the input connector to the ADC is 33.8dB and an input level of -23.8dBm will drive a full-scale input at the ADC. With the DVGA set to minimum gain, the total analog gain is -8.3dB and a +18.3dBm input level is required to drive the ADC to full scale. Typically, the AGC reference level will be set such that the ADC will never see full scale and the lowest gain setting of the DVGA will not be used.

The total gain of the DRCS Board, including both the analog and digital parts is best described by the equation,

$$G_{TOTAL} = G_{XFMR}G_{DVGA}G_{LC}G_{DDC}, \qquad \textbf{(EQ. 2)}$$

where the first term has already been introduced and the others will be in subsequent sections of this manual.

The noise figure of the DRCS Board is 13dB and is calculated in the ADC section on page 3.

DVGA

The DVGA is a 350MHz amplifier that has a digitally-controlled voltage gain range from -12 to +30dB in 6dB steps. It has a 3rd-order output intercept point of 24dB at 150MHz and an output noise spectral density of $69 nV/\sqrt{Hz}$. At 150MHz, the data sheet plots place the maximum gain at about 28.5dB or,

$$G_{DVGA} = (0.21) \cdot 2^{AGAIN}, \qquad \textbf{(EQ. 3)}$$

where $AGAIN$ is the 3-bit data word into the DVGA digital input of channel A. Refer to the CLC5526 data sheet for further details.

The DVGA, in conjunction with the DDC/AGC, forms an automatic leveling loop that compresses the dynamic range of the input IF signal prior to sampling by the ADC. By doing so, it extends the dynamic range of the ADC by as much as 42dB. The loop dynamics and threshold of the AGC are set by programming the control registers within the DDC/AGC. It is also possible to inhibit the loop and force specific DVGA gain values. These topics are addressed later within this document.

Noise Filter

A simple noise filter resides between the DVGA and ADC. Its only purpose is to attenuate noise from the DVGA that appears at the ADC sampling image frequencies. Because of its simplicity, it does not have the ability to sufficiently reject signals from the antenna that are located at the sampling images. It is assumed that a SAW filter will precede the DVGA and provide this capability. The usefulness of the noise filter is due to the fact that both the DVGA and ADC have wide bandwidths and so there are many sampling images that fall in band. Each of these will add noise power to the output if they are not attenuated. See Figure 2.

The nominal component values for the filter provide a center frequency of 150MHz, a 3dB bandwidth of 18MHz, and an insertion loss of 0.7dB. Assuming an ADC sample rate of 52MSPS, the filter provides about 4dB of attenuation at the closest image frequency which is at 162MHz (Figure 2). The attenuation at the image frequencies not shown will of course be greater. More attenuation is possible by increasing the Q of the filter, but this would make the center frequency tolerance more critical and also increase the group delay through the filter. (The damping of the AGC loop is negatively impacted by large group delays.) More attenuation will also be achieved if the IF is moved further away from 156MHz.

To change the IF frequency of the DRCS Board, the noise filter components must be changed. The equations below pertain to Figure 3 and provide a means of computing the new values:

$$\omega_c = \frac{1}{\sqrt{L_1 C_T}} \qquad \textbf{(EQ. 4)}$$

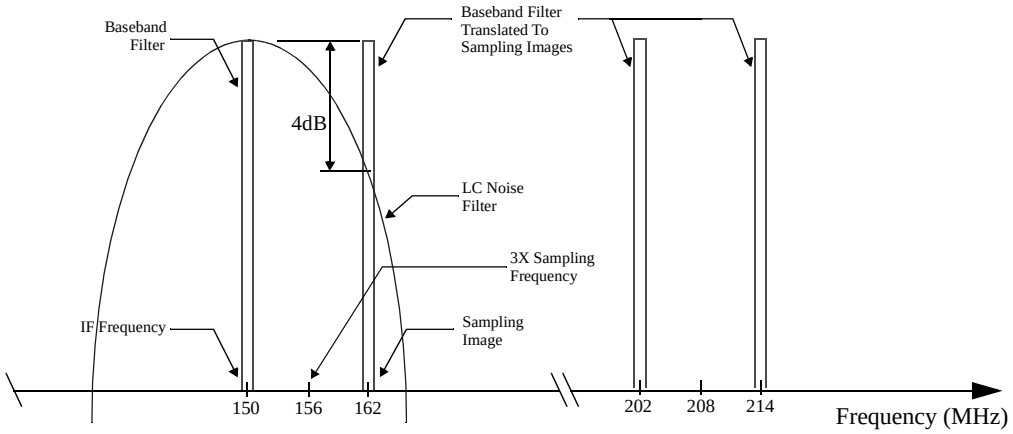

Figure 2 Illustration of the need for noise filter attenuation at the sampling images.

$$\omega_{BW} = \frac{1}{R_T C_T} \quad \textbf{(EQ. 5)}$$

$$G_{LC} = 1 + \frac{R_T}{Q_L} \cdot \sqrt{\frac{C_T}{L_1}} \quad \textbf{(EQ. 6)}$$

$$C_T = C_{93}/2 + C_{99} + 1.5pF \quad \textbf{(EQ. 7)}$$

In these equations, $C_{93} = C_{94}$, $R_T = 600 \parallel 1K = 375\Omega$, G_{LC} is the filter gain at ω_c, and Q_L is the quality factor of the inductor at ω_c.

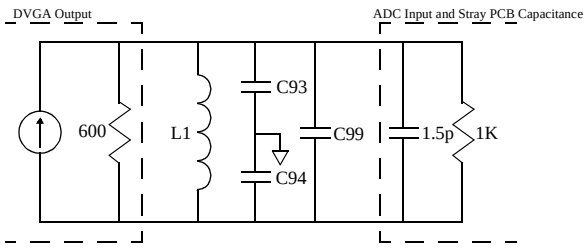

Figure 3 Noise filter components for AIN1.

In addition to setting the center frequency of the filter, capacitors C93 and C94 absorb the transient current that is sourced out of the ADC coincident with the sampling instant. It is recommended that C_{93} and C_{94} be no less than 20pF.

The frequency response of the noise filter can be checked at spot frequencies by observing either the CLC5902 Mixer AI or BI outputs in debug mode with the NCO set to 0 frequency and 0 phase.

ADC

The ADC is a 12 bit, wideband converter capable of inputs as high as 300MHz at sample rates of 52MSPS. The SNR for an input 3dB below the full scale input of $2V_{PP}$ differential is 62dBFS at an IF frequency in the range of 150MHz. For levels much below this, however, the SNR improves to 68dBFS (or, $55nV/\sqrt{Hz}$ at 52MSPS). This behavior is due to the fact that the large-signal, high-frequency SNR is dominated by clock jitter. Communication systems such as GSM require minimum SNRs of no better than 9dB which can be achieved at input levels of 59dB below full scale. Therefore, the ADC acts as though it were a 68dB device for these systems (Figure 4). The digital filters following the ADC provide processing gain that

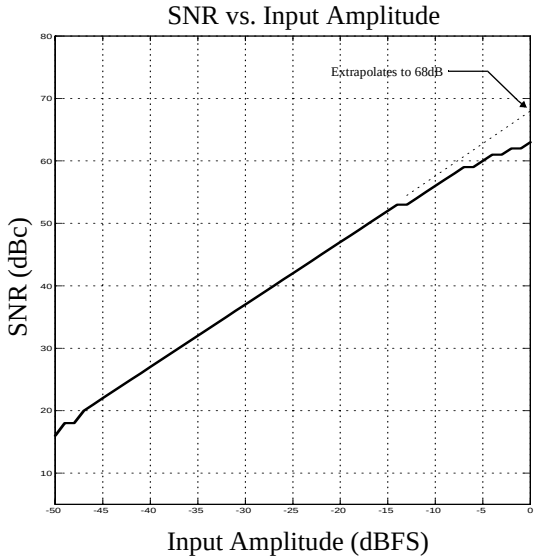

Figure 4 CLC5956 SNR extrapolates to 68dBFS.

improve further upon this by 24dB (factory default configuration). Assuming that a single sampling image interferes at a level of -4dB (Figure 2), the total noise voltage density at the ADC input is,

$$\sqrt{55^2 + 69^2(1 + 10^{-4/10})} = 98nV/\sqrt{Hz}. \quad \textbf{(EQ. 8)}$$

When this is referred through the 33.8dB maximum gain to the input connector, this yields a 13dB noise figure for the DRCS Board.

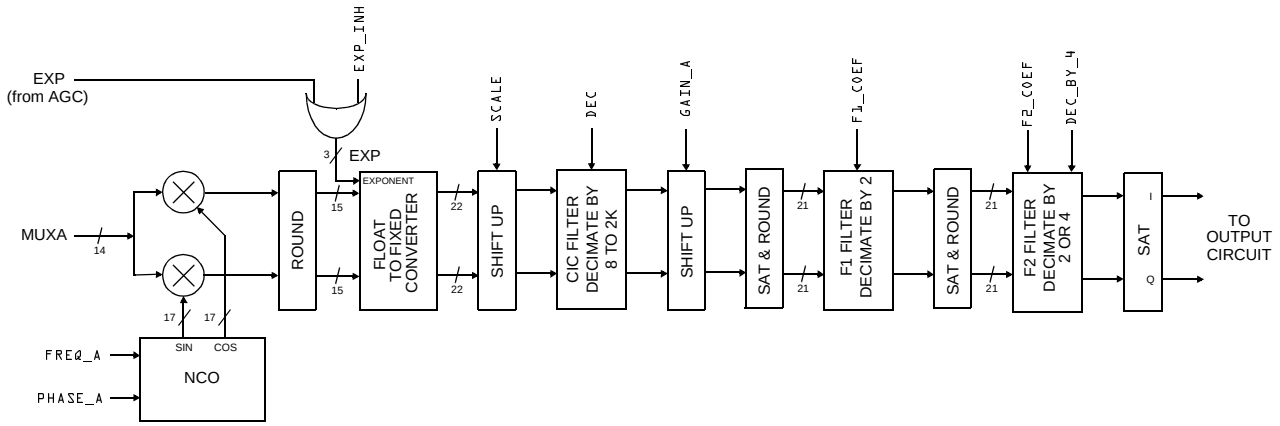

Figure 5 CLC5902 down converter, channel A.

The digital output format of the ADC is two's complement. For further information, consult the CLC5956 data sheet.

DDC

The ADC outputs feed into the two channel DDC/AGC. This part consists of two down converter channels (DDC) and automatic gain control (AGC) loops. The DDC performs the final mix to baseband and baseband filtering (see Figure 5).

The NCO can tune across the full Nyquist band with 32 bit precision. With phase dither enabled, the spurious performance is -101dBc or better and SNR is 84dB. The frequency and phase of the two channels are completely independent. In addition, the phase dither of the two are uncorrelated.

The baseband filtering is performed by a cascade of three decimating FIR filters. The overall decimation ratio can be programmed from 8 to 16,384. The two final filters feature 21 and 63 user-programmable taps, respectively. A set of tap coefficients are published in the CLC5902 data sheet which provide adequate filtering to meet the GSM blocker and interferer requirements. The frequency response for these at a sample rate of 52MSPS is shown in Figure 6.

Although the ADC combined with the processing gain of the digital filters provides 92dB of instantaneous SNR, this is not enough to meet the requirements of the GSM900 specification without some analog filtering to attenuate the blocker. Nonetheless, the digital filters can be used to relax the requirements on the analog filter. In particular, the digital filters can meet the reference interference level of *ETSI GSM 05.05 paragraph 6.3* without any assistance from the analog filter. Further, the blocker performance of *ETSI GSM 05.05 paragraph 5.1* can be met with only minor assistance from the analog filter.

The FLOAT TO FIXED CONVERTER within the DDC will match any change in gain by the DVGA with a compensating digital gain change. It does this by treating the complement of the DVGA control word as an exponent to the ADC output. The overall effect of this is to make the

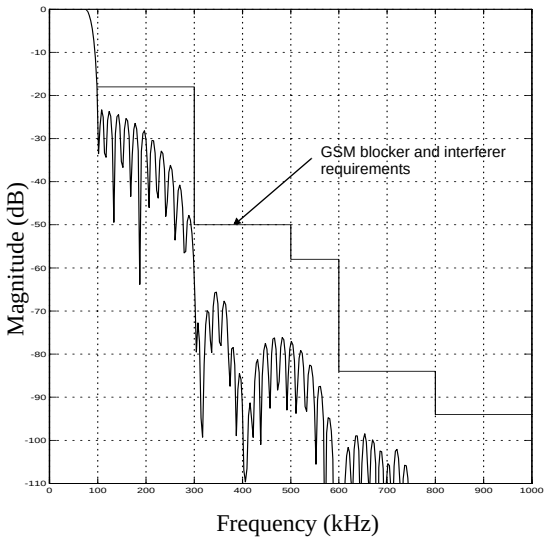

Figure 6 Frequency response of down converter

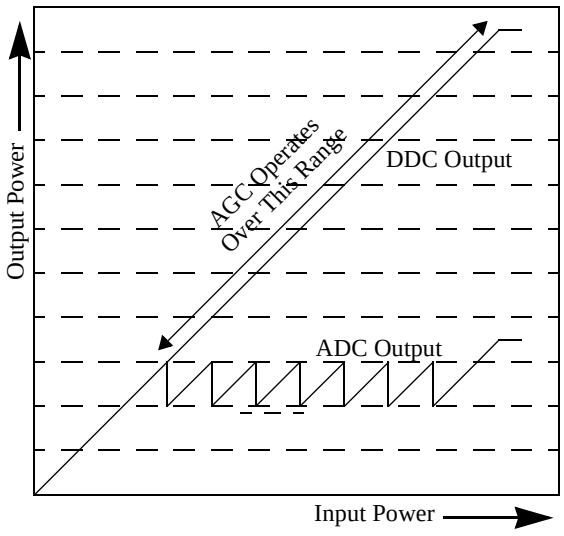

Figure 7 ADC and DDC output level vs. input level

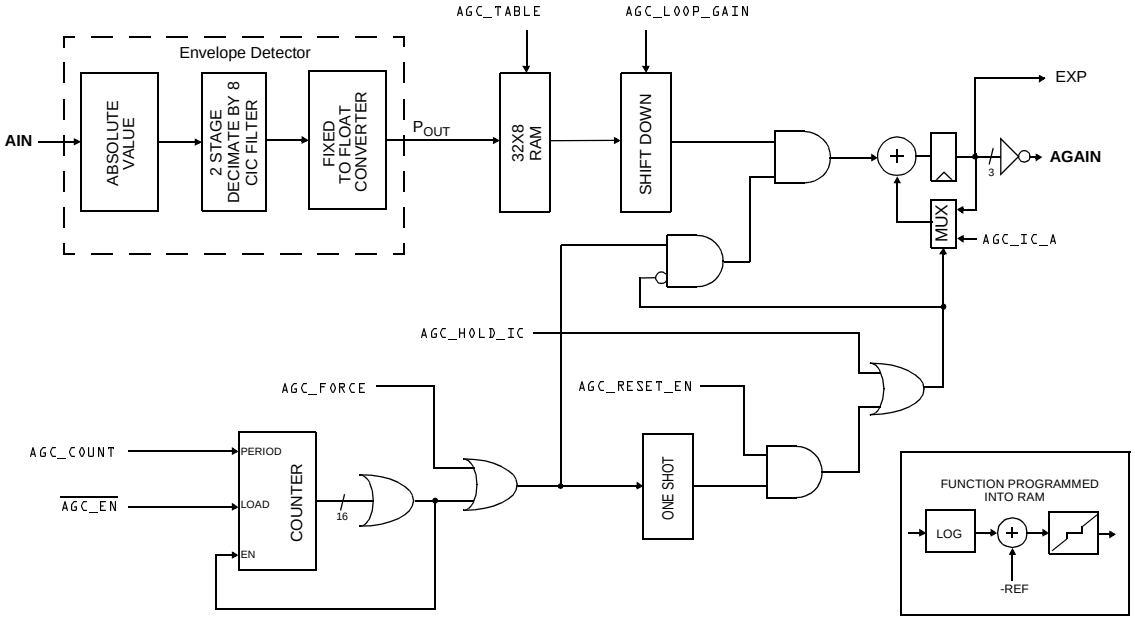

Figure 8 AGC circuit, channel A.

DRCS Board appear as a fixed gain channel with extremely large dynamic range as shown in Figure 7. This mode can also be inhibited by asserting EXP_INH. An expression for the gain through the DDC channel A is,

$$G_{DDC} = \frac{1}{2}(DEC+1)^4 \cdot 2^{[SCALE-44-AGAIN\cdot(1-EXP\_INH)]} \cdot 2^{GAIN} \cdot G_{F1} \cdot G_{F2} \quad \text{(EQ. 9)}$$

$$G_{F1} = \frac{\sum_{i=1}^{21} h_1(i)}{2^{16}}, \quad \text{(EQ. 10)}$$

$$G_{F2} = \frac{\sum_{i=1}^{63} h_2(i)}{2^{16}}. \quad \text{(EQ. 11)}$$

The numerators of G_{F1} and G_{F2} equal the sums of the impulse response coefficients of F1 and F2, respectively. For the STD and GSM sets, G_{F1} and G_{F2} are nearly equal to unity. Observe that the *AGAIN* term in (EQ. 9) is cancelled by the corresponding term appearing in (EQ. 3) so that the entire gain of the DRCS Board is independent of the DVGA setting when EXP_INH=0. The $\frac{1}{2}$ appearing in (EQ. 9) is the result of the 6dB conversion loss in the mixer.

AGC

The AGC loop for channel A is shown in Figure 8. Each channel has its own loop. The ADC output power is measured with an envelope detector and used to adjust the DVGA gain. Envelope detection is performed by an absolute value circuit followed by a lowpass filter whose response is shown in Figure 9. The filtered signal is used

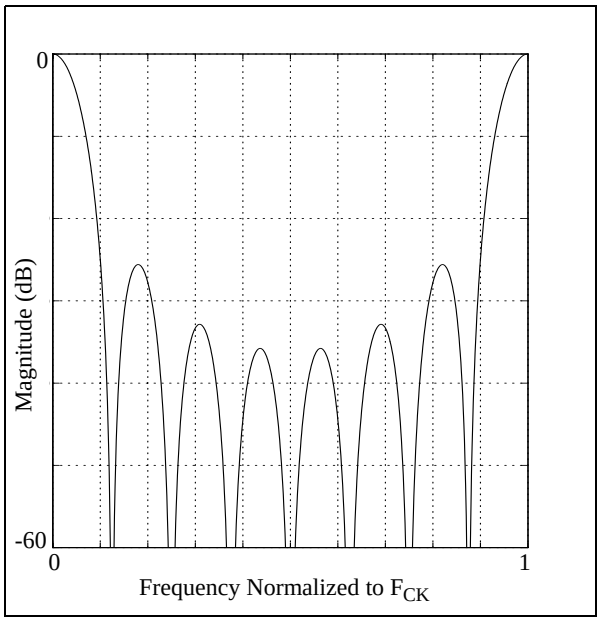

Figure 9 Frequency response of envelope detector filter.

to address a lookup table which generates an error signal based on the programmed threshold, deadband and loop time constant targets. This error is integrated to produce the 3 bit control signal for the DVGA. Integrator gain is

programmable via the shifter preceding it to allow loop time constants that can be varied by factors of 2. Fractional control of time constant can be achieved by altering the slope of the transfer function stored within the lookup table.

In the course of measuring ADC power, the absolute value block within the envelope detector also generates a second harmonic of the aliased IF frequency. For example, an IF of 150MHz aliases to -6MHz at the ADC output when the sample rate is 52MHz. The absolute value block produces from this a dc term and a second harmonic at -12MHz, the latter of which is rejected by the low pass filter. If the alias frequency is too low, though, its second harmonic will fall within the passband of the filter and a clean power detection will not occur. This problem can be avoided by choosing the IF and sample rates such that the alias frequency magnitude is greater than $F_{CK}/16$.

The user interface software makes programming of the AGC very easy. The user need only specify the loop time constant, reference and deadband and from these, the lookup table values and shifter values are computed. As shown in Figure 10, deadband in excess of 6dB shows up as hysteresis. Hysteresis will eliminate excessive DVGA gain changes caused by the input signal level dwelling at a transition point.

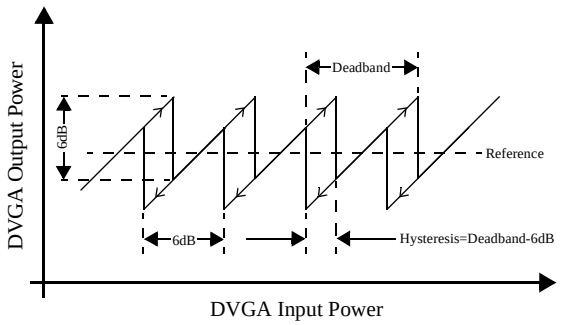

Figure 10 Relationship between deadband and hysteresis.

The AGC has several operating modes. The simplest is the free-run mode where the loop is closed continuously and the DVGA gain setting is constantly updated in response to the signal level applied to the board. This mode is easiest to use and is probably suitable for most applications. The default configuration of the DRCS Board and user software is for this mode. The other mode is a gated mode and is useful, for example, in TDMA systems when one wishes the AGC to be active only during the power ramp up. In this mode, the loop is active when the gate signal is applied and then opens when the gate is removed. The gate signal can be an external pulse whose width defines the AGC active period. Alternatively, the gate can be an edge which starts a counter within the DDC/AGC. The AGC active period is then the time it takes for the counter to reach its terminal value. By using the configuration registers, it is possible to write the initial gain condition of the loop into the integrator and also to read the final gain value from this integrator. Consult the CLC5902 data sheet for further details.

Data and Clock Outputs

The CLC5902 outputs several standard serial formats for interface to a DSP. These formats can be specified by loading the appropriate values in the CLC5902 registers. The CLC5902 datasheet provides complete information. The default setup of the DRCS Board is PACKED, MUX_MODE=1, and FORMAT=2. These settings provide a 24-bit serial output word, a frame sync output pulse once for each I/Q pair, and the outputs for channel A and B muxed onto the single output pin AOUT. The serial outputs and control signals are available at the Eurocard connector J1. This connector mates directly to the data capture board which can be used to transfer data to a PC. The serial output is also available from the 16-pin DSP interface header. Note that AND gate U12 is not factory loaded but a location is provided for compatibility with previous versions of the DRCS Board. **The trace from pin 2 to 4 of U12 must be cut before installing it.**

The default serial output configuration is compatible with the TMS320C54X serial input. Figure 11 shows the timing. To interface to the ‘C54X, set the DSP serial port in continuous mode (FSM bit set to 0) with frame ignore enabled (FIG bit set to 1). In this mode the 24-bit words may be read as 3 groups of 8 bits. The overall input stream of four 24-bit words is read as twelve 8-bit words for later reassembly by the DSP.

The parallel outputs from the CLC5902 are also available on the Eurocard connector J1. The parallel output bus of

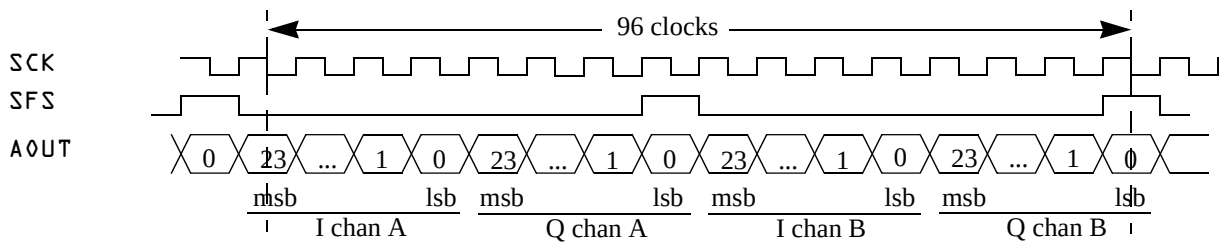

Figure 11 DSP Interface Timing Diagram

the CLC5902 is 16 bits wide and a set of enable and address lines allow the I/Q data from channels A and B to be accessed from 8 internal registers. These control lines also connect to J1. A set of DIP switches SW1D allow the enable and address lines to be statically set. **These switches must be open if the Data Capture Board is used for parallel data capture.**

A simple inversion of the MSB converts two's complement data to offset binary data. In this format the MSB has the same polarity as all the other bits so that negative full scale is all zeroes and positive full scale is all ones. An inverter is provided on the board to generate this output coding for the parallel output. The inverted MSB is brought out on pin 3A of J1.

Refer to the CLC5902 data sheet for further information on the parallel output.

Probing of DDC/AGC Debug Nodes

The user has the ability to probe internal nodes within the CLC5902 by selecting the desired node using the internal configuration registers. The node is then switched on to the 20-bit wide parallel debug bus which is a collection of output pins that are re-assigned to this function when the debug mode is enabled. (Refer to the CLC5902 data sheet for pin assignments, output data formats, and configuration register parameters.) Both the DRCS Control Panel and Data Capture Board support this mode.

When this mode is enabled, signal pin SCK is re-configured as a data strobe with the proper timing for the selected internal node. This gives the user the ability to debug his design when trouble arises. The internal nodes available for probing include the outputs of the mixers, CIC filters, and AGC power detectors.

µController

The COP8 microcontroller contains preprogrammed data to load into the CLC5902. When the board is powered up or the reset switch is closed, the COP8 reads the 8-position dip switch SW2 to determine which set of data to load. The CLC5902 is loaded, the LEDs alternate briefly, and the COP8 enters an idle loop awaiting further serial communication. To change the operating program in the CLC5902, change the SW2 dip switch setting and press the 'RESET' switch. The new data is loaded and the COP8 again enters the idle loop.

The COP8 provides an RS-232 serial port for connection to an external controller on connector J9. This port allows the DRCS Control Panel software to access the DDC registers thus providing greater configuration flexibility.

System Clock

The DRCS Board is equipped with an SMA connector labeled as CLK so that an external clock signal can be applied. However, the board is factory-configured with an on-board 52MHz crystal oscillator (Y2) and so the external clock signal is not needed. **If the user wishes to use an external clock, the socketed oscillator must first be removed.** The CLK connector hooks to a sine-to-PECL clock converter to drive the ADCs. This circuit requires a 2-3V_{PP} (10 to 16dBm) sinewave at the clock SMA connector. The PECL clock is further converted to a TTL clock for use by DDC/AGC.

For optimal ADC performance the clock must have less than 1psec jitter. Higher levels of jitter will spread out the spectrum of any applied signals. In a laboratory environment, we suggest the use of a low phase noise synthesizer such as the HP8643 or the HP8644 as a sinewave source. Excessive phase noise will cause unacceptable levels of jitter.

DRCS Control Panel Software

The DRCS Control Panel (*drcscp.exe*) requires Windows 95/98/NT and a free serial port to operate. Run *setup.exe* from the CD ROM to copy the appropriate files to your hard drive and build the necessary directory structure. Run *drcscp.exe* to start the program. To configure the COM port, choose **Configure I/O** from the **File** menu.

The DRCS Control Panel is a program interface which allows the CLC5902 configuration registers to be programmed. All register settings are controlled from the four tabs on the left. The **Registers** page allows you to view a summary of the register values that are down-loaded to the CLC5902. Except for the **Registers** page, each page has a **Send Page** or **Send** button. When pressed, the register values associated with that page are down-loaded to the CLC5902. In addition, a **Send All Data** command is available under the **File** menu. Although the registers within the CLC5902 can also be read, the present version of the software does not provide this capability.

The configuration data entered into the various pages can be written to a *.dcp* configuration file. This provides a convenient method of retrieving previous configurations because these files can also be read into the DRCS Control Panel. The file is ASCII and has one line for each byte that is written to the CLC5902. The first column is the address and the second is the data. Both are in hex format. The **Load Configuration** and **Save Configuration** commands can be found under the **File** menu.

When you start the DRCS Control Panel, it will load the last used *.dcp* file within the Data subdirectory. If you have not yet created one, it will look for *default.dcp*. If *default.dcp* is not found, it will use a set of hard-coded defaults for everything except FIR Filters F1 and F2. For the filters, the program will search for *default.f1* and *default.f2*. If they are not found, zeros will be loaded for the coefficients.

The data entry fields are designed to allow values to be entered using pulldown menus or edit boxes in familiar engineering terms, as opposed to the integer values that are required by the CLC5902. The engineering values are converted to the appropriate integer values and appear on the **Registers** page. For example, when -150.03 is entered into **Freq**, **Channel A**, the **Registers** page displays the value 493095284 for **FREQ_A**. When the mouse is held over a

data entry field, a balloon is displayed which describes the function. If a value is entered that is outside the valid range, a warning is displayed.

For the most part, the data entry fields are intuitive given an understanding of the CLC5902 data sheet. A few exceptions are noted below:

Channels Page - **Freq** is the frequency of the NCO. You can either enter the IF frequency at the ADC input or the aliased frequency at the ADC output. To down-convert without a phase inversion, enter the negative of the frequency of interest. For example, an IF frequency of 150.03MHz requires an entry of -150.03 for no phase inversion. An alternative is to recognize that 150.03MHz aliases to -5.97MHz when **FCK** is 52MHz and, for no phase inversion, enter +5.97. **FCK** refers to the sample rate of the DRCS Board, which has a factory default of 52MHz. `Scale` refers to the bit shift prior to the CIC filter (Figure 5). **Scale (Calculated)** is calculated by the program and is the value required of `Scale` to maintain the gain of the DDC up to and including the CIC filter to unity or just less. It changes when **CIC Decimation** changes. **Scale Adjust** is a bit shift value added to `Scale` prior to downloading to the CLC5902. You can enter either a positive or negative value with the restriction that **Scale Adjust** + **Scale (Calculated)** fall within the range of 0 to +44 inclusive. A warning is issued for values entered outside this range. **Gain** refers to the bit shift after the CIC filter (Figure 5).

AGC Page - The popup menus for initial conditions and gains refer to the gain of the DVGA. The loop dynamics for the AGC are set in the lower left box. Press the Calculate button after entering values for **Threshold**, **Deadband**, and **Time Constant** and the AGC lookup table values and `AGC_LOOP_GAIN` are computed.

Output Page - **SCK Rate** must be selected low enough to allow all serial bits to exit within one output sample period. See the CLC5902 data sheet for further discussion.

Filter Data Page - The coefficient values for each of the symmetric FIR filters can be manually entered or loaded from an ASCII text file using the **Load** button. The file must have a *.f1* extension for **FIR Filter 1** and a *.f2* extension for **FIR Filter 2**. The file format is one signed integer coefficient per line and the number of lines must equal the number of unique coefficients. Also, there must be no blank space before the values in the files.

There is no handshaking between the DRCS Board and the PC. If the system is operating correctly, all the LEDs will light during transmission and only LED1 will remain lit at the completion of transmission. If the transmit sequence is upset, reset the DRCS Board and re-send.

Data Capture Board Settings

The Data Capture Board and companion software provides the ability to capture data from the DRCS Board as well as a variety of analog-to-digital converter products. When used together, it is important that the settings of one board do not conflict with those of the other. If any conflicts occur, it will be with entries on the **Output** page of the DRCS Control Panel and often will result in the data being unintelligible. The first step to ensure compatibility is by making sure all switches on the Data Capture Board are off. The next step is to obtain a copy of the Data Capture Board documentation.

Default Configuration and SW2 Settings

The CLC-DRCS-PCASM is shipped configured with an on-board 52MHz crystal clock source. The LC noise filter has an 18MHz bandwidth centered at 150MHz. These

	SW2 Switch Settings (4321)						
Register Name	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**
DEC	47	3	7	47	47	47	47
DEC_BY_4	0	0	0	0	0	0	0
SCALE	21	36	32	21	21	21	21
FREQ_A	-493,095,283[a]	-493,095,283	-493,095,283	0	-479,054,044[b]	-479,054,044	-479,054,044
FREQ_B	-493,095,283	-493,095,283	-493,095,283	0	-1,156,337,348[c]	-479,054,044	-1,156,337,348
DITH_A/B	1	1	1	1	1	1	0
AGC_LOOP_GAIN	1[d]	1	1	1	1	1	1
DEBUG_EN	0	1	1	0	0	0	1
TAP_SEL	0	6 (F1 AI Input)	6 (F1 AI Input)	12 (NCO AI)	0	0	8 (NCO A cosine)

Table 1 [e]CLC5902 configurations for SW2 segment 1 settings (continued in Table 2).

a. With FCK=52MHz, -493,095,283 (0xE29BF68D) provides an NCO frequency of -5.97MHz. F_{IN}=150.03MHz aliases to 150.03MHz-3*52MHz=-5.97MHz

b. With FCK=52MHz, -479,054,044 (0xE3723724) provides an NCO frequency of -5.8MHz.

c. With FCK=52MHz, -1,156,337,348 (0xBB13B13C) provides an NCO frequency of -14MHz.

d. Yields a loop time constant of 1.5µs for FCK=52MHz and either position of switch number 6.

e. See Table 3 for register values common to all SW2 configurations.

	SW2 Switch Settings (4321)					
Register Name	**0111**	**1000**	**1001**	**1010**	**1011**	**1100**
DEC	47	23	1	47	47	23
DEC_BY_4	0	1	0	0	0	1
SCALE	21	25	40	21	21	25
FREQ_A	-479,054,044	-493,095,283	-493,095,283	0	0	-479,054,044
FREQ_B	-1,156,337,348	-493,095,283	-493,095,283	0	0	-1,156,337,348
DITH_A/B	0	1	1	0	0	1
AGC_LOOP_GAIN	1	1	1	0[a]	1	1
DEBUG_EN	1	0	1	1	1	0
TAP_SEL	10 (NCO B cosine)	0	6 (F1 AI Input)	12 (Mixer AI)	14 (Mixer BI)	0

Table 2 [b]CLC5902 configurations for SW2 segment 1 settings (continued from Table 1).

a. Yields a loop time constant of 3.0µs for FCK=52MHz and either position of switch number 6.
b. See Table 3 for register values common to all SW2 configurations.

values are designed to operate in combination with SW2 configured to **0000|0000** as discussed below.

It is advised that the reader has a copy of the CLC5902 data sheet available while reading the following material even though it is not necessary to fully understand that document before using the DRCS Board. Immediate results can be obtained most easily when the DRCS Board is used in conjunction with the DRCS Control Panel software, Data Capture Board and the capture board software. The DRCS Control Panel software allows a user to communicate with the DRCS Board using plain-English commands from a menu. If the user wishes to configure the board without a PC, though, SW2 is the only other means apart from building their own interface. The set of configurations available with SW2 is described below. Requests for configurations not presently available should be directed to the factory.

On power up (or on reset), the COP8 reads the value of DIP switch SW2 and programs the CLC5902 configuration registers. SW2 can be thought of as being segmented into two pieces. Segment 1 comprises switch positions 1 through 4. These program the CLC5902 as shown in Table 1 and Table 2. The CLC5902 register values that are common to all of these configurations are given in Table 3.

Segment 2 is comprised of the remaining switches, each of which programs an independent function as shown in Table 4. The CLC5902 data sheet should be referenced for the F1/F2 filter coefficients corresponding to the STD Set and the GSM Set coefficients. The AGC lookup table values corresponding to the two choices of AGC dynamics are given in Table 5.

Register Name	**Value**
GAIN_A/B	2
RATE	1
SOUT_EN	1
SCK_POL	0
SFS_POL	0
RDY_POL	0
MUX_MODE	1
PACKED	1
FORMAT	2 (24 bit)
PHASE_A/B	0
A_SOURCE	0
B_SOURCE	1
TEST_REG	4096

Table 3 Common register values for segment 1 of SW2.

		SW2 Switch Settings	
Function	**Switch Position**	**0**	**1**
F1/F2 Coefficient Set	5	STD Set	GSM Set
[a]AGC Dynamics (Threshold/Dead-band)	6	-12dB/12dB	-15dB/15dB
AGC Mode	7	Continuous	Burst
Dither	8	On	Off

Table 4 SW2 Segment 2 settings.

a. AGC_LOOP_GAIN is controlled from segment 1. See Table 1 and Table 2.

	Decimal Values (Hex)	
Decimal Register Address (Hex)	-12dB/-12dB	-15dB/-15dB
128 (0x80)	-88 (0xA8)	-82 (0xAE)
129 (0x81)	-88 (0xA8)	-82 (0xAE)
130 (0x82)	-75 (0xB5)	-68 (0xBC)
131 (0x83)	-66 (0xBE)	-60 (0xC4)
132 (0x84)	-61 (0xC3)	-54 (0xCA)
133 (0x85)	-56 (0xC8)	-49 (0xCF)
134 (0x86)	-53 (0xCB)	-46 (0xD2)
135 (0x87)	-50 (0xCE)	-43 (0xD5)
136 (0x88)	-47 (0xD1)	-40 (0xD8)
137 (0x89)	-42 (0xD6)	-36 (0xDC)
138 (0x8A)	-39 (0xD9)	-32 (0xE0)
139 (0x8B)	-36 (0xDC)	-29 (0xE3)
140 (0x8C)	-33 (0xDF)	-26 (0xE6)
141 (0x8D)	-29 (0xE3)	-22 (0xEA)
142 (0x8E)	-25 (0xE7)	-18 (0xEE)
143 (0x8F)	-22 (0xEA)	0 (0x00)
144 (0x90)	-19 (0xED)	0 (0x00)
145 (0x91)	-15 (0xF1)	0 (0x00)
146 (0x92)	0 (0x00)	0 (0x00)
147 (0x93)	0 (0x00)	0 (0x00)
148 (0x94)	0 (0x00)	0 (0x00)
149 (0x95)	0 (0x00)	0 (0x00)
150 (0x96)	0 (0x00)	0 (0x00)
151 (0x97)	0 (0x00)	0 (0x00)
152 (0x98)	0 (0x00)	0 (0x00)
153 (0x99)	0 (0x00)	20 (0x14)
154 (0x9A)	17 (0x11)	23 (0x17)
155 (0x9B)	20 (0x14)	26 (0x1A)
156 (0x9C)	22 (0x16)	29 (0x1D)
157 (0x9D)	27 (0x1B)	34 (0x22)
158 (0x9E)	30 (0x1E)	37 (0x25)
159 (0x9F)	34 (0x22)	40 (0x28)

Table 5 AGC lookup table values for the two AGC dynamics options.

For either selection, a loop time constant τ of 1.5µs results when AGC_LOOP_GAIN=1 and F_{CK}=52MHz. Each increase of AGC_LOOP_GAIN by 1 will decrease τ by a factor of 2. Halving F_{CK} will increase τ by a factor of 2.

Table 6 gives the configuration register values for each of the AGC modes associated with switch position 7 as mentioned in Table 4.

	SW2 Switch Position 7 Settings	
Register Name	0	1
AGC_HOLD_IC	0	0
AGC_RESET_EN	0	0
AGC_FORCE	1	0
EXP_INH	0	0
AGC_COUNT	2815	2815
AGC_IC_A/B	32	32

Table 6 Register values corresponding to SW2 switch position 7.

Any of these default configurations can be modified by using the DRCS Control Panel software. See the DRCS Control Panel Software section on page 7.

Initial Operation

This procedure will verify proper operation of the DRCS Board and Data Capture Board

It is assumed that the you will be conducting this test in conjunction with the Data Capture Board. If not, you will have to solve the problem of data capture. Refer to the CLC5902 data sheet to understand its data capture requirements. The sequence below requires an unmodulated source such as an HP8643 or the HP8644.

1. If you have not already done so, install the DRCS Control Panel and Data Capture Board software.
2. Connect +5V to VCC and ground to GND of connector J3 on the Data Capture Board. When the boards are connected together in the next step, these connections will power both boards. Note that VEE is not required because neither board needs a negative power supply.
3. Connect J1 of the DRCS Board to J1 of the Data Capture Board.
4. Connect a serial cable from the PC to J9 on the DRCS Board.
5. If two serial ports are available on the PC, connect the other to J9 of the Data Capture Board. If not, the single port will have to be shared.
6. Make sure that all DIP switches on both boards are set to off.
7. Turn on the power supply.
8. Start the DRCS Control Panel and Data Capture Board software.
9. Configure the COM ports for the DRCS Control Panel and Data Capture Board software. The COM

port setup for the DRCS Control Panel is located under **File**, **Configure I/O**. The COM port setup for the Data Capture Board software is accessed by right-mouse-button clicking anywhere on the program window and selecting **Configure I/O**. Note that power must be applied to the Data Capture Board and the serial cable must be connected in order for the software to accept the COM port configuration.

10. Connect a -10dBm sinewave at 150.00MHz to the DRCS Board AIN1 input.

The DVGA should servo to a gain of either 0dB (AGAIN=2) or +6dB (AGAIN=3) and the ADC should be operating at a level of -16 or -10dBFS. Because `EXP_INH` is not asserted for this configuration, the DDC output (which will be observed below) should be at -32dBFS. This can be computed from the gain equations presented earlier and the register data provided in the **Registers** page of the DRCS Control Panel.

The first measurement will be to use the debug mode of the CLC5902 to probe the output of the ADC.

11. On the **Channels** page of the DRCS Control Panel, enter 0 for **Freq** within the **Channel A** box to set the frequency of the channel A NCO to zero. Also check **Debug Enabled** and select **Mixer AI** from the **Probe at** pulldown menu within the **Common** box. The screen should appear as in Figure 12 Click on the **Send Page** button. Immediately following this, a data transfer indicator box will appear on the monitor and all the LEDs on the DRCS Board will light momentarily.

12. On the **Configure Capture** screen of the Data Capture Board software, choose **Capture Debug** within the **Mode** box. Then choose **Upper 18 Bits** within the **Bits** box. Press **OK.** The screen should appear as in Figure 13.

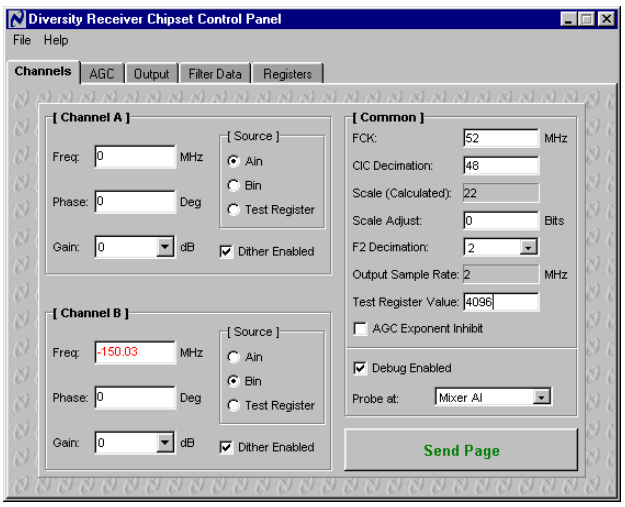

Figure 12 Screen configuration for step 11.

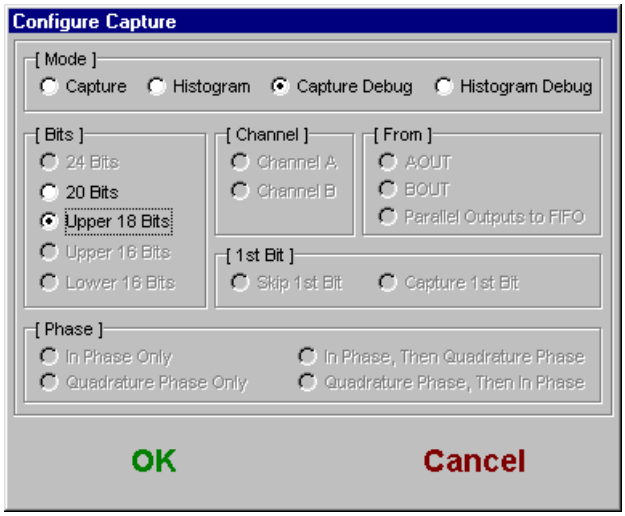

Figure 13 Screen configuration for step 12.

13. Press **Start** on the front panel of the Data Capture Board software window. When the completion bar reaches 100%, the captured data will be written to the file C:\TEMP\DATA.DAT.

If the TEMP directory did not previously exist, the software will create it. You can also specify a different file name and directory by right-mouse-button-clicking on the Data Capture Board software window and choosing the **Change Data File** command.

The values in DATA.DAT represent 24-bit 2's complement integers. When **Mixer AI** is selected, only the upper 15 bits are non-zero. These numbers can be converted to signed fractional values using the following MATLAB script:

```
load c:\temp\data.dat
data=data/2^23;
data=data.*(data<1)+(data-2).*(data>=1);
```

Verify that the waveform is sinusoidal with amplitude of either -16 or -10dBFS and frequency of 150MHz-(3*52MHz) = -6MHz.

The next measurement will be to observe the output of the DDC.

14. On the **Channels** page of the DRCS Control Panel, enter -150.03 for **Freq** of **Channel A**, uncheck **Debug Enabled**. The screen should appear as in Figure 14. Click on the **Send Page** button.

15. Choose **Capture** within the **Mode** box of the **Configure Capture** screen of the Data Capture Board software. Then choose **24 Bits** within the **Bits** box and **Capture 1st Bit** within the **1st Bit** box. Finally, choose **Channel A** from the **Channel** box and press **OK**. The screen should appear as in Figure 15.

16. Click **Start** on the front panel of the Data Capture Board software window.

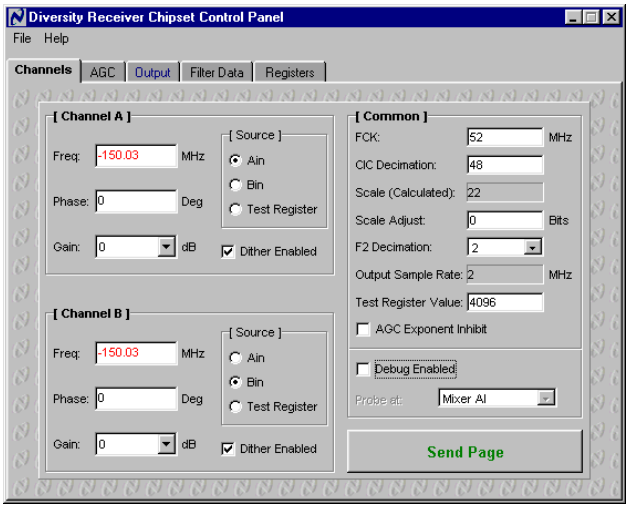

Figure 14 Screen configuration for step 14.

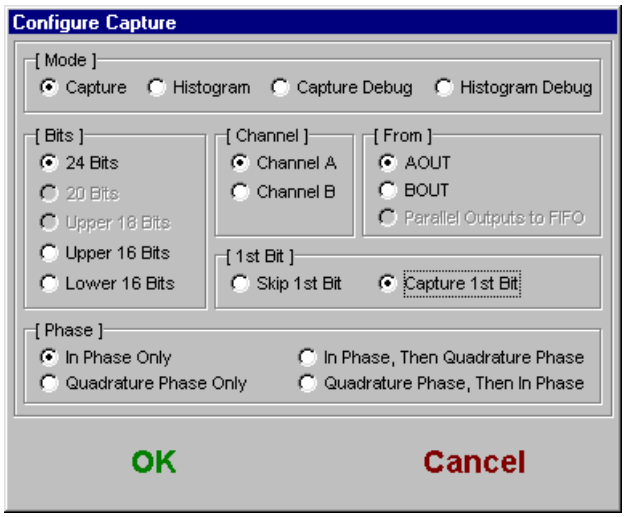

Figure 15 Screen configuration for step 15.

The values in the file again represent 24-bit 2's complement integers except now all 24 bits are non-zero. The same MATLAB script can be used to convert to signed fractional values. **Regardless of the true width of the word being captured, the Data Capture Board will always write 24-bit, 2s complement numbers to DATA.DAT. The only exception to this is when probing AGC CIC A+B in which case each number represents two appended 9 bit numbers. (Refer to the CLC5902 data sheet.)**

Verify that the output is -32dBFS at frequency 150.00MHz-150.03MHz = -0.03MHz. A slight frequency offset may exist due to variations in the frequency of the on-board 52MHz crystal oscillator. Note that the output sample rate is 52MHz/192 = 270.8KHz. If you perform an FFT you will see the CLC5902's filter bandwidth reflected in the shape of the noise floor.

17. Repeat steps 10 through 13 for input AIN2 replacing all occurrences of **Channel A** with **Channel B**.

This completes the verification of the board operation.

DDC Large-Signal Nonlinearity Exercise

This exercise is intended to illustrate the two types of large-signal nonlinearity that can be encountered when the CLC5902 is incorrectly configured. Both can be observed at the input of filter F1. The same equipment is used as in the Initial Operation section on page 10.

1. Connect a -10dBm sinewave at 150.000MHz to the DRCS Board AIN1 input.
2. Load *default.dcp* by choosing **Load Configuration** from the **File** menu of the DRCS Control Panel.
3. On the **Channels** page, enter -150.005 for **Freq** within the **Channel A** box and enter 6 for **Scale Adjust** within the **Common** box. Also check **Debug Enabled** and select **F1 In AI** from the **Probe at** pulldown menu. Click on the **Send Page** button.
4. On the **Configure Capture** screen of the Data Capture Board software, choose **Capture Debug** within the **Mode** box and **18 Bits** from the **Bits** box. Click on **OK**.
5. Press **Start** on the front panel of the Data Capture Board software window.

As before, the values in DATA.DAT represent 24-bit 2's complement integers and only the upper 18 bits are non-zero. After conversion to signed values, the first 300 points when plotted look like Figure 16. This distortion is

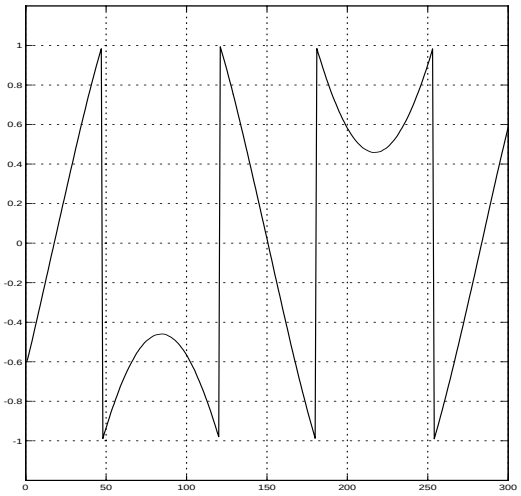

Figure 16 CIC overflow distortion.

caused by overflow in the CIC filter due to SCALE being set too large. This overflow cannot be sensed and the only way to avoid it is by making sure that SCALE is set consistent with the chosen CIC decimation value so that the CIC output is less than full scale. Figure 16 may not look exactly as yours. The exact look depends greatly on the frequency error between the on-board clock oscillator and the input source. The important characteristic of the distortion is that the positive sinusoid peaks have been translated

to negative values and the negative peaks to positive values.

6. Go back to the **Channels** page of the DRCS Control Panel and change **Scale Adjust** back to 0. Next, select **36dB** from the **Gain** pulldown menu in the **Channel A** box. Click on **Send Page**.
7. Press **Start** on the front panel of the Data Capture Board software window.

Convert the numbers in DATA.DAT to signed values and plot the first 300 points. You should see the clipping as shown in Figure 17. This represents the type of nonlinearity at all stages of the DDC other than within the CIC filter.

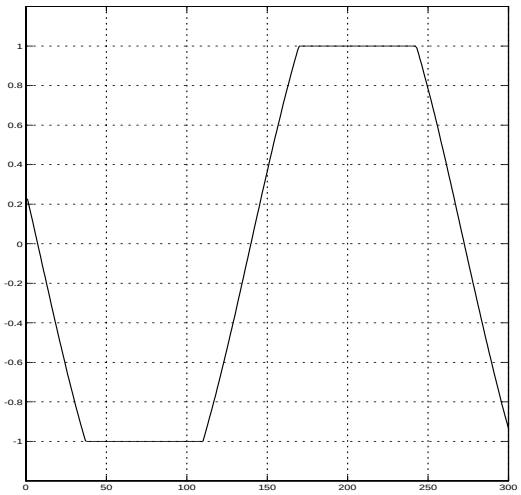

Figure 17 Data path saturation at the input of F1.

This completes this exercise.

Connector Pinouts

Table 7 describes the 64-pin Eurocard connector (J1) pinouts on the DRCS Board. Table 8 describes 10-pin JTAG header and 16-pin DSP header pinouts. The schematics provide the pinout for J9, a female DB-9 used to connect the standard RS-232 serial cable from the PC.

Power is supplied through J1. If the Data Capture Board is connected to J1, power must be connected to the power connector on the Data Capture Board.

Pin	J1 A	J1 B
1	N/C	N/C
2	GND	GND
3	MSB_T	MSB_F
4	N/C	D14_T
5	N/C	D13_T
6	N/C	D12_T

Table 7 Eurocard connector J1 pinout.

Pin	J1 A	J1 B
7	N/C	D11_T
8	N/C	D10_T
9	N/C	D9_T
10	N/C	D8_T
11	N/C	D7_T
12	N/C	D6_T
13	N/C	D5_T
14	N/C	D4_T
15	N/C	D3_T
16	N/C	D2_T
17	N/C	D1_T
18	N/C	LSB_T
19	GND	GND
20	N/C	RDY
21	SFS	SCK
22	BOUT	AOUT
23	POUT_SEL2	N/C
24	POUT_SEL1	N/C
25	POUT_SEL0	RDY
26	POUT_EN	AGC_EN
27	GND	GND
28	GND	GND
29	N/C	N/C
30	N/C	N/C
31	+5V (DIGITAL)	+5V (DIGITAL)
32	+5V (ANALOG)	+5V (ANALOG)

Table 7 Eurocard connector J1 pinout.

Pin	JTAG	DSP
1	TCK	N/C
2	GND	GND
3	TDO	SCK
4	VCC	GND
5	TMS	BFSR
6	N/C	GND
7	TRST	BDR
8	SCAN_EN	GND
9	TDI	GND
10	GND	GND
11		N/C
12		GND
13		N/C
14		GND
15		N/C
16		GND

Table 8 JTAG and DSP header pinouts.

Schematics

Figure 18, Figure 19, Figure 20, and Figure 21 are the CLC-DRCS-PCASM schematics.

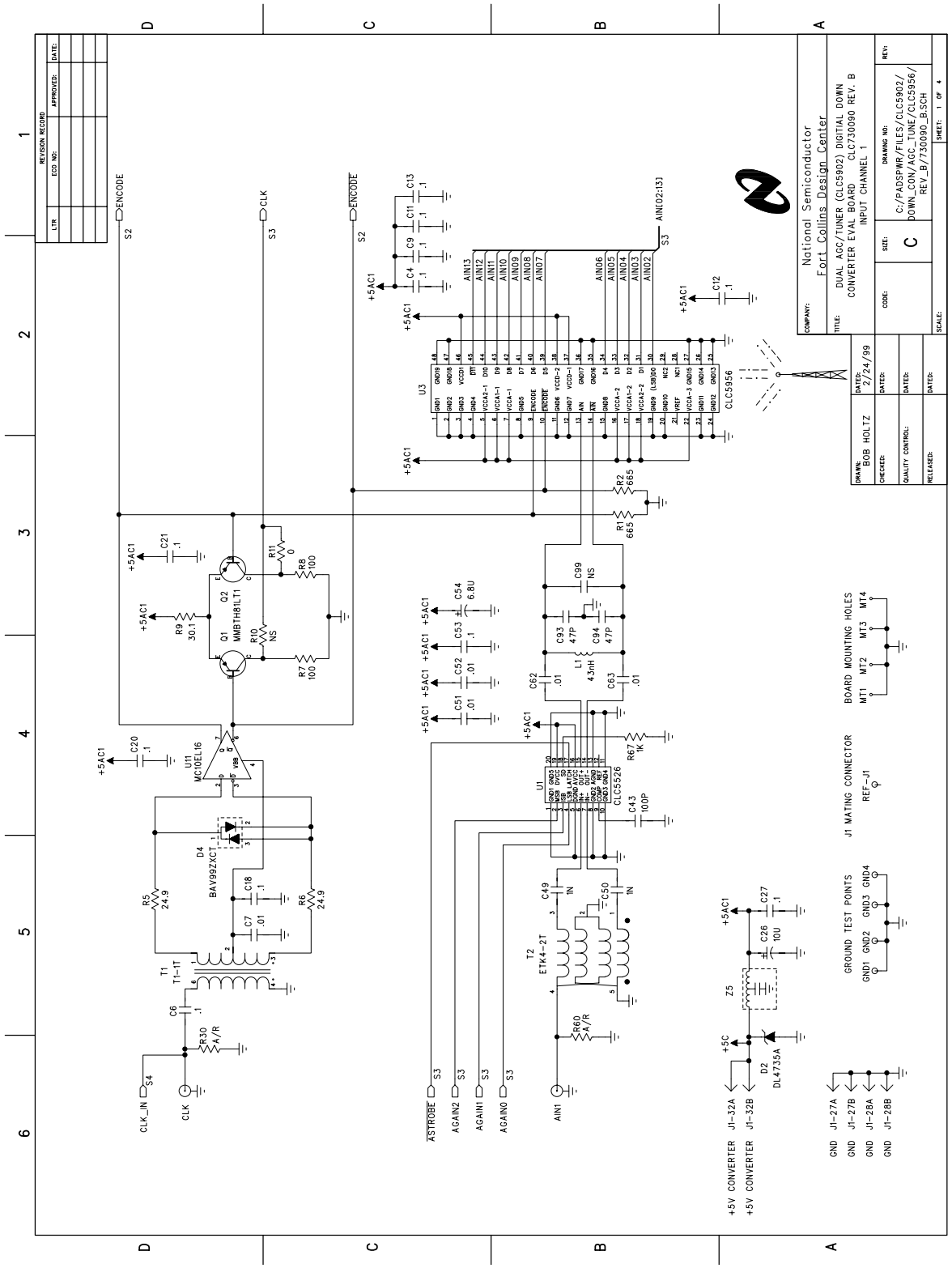

Figure 18 ADC Input AIN1

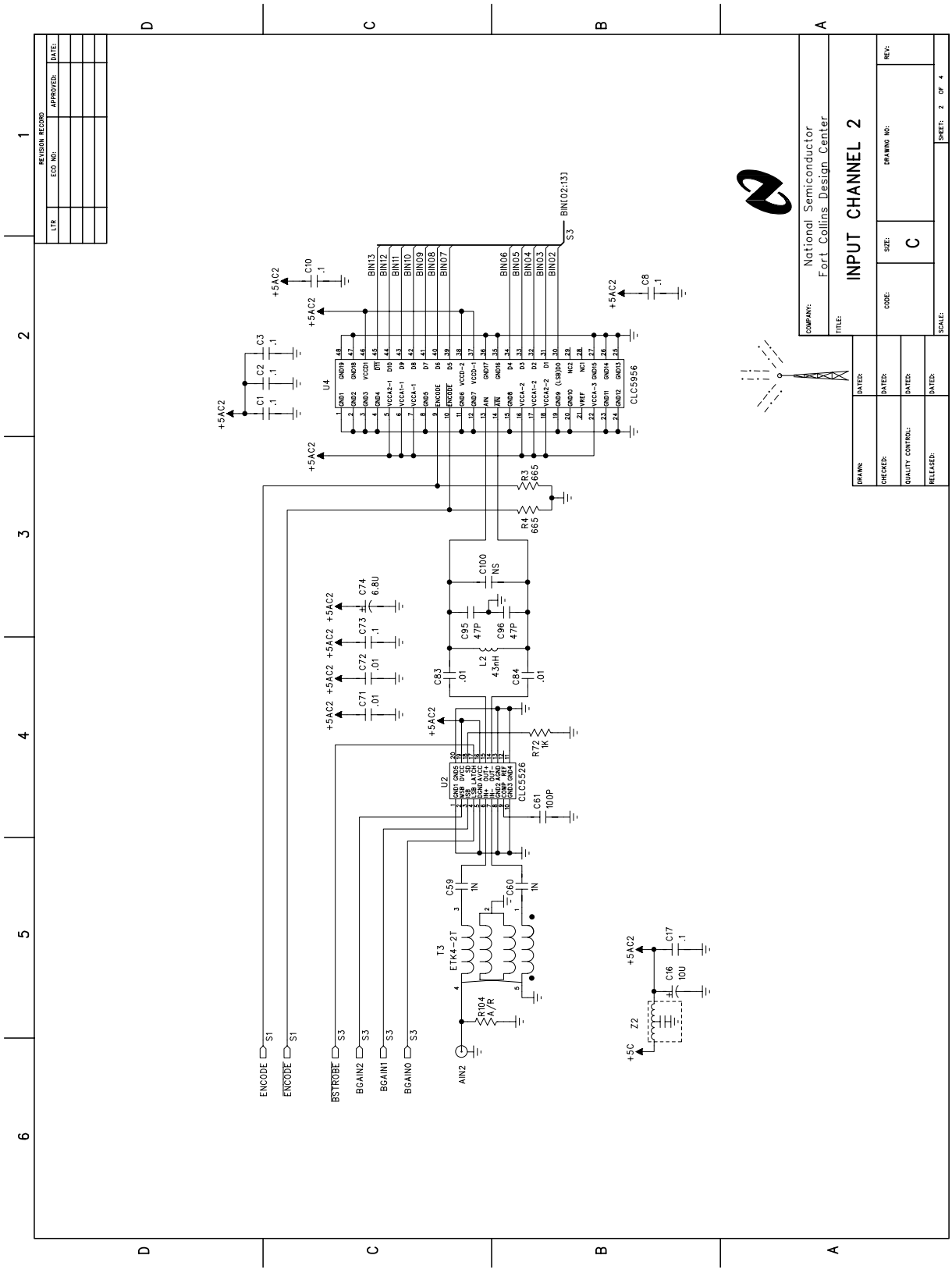

Figure 19 ADC Input AIN2

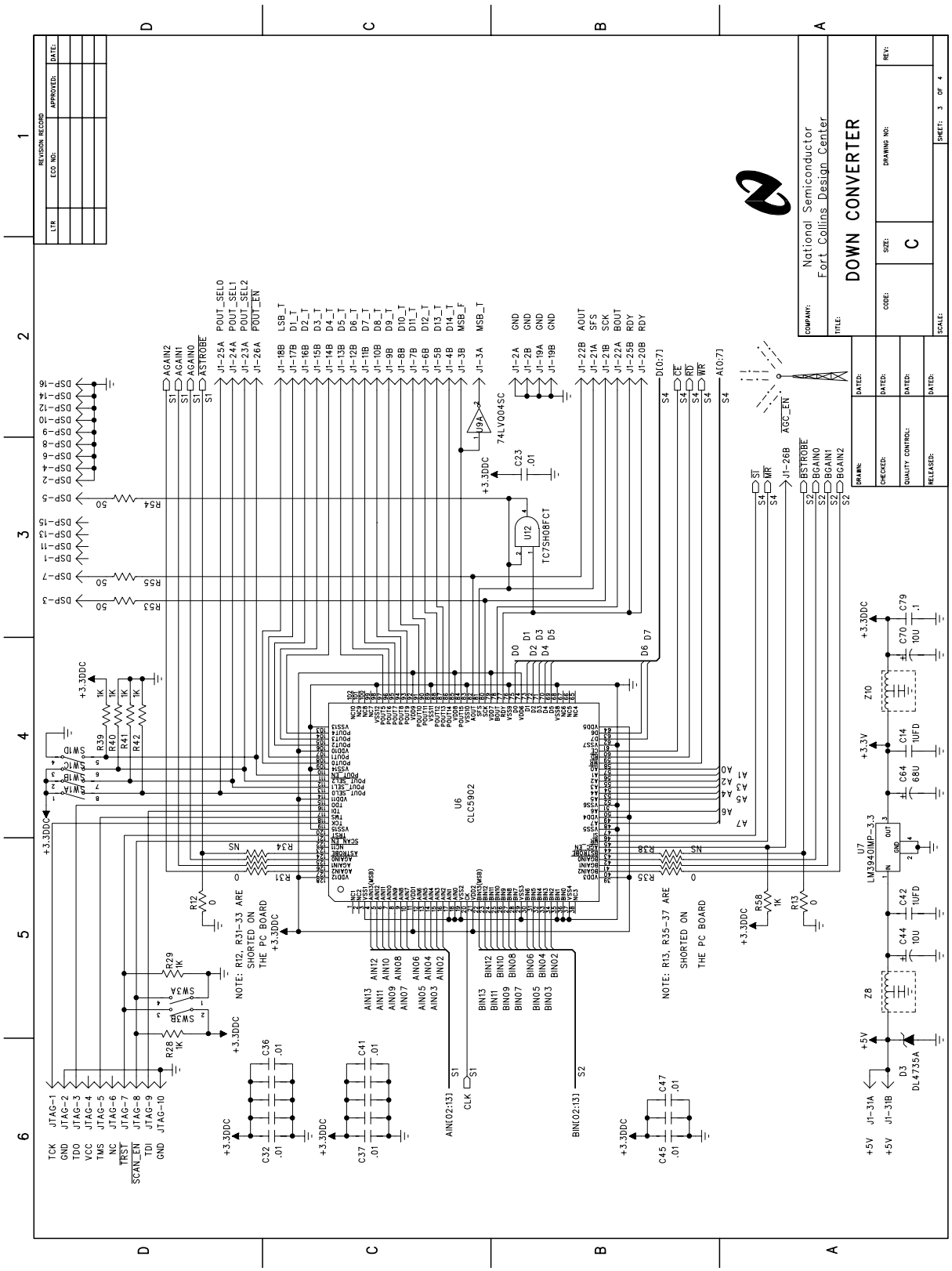

Figure 20 CLC5902 Dual Digital Tuner/AGC

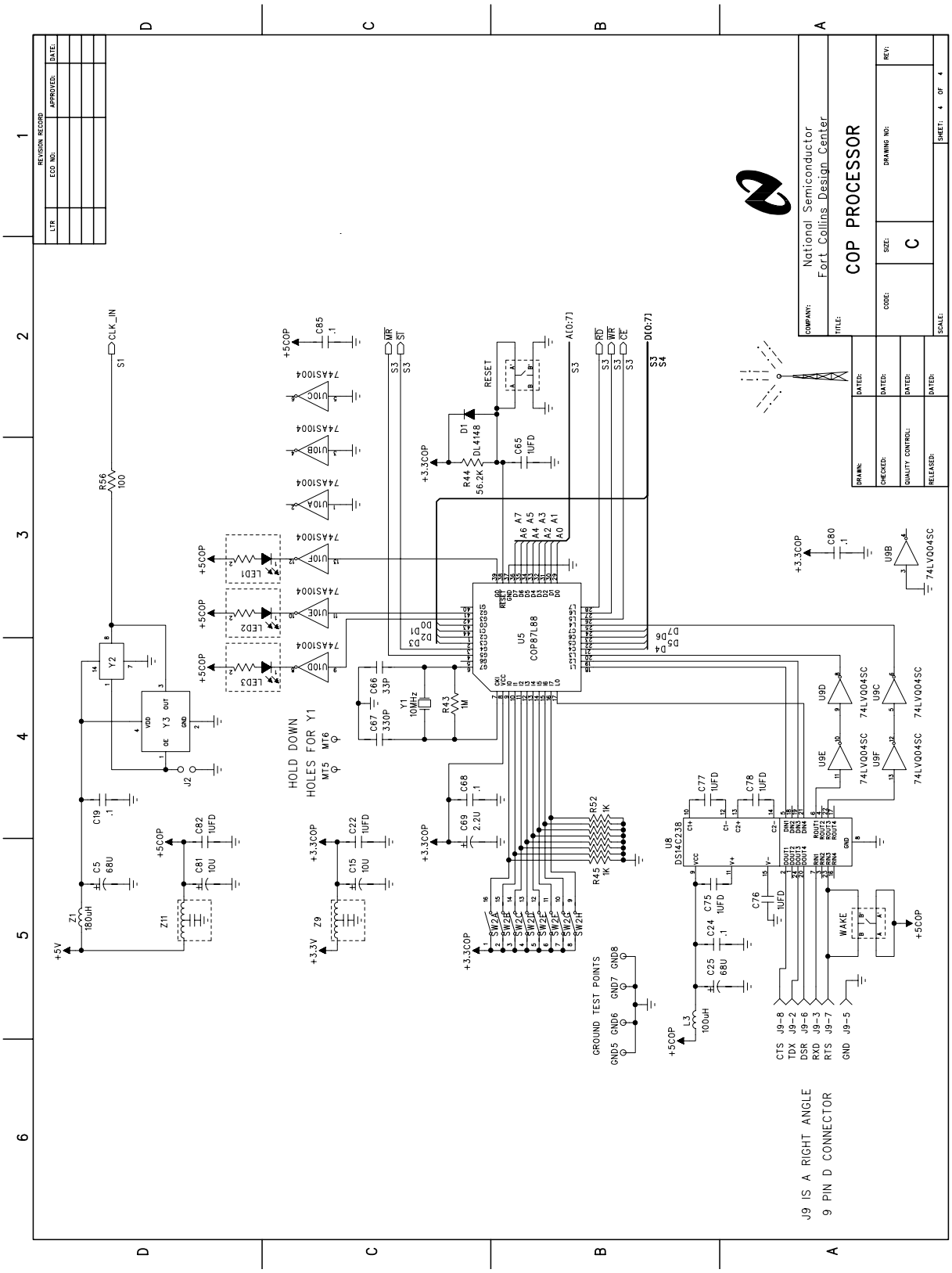

Figure 21 COP8 Microprocessor

PC Board Layout

Silk screen parts placement drawings are shown below. The complete board layout package can also be provided. Primary areas of concern are the analog inputs to the ADC and the ADC digital outputs.

Care has been exercised to prevent ground loops and noise coupling on the circuit board at the inputs.

The ADC outputs have been kept as short as possible to minimize capacitive loading. The internal ground plane has been removed under these traces to reduce the parasitic capacitance. Higher capacitance values will load the ADC output drivers causing additional noise on the internal analog signals. This will degrade the ADC performance. Analog and digital grounds have been star connected to minimize crosstalk. The supplies have series inductors for each section to provide as much isolation as is practical.

Figure 22 and Figure 23 show the DRCS parts placement. Figure 24, Figure 25, Figure 26, and Figure 27 show the PC board layers.

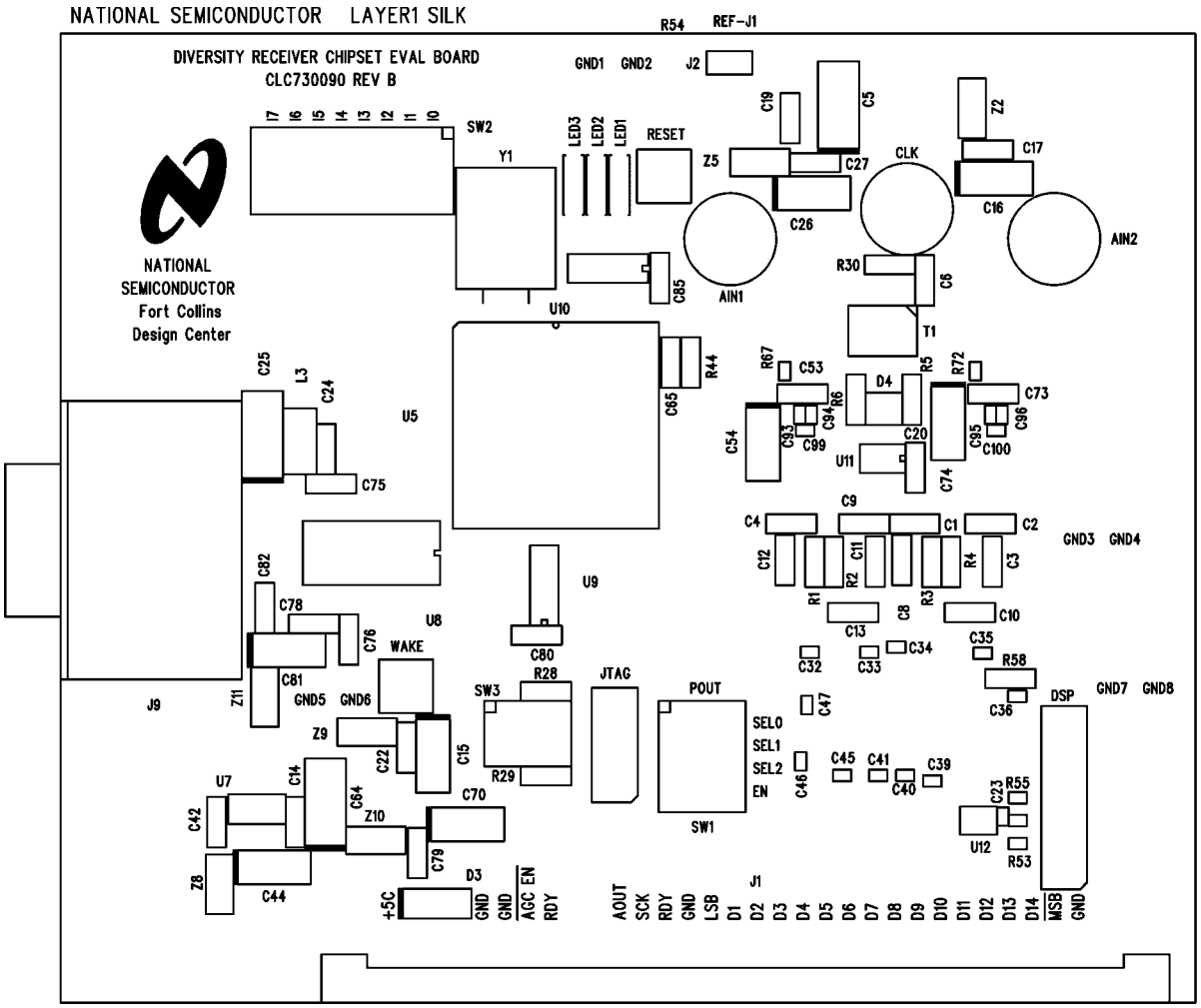

Figure 22 DRCS Board layout, top.

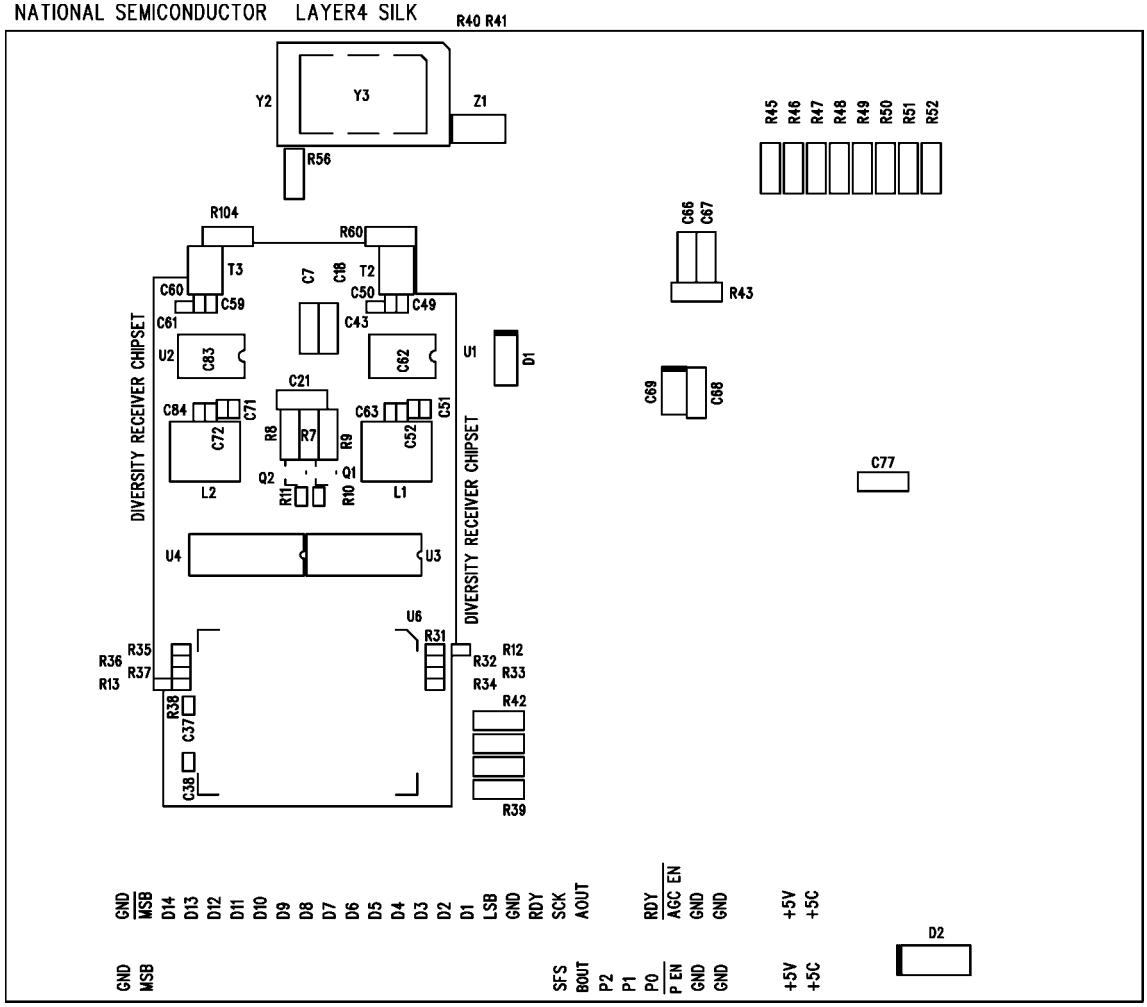

Figure 23 DRCS Board layout, bottom.

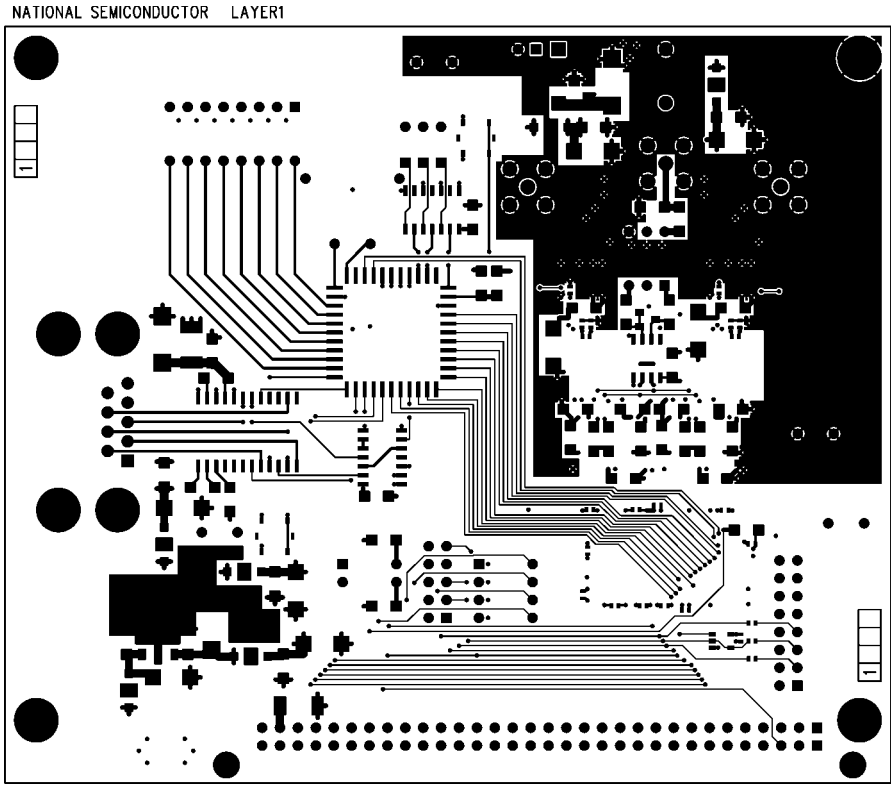

Figure 24 DRCS Board layout, L1.

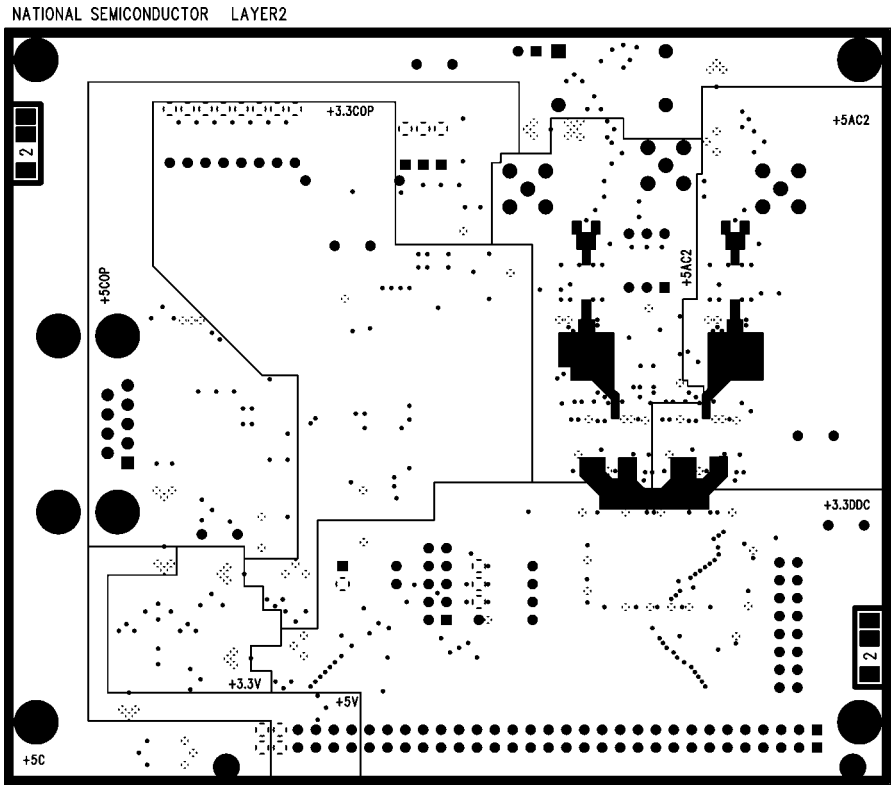

Figure 25 DRCS Board layout, L2.

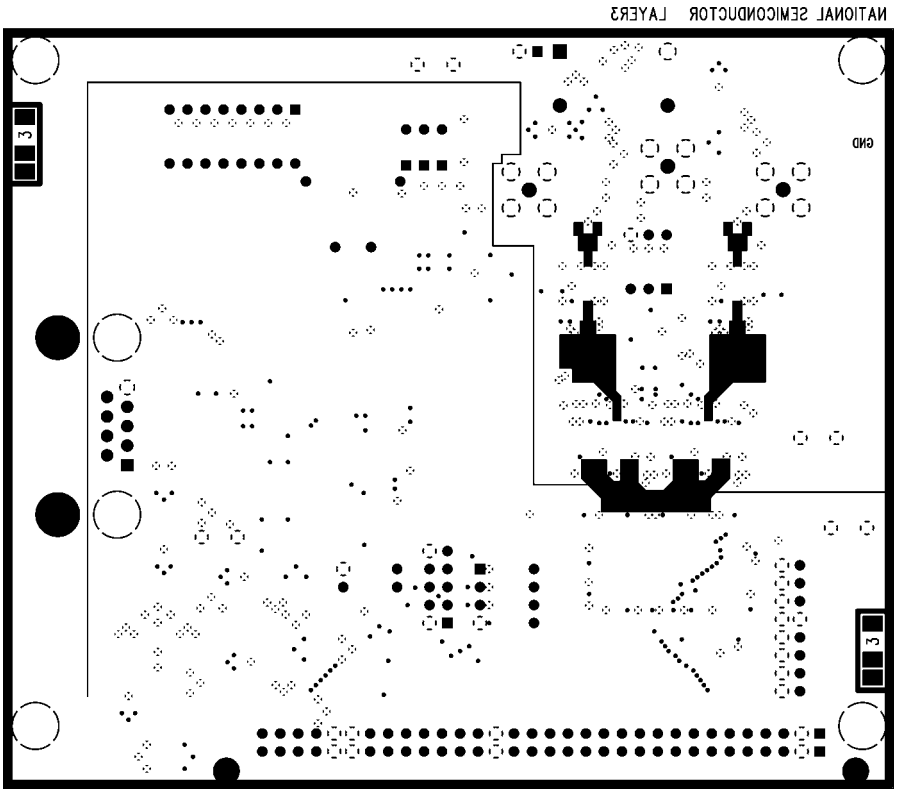

Figure 26 DRCS Board layout, L3.

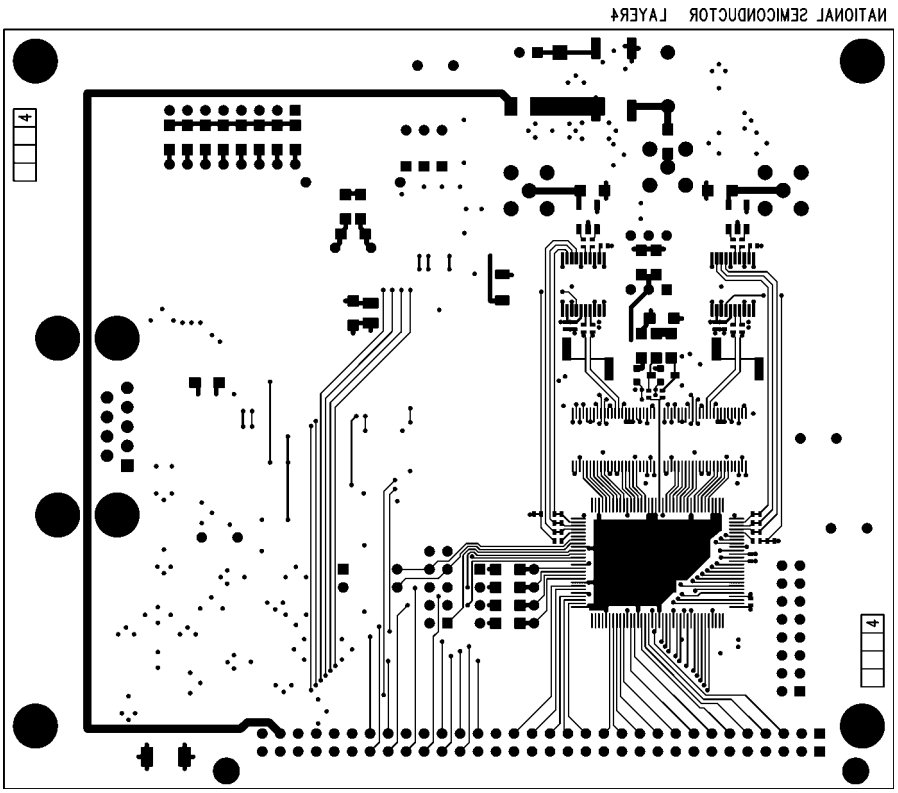

Figure 27 DRCS Board layout, L4.

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National Semiconductor Corporation

1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe

Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
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National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2309
Fax: 81-043-299-2408