National Semiconductor

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ADC14071
14-Bit, 7 MSPS, 380 mW A/D Converter

General Description

The ADC14071 is a 14-bit, monotholic analog to digital converter capable of conversion rates up to 8 Megasamples per second. This CMOS converter uses a differential, piperlined architecture with digital error correction and an on-chip track-and-hold circuit to maintain superb dynamic performance with input frequencies up to 20MHz. Tested and guaranteed dynamic performance specifications provide the designer with known performance. The ADC14071 operates on a +5V single supply consuming just 380mW (typical). The Power Down feature reduces power consumption to 20mW, typical.

The differential inputs provide a full scale input swing of $\pm V_{REF}$ with the possibility of a single input. Full use of the differential input is recommended for optimum perfomance. For ease of use, the reference input is single ended. This single-ended reference input is converted on-chip to a differential reference configuration for use by the processing circuitry. Output data format is 14-bit straight binary.

The ADC14071 may be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC14071 comes in a 48-pin TQFP and is specified to operate over the industrial temperature range of −40˚C to +85˚C.

Features

- Single +5V Operation
- Power Down Mode
- TTL/CMOS Input/Output Compatible

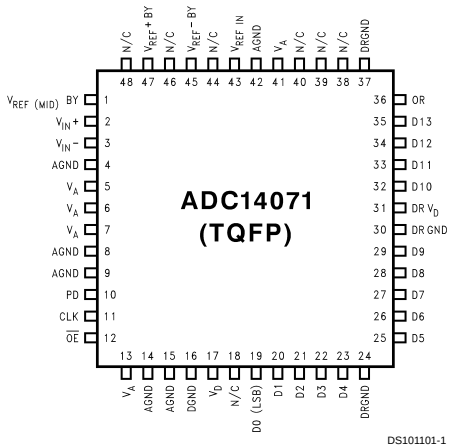
Key Specifications

■ Resolution	14 Bits
■ Max Conversion Rate	7 Msps (min)
■ DNL	±0.6 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ ENOB (f_W = 500 kHz)	12.6 Bits (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	380 mW (typ)

Applications

- Document Scanners
- Imaging
- Instrumentation
- PC-Based Data Acquisition
- Spectrum Analyzers
- Sonar/Radar
- xDSL
- Wireless Local Loop
- Data Acquisition Systems
- DSP Front End

Connection Diagram



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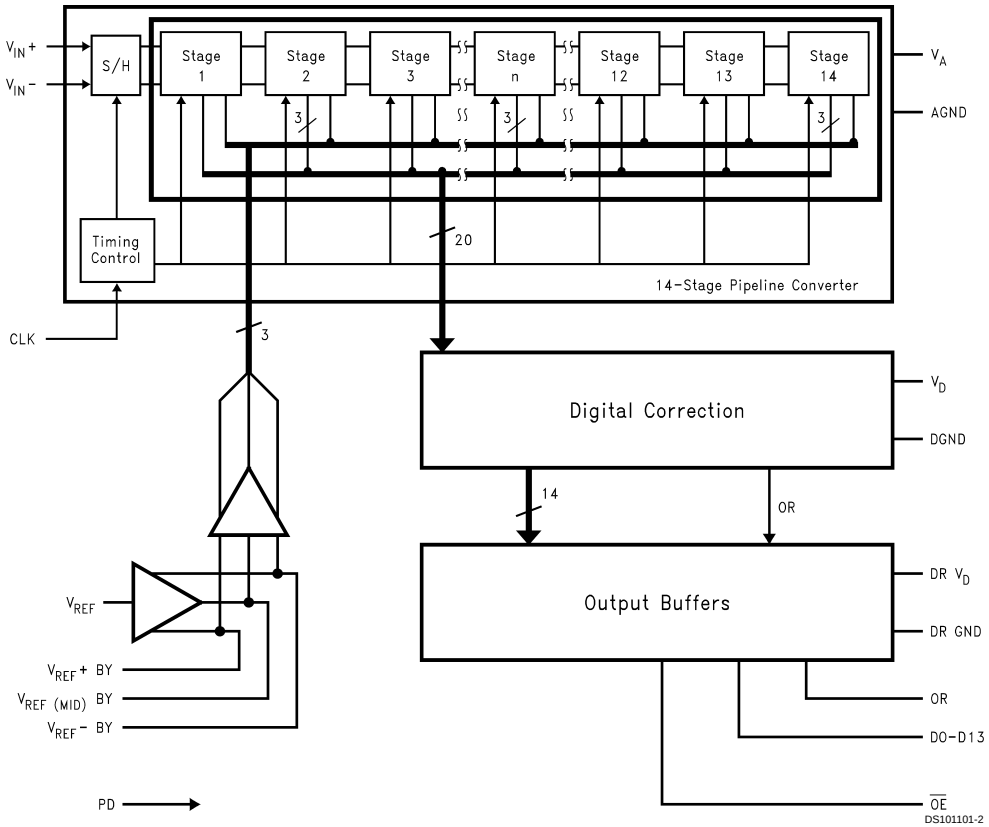
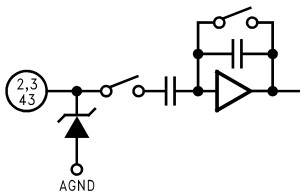
Ordering Information

Industrial Temperature Range ($-40^{\circ}C \le T_A \le +85^{\circ}C$)	NS Package
ADC14071CIVBH	VBH48A 48-Pin Thin Quad Flatpak
ADC14071EVAL	Evaluation System

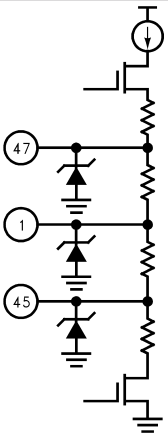
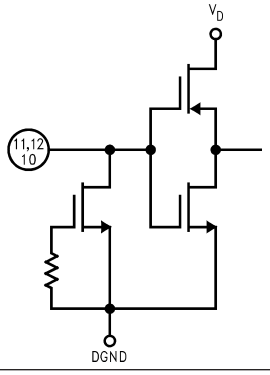
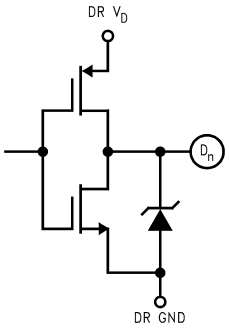
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	$V_{IN}+$		Non-Inverting analog signal input. With a 2.0V reference voltage the input signal voltage range is from 0V to 2.0V.
3	$V_{IN}-$		Inverting analog signal input. With a 2.0V reference voltage the input signal voltage range is from 0V to 2.0V. This pin may be connected to a voltage of ½ the reference voltage for single-ended operation, but a balanced input signal is required for best performance.
43	$V_{REF\ IN}$		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 2.0V nominal and should be in the range of 1.0V to 2.7V.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
47	V_{REF}+ BY		These pins are high impedance reference bypass pins only. Connect a 0.1µF capacitor from each of these pins the AGND. DO NOT connect anything else to these pins.
1	$V_{REF\ (MID)}$ BY		
45	V_{REF}− BY		
DIGITAL I/O			
11	CLOCK		Digital clock input. The range of frequencies for this input is 25 kHz to 8 MHz (typical) with guaranteed performance at 7 MHz. The input is sampled on the rising edge of this input.
12	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE® data output pins. When this pin is high, the outputs are in a high impedance state.
10	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
36	OR		Out of Range pin. A high at this output pin indicates that the input voltage is either above the reference voltage or is below ground. When this pin is high, the digital output pins will indicate a full scale for input voltages above the reference voltage, or will indicate a zero scale for input voltages below zero scale.
19-23, 25-29, 32-35	D0–D13		Digital data output pins that make up the 14-bit conversion results. D0 is the LSB, while D13 is the MSB of the straight binary output word.
ANALOG POWER			
5, 6, 7, 13, 41	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V voltage source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and by a 10 µF capacitor.
4, 8, 9, 14, 15, 42	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC14071 package. See Section 5 (Layout and Grounding) for more details.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
DIGITAL POWER			
17	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
16	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC14071 package. See Section 5 (Layout and Grounding) for more details.
31	DR V_D		Positive digital supply pin for the ADC14071's output drivers. This pin should be connected to a voltage source of +3 to +5V and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor and never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
24, 30, 37	DR GND		The ground return for the digital supply for the ADC14071's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC14071's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.
NC			
18, 38, 39, 40, 44, 46, 48	NC		All pins marked NC (no connect) should not be connected to any potential (or to ground). Allow these pins to float.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ = V_A = V_D = DR\ V_D$)	6.0V
$V_A - DR\ V_D$, $V_D - DR\ V_D$	≥0V
Voltage on Any I/O Pin	−0.5V to V^+ +0.5V
Input Current at Pins 1, 45 and 47(Note 3)	±10 mA
Input Current at Any Other Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	1500V
Machine Model	200V
Soldering Temperature, Infrared, 10 seconds (Note 6)	300˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$-40˚C \le T_A \le +85˚C$
V_A, V_D	+4.75V to +5.25V
DR V_D	2.7V to V_D
V_{REF}	1.0V to 2.7V
Digital Inputs	−0.3V to V_D + 0.3V
Analog Inputs	−0.3V to V_A + 0.3V
$\lvert V_A - V_D \rvert$	≤100 mV
|AGND − DGND|	0V to 100 mV

Converter Electrical Characteristics

The following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$ = +5.0V_{DC}, DR V_D = 3.0V or 5.0V, PD = 0V, $V_{REF\ IN}$ = +2.0V, V_{IN} (common mode) = 1.0V, f_{CLK} = 7 MHz @ 50% duty cycle, t_r, t_f = 4ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_A = T_J$ = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 11)	Units
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**14**	Bits (min)
INL	Integral Non-Linearity (note 12)			±2.2		LSB
DNL	Differential Non-Linearity			±0.6	**+1.0 −0.85**	LSB (max)
FSE	Positive and Negative Full-Scale Error	25˚C		0.9	2.3	%FS
TC FSE	Full-Scale Error Tempco			−5		ppm/˚C
ZSE	Zero Offset Error	25˚C		0.1		%FS
TC ZSE	Zero Offset Error Tempco			−0.6		ppm/˚C
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{REF}	Reference Voltage Range			2.00	**1.0** **2.7**	V(min) V(max)
R_R	Reference Input Resistance			10M		Ohms
C_R	Reference Input Capacitance			5		pF
V_{IN}	Input Voltage Range ($V_{IN^+} - V_{IN^-}$)	V_{IN} (common Mode) = V_{REF}/2		±2.0	**±1.0** **±2.7**	V(min) V(max)
C_{IN}	V_{IN^+}, V_{IN^-} Input Capacitance	V_{IN} = 1.0V+0.7 Vrms	(CLK LOW)	14		pF
			(CLK HIGH)	5		pF
DYNAMIC CONVERTER CHARACTERISTICS						
BW	Full Power Bandwidth	−1 dB		20		MHz
		−3 dB		25		MHz
ENOB	Effective Number of Bits	f_{IN} = 500 kHz		12.6	12.0	Bits (min)
		f_{IN} = 3.5 MHz		12.0		Bits
SINAD	Signal-to-Noise and Distortion	f_{IN} = 500 kHz		77	74	dB (min)
		f_{IN} = 3.5 MHz		74		dB
SNR	Signal -to-Noise Ratio (Note 13)	f_{IN} = 500 kHz		80	78	dB (min)
		f_{IN} = 3.5 MHz		77		dB
THD	Total Harmonic Distortion	f_{IN} = 500 kHz		−83	−76	dB (min)
		f_{IN} = 3.5 MHz		−79		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +5.0V_{DC}$, DR V_D = 3.0V or 5.0V, PD = 0V, $V_{REF\ IN}$ = +2.0V, V_{IN} (common mode) = 1.0V, f_{CLK} = 7 MHz @ 50% duty cycle, t_r, t_f = 4ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_A = T_J = 25^\circ C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
DYNAMIC CONVERTER CHARACTERISTICS					
SFDR	Spurious Free Dynamic Range	f_{IN} = 500 kHz	90		dB
		f_{IN} = 3.5 MHz	81		dB
IMD	Intermodulation Distortion	f_{IN1} = 95 kHz f_{IN2} = 105 kHz	−97		dB

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +5.0V_{DC}$, DR V_D = 3.0V or 5.0V, PD = 0V, $V_{REF\ IN}$ = +2.0V, V_{IN} (common mode) = 1.0V, f_{CLK} = 7 MHz @ 50% duty cycle, t_r, t_f = 4ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_A = T_J = 25^\circ C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
CLOCK $\overline{OE}$, $\overline{PD}$ DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical “1” Input Voltage	V^+ = 5.25V		**2.0**	V(min)
V_{IL}	Logical “0” Input Voltage	V^+ = 5.25V		**0.8**	V(max)
I_{IH}	Logical “1” Input Current	V_{IN} = 5.0V	1		µA
I_{IL}	Logical “0” Input Current	V_{IN} = 0V	−1		µA
C_{IN}	V_{IN} Input Capacitance		5		pF
D00 – D13 DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Logical “1” Output Voltage	DR V_D = 4.75V, I_{OUT} = −360 µA		**4.5**	V(min)
		DR V_D = 2.7V, I_{OUT} = −360 µA		**2.5**	V(min)
V_{OL}	Logical “0” Output Voltage	DR V_D = 4.75V, I_{OUT} = 1.6 mA		**0.4**	V(max)
		DR V_D = 2.7V, I_{OUT} = 1.6 mA		**0.4**	V(max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 3V or 5V	100		nA
		V_{OUT} = 0V	−100		nA
$+I_{SC}$	Output Short Circuit Source Current	DR V_D = 3V, V_{OUT} = 0V	−10		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = DR V_D = 3V	12		mA
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = DGND	75.7	**81**	mA(max)
$I_D + I_{DR}$	Digital Supply Current	PD = DGND, no output load, dc input	0.3	**2**	mA(max)
	Total Power Consumption	PD = DGND, no output load, dc input	380	**425**	mW(max)
		PD = DR V_D, no output load, dc input	20		mW
PSRR	Power Supply Rejection Ratio	Change in FS Error with 0.5V change in V_A	70		dB
		250 mV_{PP} 100 kHz riding on V_A	46		dB

AC Electrical Characteristics

The following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +5.0V_{DC}$, DR V_D = 3.0V or 5.0V, PD = 0V, $V_{REF\ IN}$ = +2.0V, V_{IN} (common mode) = 1.0V, f_{CLK} = 7 MHz @ 50% duty cycle, t_r, t_f = 4 ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_A = T_J = 25^\circ C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
f_{CLK}	Conversion Clock Frequency		25 8	 **7**	kHz(min) MHz(max)
	Conversion Clock Duty Cycle		45 55		%(min) %(max)

AC Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +5.0V_{DC}$, DR V_D = 3.0V or 5.0V, PD = 0V, $V_{REF\ IN}$ = +2.0V, V_{IN} (common mode) = 1.0V, f_{CLK} = 7 MHz @ 50% duty cycle, t_r, t_f = 4 ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_A = T_J = 25^\circ C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
t_{CL}	Conversion Clock Low Time		**63**		ns(min)
t_{CH}	Conversion Clock High Time		**63**		ns(min)
t_{CONV}	Conversion Latency		12		Clock Cycles
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		5		ps(rms)
t_{OD}	Rising Edge of CLOCK to Data Valid	DRV_D = 3.0V	45	**58**	ns(max)
		DRV_D = 5.0V	34	**53**	ns(max)
t_{EN}	$\overline{OE}$ Low to Data Valid on D00 – D13		35		ns
t_{DIS}	$\overline{OE}$ High to D0 – D13 into TRI-STATE®		12		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = DR GND = 0V, unless otherwise specified.

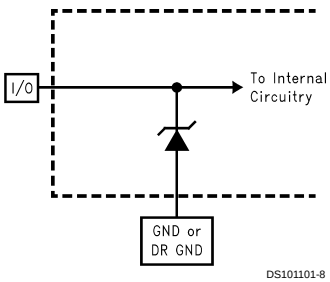
Note 3: When the input voltage at any pin exceeds the power supplies (that is, $V_{IN} < AGND$ or $V_{IN} > V_A$ or V_D), the current at that pin should be limited to 25 mA (10 mA for pins 1, 45 and 47). The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_DMAX = (T_Jmax - T_A)/\theta_{JA}$. In the 48-pin TQFP, θ_{ja} is 76°C/W, so P_DMAX = 1,345 mW at 25°C and 855 mW at the maximum operating ambient temperature of 85°C. Note that the power dissipation of this device under normal operation will typically be about 400 mW (380 mW quiescent power +20 mW due to 1 TTL load on each digital output. The values for maximum power dissipation listed above will be reached only when the ADC14071 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms.

Note 6: See AN450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The inputs are protected as shown below. Input voltage magnitudes up to 0.3V above V_A or to 0.3V below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above (V_A −2.0V) or below GND by more than 300 mV. As an example, if V_A is $4.75V_{DC}$, the full-scale input voltage must be ≤ $2.75V_{DC}$ or ≥ −300 mV to ensure accurate conversions.



ESD Protection Scheme for Input and Output Pins

Note 8: To guarantee accuracy, it is required that V_A and V_D be connected together and to the same power supply with separate bypass capacitors at each V^+ pin.

Note 9: With the test condition for V_{REF} = ($V_{REF}+ - V_{REF}-$) given as +2.0V, the 14-bit LSB is 244 µV.

Note 10: Typical figures are at $T_A = T_J = 25^\circ C$, and represent most likely parametric norms.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Integral Non-Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and negative full-scale.

Note 13: Optimum SNR performance will be obtained by keeping the reference input in the 1.8V to 2.7V range. The LM4041CIM3-ADJ (SOT-23 package) or the LM4041CIZ-ADJ (TO-92 package bandgap voltage reference is recommended for this application.

AC Electrical Characteristics (Continued)

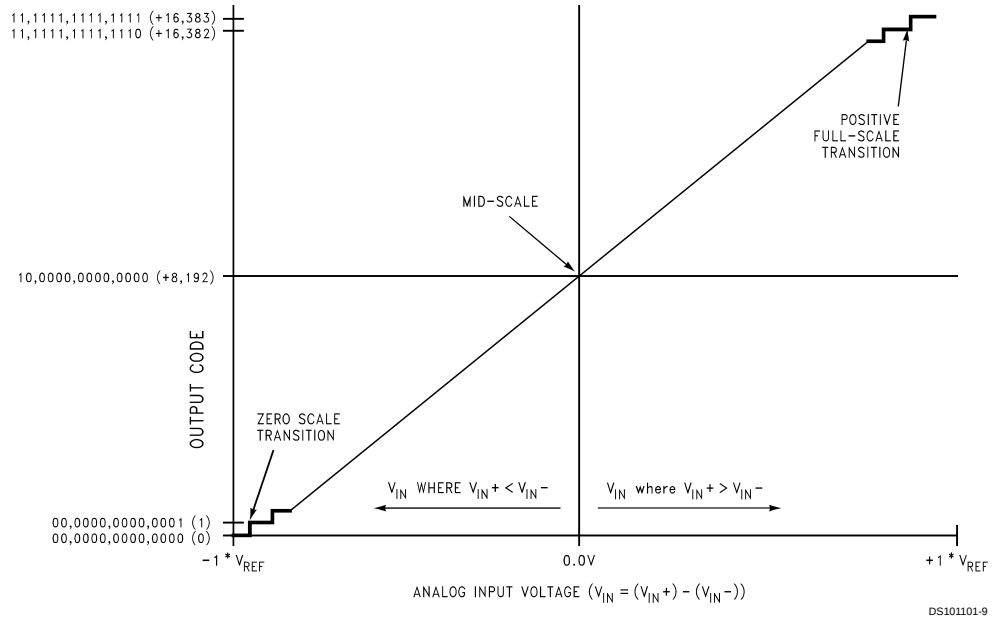


FIGURE 1. Transfer Characteristic

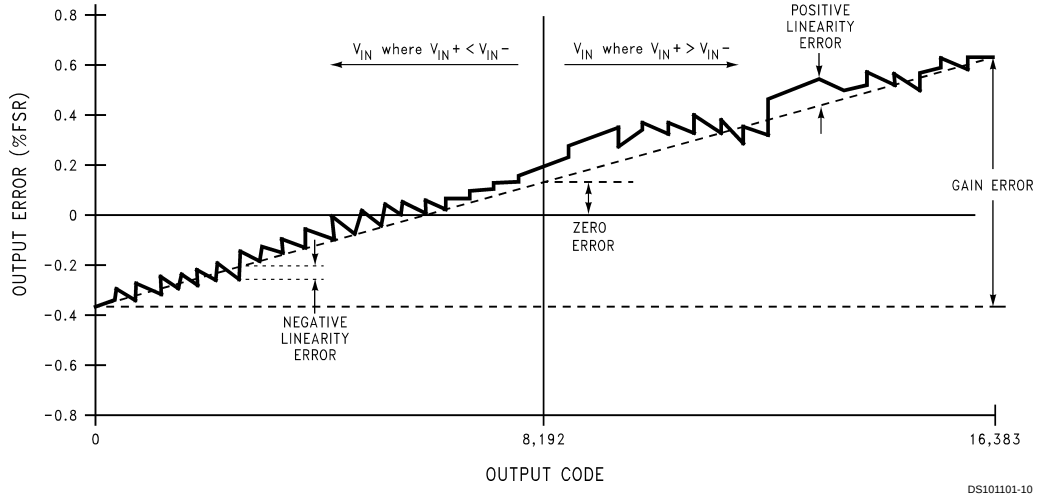
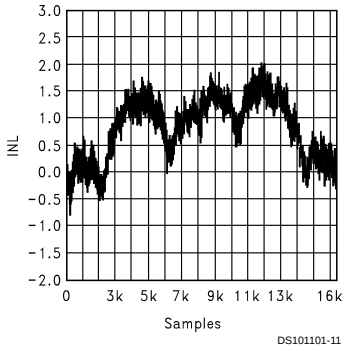


FIGURE 2. Description of Errors

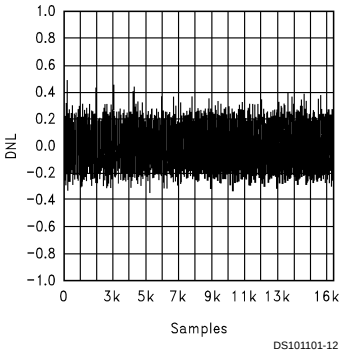
Typical Performance Characteristics

$V_A = V_D = DR\ V_D = 5V$. $f_{CLK} = 7MHz$, $f_{IN} = 500KHz$ unless otherwise stated.

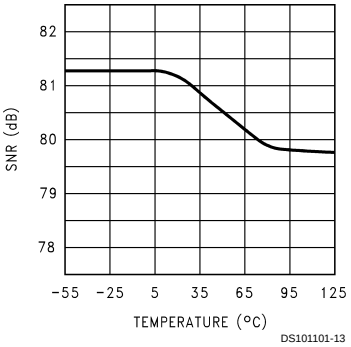
INL



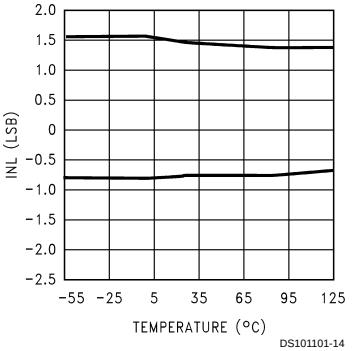
DNL



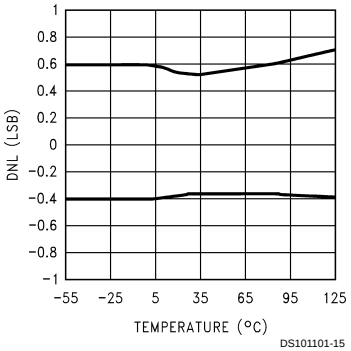
SNR vs Temperature



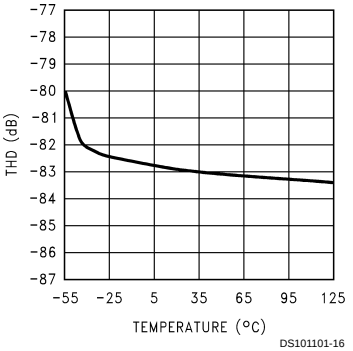
INL vs Temperature



DNL vs Temperature



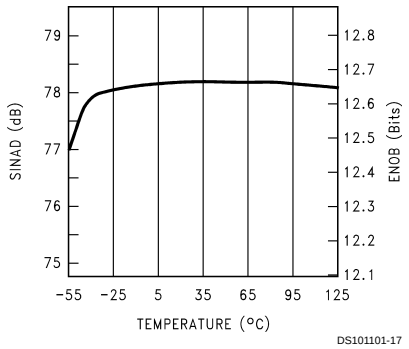
THD vs Temperature



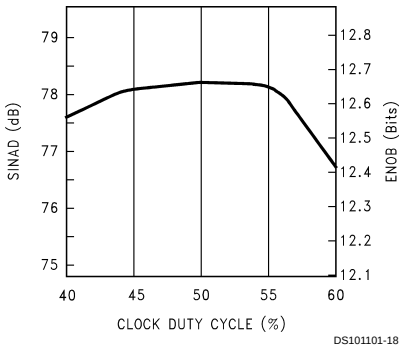
Typical Performance Characteristics

$V_A = V_D = DR\ V_D = 5V$. $f_{CLK} = 7MHz$, $f_{IN} = 500KHz$ unless otherwise stated. (Continued)

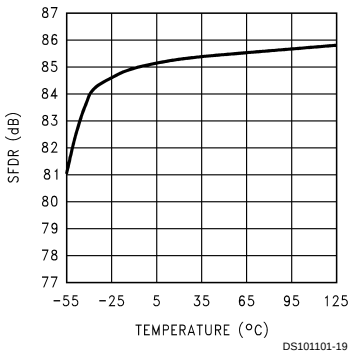
SINAD & ENOB vs Temp



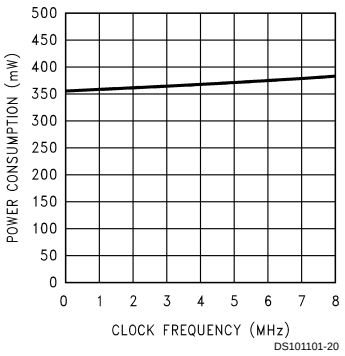
SINAD & ENOB vs Clock Duty Cycle



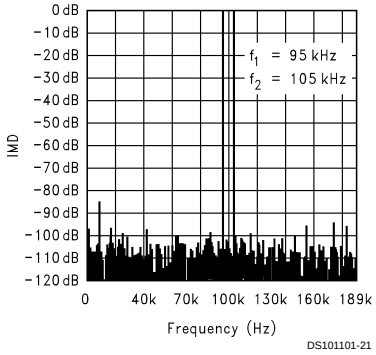
SFDR vs Temperature



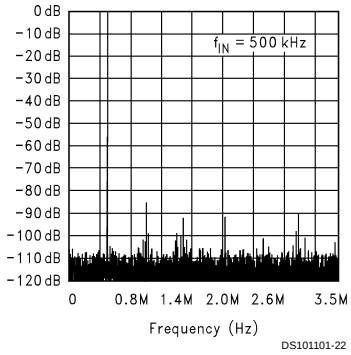
Power Consumption vs f_{CLK}



IMD Response



Spectral Response



Specification Definitions

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

APERTURE DELAY is the time from the sampling edge of the clock to when the input signal is acquired or held for conversion. In other words, it is the time required for the Sample/Hold circuit to go from the ″sample″ mode to the ″hold″ mode. The Sample/Hold circuit effectively stops capturing the input signal and goes into the ″hold″ mode this amount of time after the clock transition.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and

Specification Definitions (Continued)

Distortion or SINAD. ENOB is defined as (SINAD - 1.76)/6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dB.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

NEGATIVE FULL SCALE ERROR is the measure of how far the last code transition is from the ideal of ½LSB above nominal negative full scale. It is the difference between the input voltage ($V_{IN}^+ - V_{IN}^-$) just causing a transition to the first code and the ideal voltage to cause that transition. The ideal LSB transition (when it should occur) is (V_{IN}^+) − (V_{IN}^-) = ½LSB

OFFSET ERROR is the difference between the ideal and actual voltages that cause a transition to mid-scale (a code of 8192) when approached from a lower code. The ideal LSB transition (when it should occur) is (V_{IN}^+) − (V_{IN}^-) = 0

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and the availability of that same conversion result at the output. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is a measure of how far the last code transition is from the ideal of 1½LSB below nominal positive full scale. It is the difference beween the input voltage ($V_{IN}^+ - V_{IN}^-$) just causing a transition to positive full scale and V_{REF} − 1½LSB. Full Scalse Error is sometimes called Full Scale Offset Error.

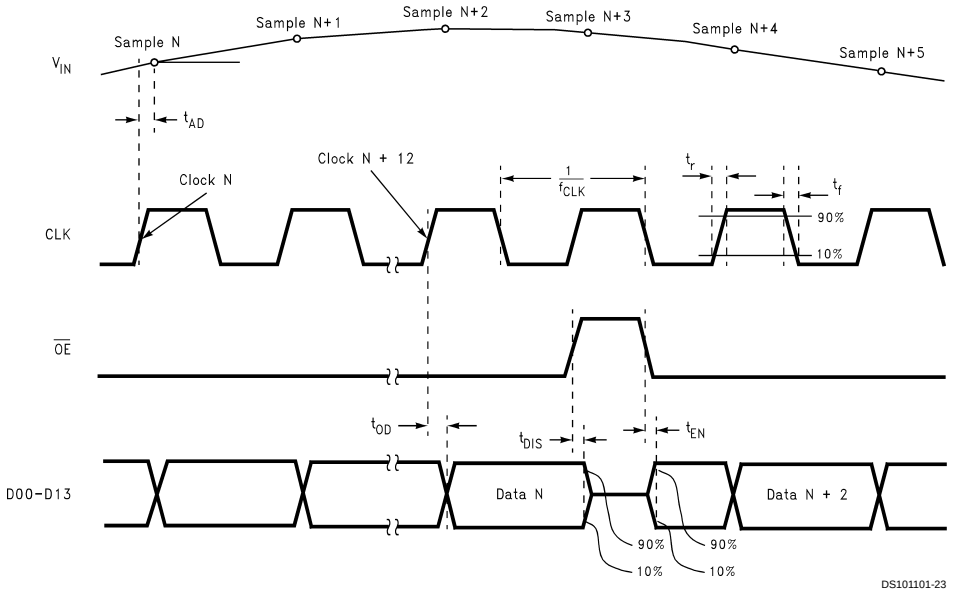
SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first nine harmonic components to the rms value of the input signal.

Timing Diagram



Output Timing

Functional Description

Operating on a single +5V supply, the ADC14071 uses a pipelined architecture and has error correction circuitry to help ensure maximum performance.

Balanced analog signals are digitized to 14 bits. Each of these input signals should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and can be centered around $V_{REF}/2$. *Table 1* and *Table 2* indicate the input to output relationship of the ADC14071. As indicated in *Table 2*, biasing one input to $V_{REF}/2$ and driving the other input with its full range signal results in a 6 dB reduction of the output range, limiting it to the range of ¼ to ¾ of the minimum output range obtainable if both inputs were driven with complimentary signals.

Section *1.3 SIGNAL INPUTS* explains how to avoid this signal reduction.

TABLE 1. Input to Output Relationship — Differential Input

V_{IN}^+	V_{IN}^-	Output
0	V_{REF}	00 0000 0000 0000
0.25*V_{REF}	0.75*V_{REF}	01 0000 0000 0000
0.50*V_{REF}	0.50*V_{REF}	10 0000 0000 0000
0.75*V_{REF}	025*V_{REF}	11 0000 0000 0000
V_{REF}	0	11 1111 1111 1111

TABLE 2. Input to Output Relationship — Single-Ended Input

V_{IN}^+	V_{IN}^-	Output
0	$V_{REF}/2$	01 0000 0000 0000
0.25*V_{REF}	$V_{REF}/2$	01 1000 0000 0000
0.50*V_{REF}	$V_{REF}/2$	10 0000 0000 0000
0.75*V_{REF}	$V_{REF}/2$	10 1000 0000 0000
V_{REF}	$V_{REF}/2$	11 0000 0000 0000

The output word rate is the same as the clock frequency, which can be between 25kSPS and 8 MSPS (typical). The analog input voltage is acquired at the rising edge of the clock and the digital data for that sample is delayed by the pipeline for 12 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 20 mW.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC14071:

$4.75V \le V_A \le 5.25V$

$V_D = V_A$

$2.7 \le DR\ V_D \le V_D$

$25\ kHz \le f_{CLK} \le 8\ MHz$

$1.0V \le V_{REF} \le 2.7V$

1.1 ANALOG INPUTS

The ADC14071 has two analog signal inputs, V_{IN}^+ and V_{IN}^-. These two pins form a differential input. There is one reference input pin, V_{REF}.

1.2 REFERENCE INPUT

The ADC14071 is designed to operate with a 2.0V reference, but performs well with reference voltages in the range of 1.0V to 2.7V. Reducing the reference voltage below 1.0V will decrease the signal-to-noise ratio (SNR) of the ADC14071. Increasing the reference voltage (and the input signal swing) beyond 2.7V will degrade THD.

It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path.

The reference bypass pins (V_{REF}^+ BY, V_{REF}^- BY and V_{REF} and $V_{REF\ (MID)}$ BY) are for bypass purposes only. Bypass each of these pins to AGND with 0.1µF capacitors. DO NOT LOAD these pins.

1.3 SIGNAL INPUTS

The signal inputs are V_{IN}^+ and V_{IN}^-. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}^+) - (V_{IN}^-).$$

Figure 3 shows the expected input signal range.

Note that the nominal input common mode voltage is 1.0V. This assumes that the input signals run between the limits of AGND and 2V with V_{REF} = 2.0V. As the input signal V_{IN} increases above 4 V_{P-P}, the input common mode range should become $V_{REF}/2$. The Peaks of the input signals should never exceed the voltage described as

$$\text{Peak Input Voltage} = V_A - 2.0V$$

to maintain signal integrity and THD and SINAD performance.

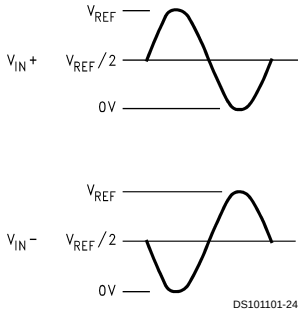


FIGURE 3. Expected Input Signal Range

The ADC14071 performs best with a differential input centered around half the reference voltage, V_{REF}. The peak-to-peak voltage swing at both V_{IN}^+ and V_{IN}^- should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180˚ out of phase from each other and of the same amplitute to avoid a reduction in the output amplitude. For angular deviations of up to 10˚ from these two signals being 180 out of phase, the full scale error in LSB can be described as

$$E_{FS} = dev^{1.79}.$$

Where dev is the angular difference between the two signals having a 180˚ relative phase relationship to each other, as shown in *Figure 4*. Drive the analog inputs with a source impedance less than 100Ω.

Applications Information (Continued)

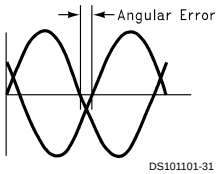


FIGURE 4. Angular Errors between the Two Input Signals Will Reduce the Output Level

For single ended operation, one of the analog inputs should be connected to a voltage equal to the reference voltage, with the common mode voltage of the driven input equal to that same voltage. The peak-to-peak input signal should be twice the reference voltage to minimize SNR and SINAD loss. For example, set the V_{REF} to 1.0V, bias V_{IN^-} to 1.0V and drive V_{IN^+} with signal range of 0V to 2.0V.

The V_{IN^+} and the V_{IN^-} inputs of the ADC14071 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 14 pF when the clock is low, and 5 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than is a fixed capacitance, choose the driving amplifier carefully. The LM6172 is a good amplifier for driving the ADC14071.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 33Ω series resistors at each of the signal inputs with a 0.0022 µF capacitor across the inputs, as can be seen in *Figures 6, 7*. These components should be placed close to the ADC as the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input.

2.0 DIGITAL INPUTS

Digital inputs consist of CLOCK, $\overline{OE}$ and PD.

2.1 CLOCK

The **CLOCK** signal controls the timing of the sampling process. Drive the clock input with a stable, low phase jitter clock signal in the range of 25 kHz to 8 MHz and rise and fall times of less than 4 ns. The trace carrying the clock signal should be as short as possible. This trace should not cross any other signal line, analog or digital, not even at 90˚.

The **CLOCK** signal also drives the internal state machine. If the clock is interrupted, the charge on internal capacitors can dissipate to the point where the output data will lose accuracy.

The **CLOCK** pin should be terminated with a series 100Ω resistor and 200 pF capacitor to ground located within two centimeters of the ADC14071 clock pin, as shown in *Figure 5*.

Whenever the trace between the clock source and the ADC clock pin is greater than 2 cm, use a 50Ω series resistor in the clock line, located within 2 cm of the driving source.

2.2 $\overline{OE}$

The **$\overline{OE}$** pin, when low, puts the output pins into a high impedance state. Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through DR V_D and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem.

Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC14071, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω.

2.3 PD

The **PD** pin, when high, holds the ADC14071 in a power-down mode to conserve power when the converter is not being used. In this state the power consumption is 20 mW. The output data pins may change randomly when the PD pin is high. Power consumption during power-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in the power down mode.

3.0 OUTPUTS

The ADC14071 has 15 digital outputs: 14 Data Output pins and OR (Out of Range).

The output pins are TTL/CMOS compatible and the output data format is straight binary. Valid data is present at these outputs while the $\overline{OE}$ pin is low. While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the *falling edge* of the conversion clock (pin 11).

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry. Only one input should be connected to each output pin. Additionally, inserting series resistors of 47Ω to 56Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuitry capacitances and limit the output currents which could otherwise result in performance degradation, as discussed in Section 2.2. See *Figure 5*.

The OR pin indicates when the input signal is under- or over-range. This pin and the MSB, used together, will indicate whether the input is out of range low or high.

Applications Information (Continued)

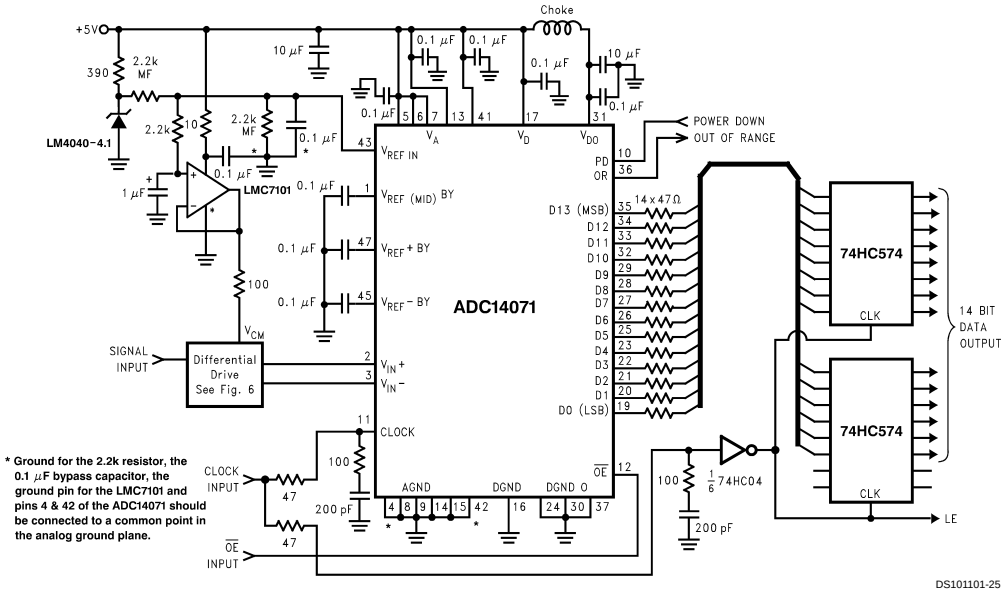


FIGURE 5. Simple Application Circuit with Single-Ended to Differential Buffer

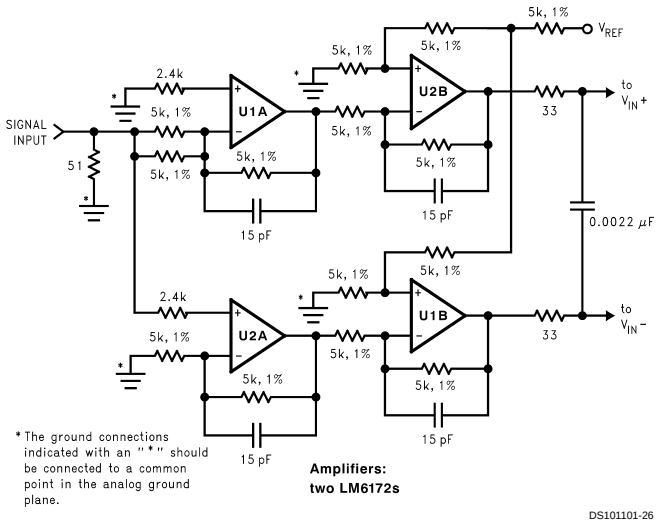


FIGURE 6. Differential Drive Circuit of *Figure 5*. All 100Ω Resistors are 0.1%. Tolerance of the other Resistors is not Critical.

Applications Information (Continued)

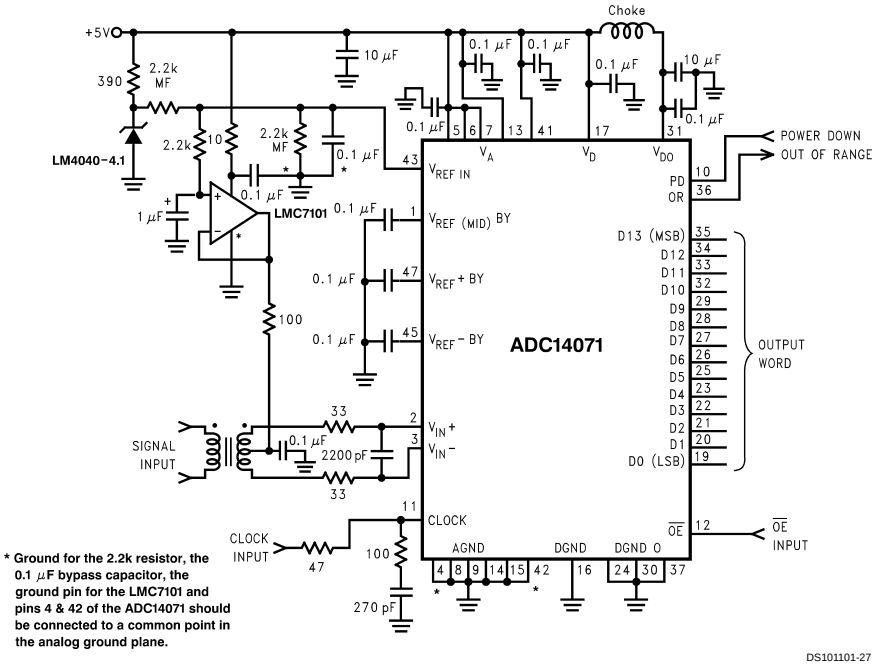


FIGURE 7. Driving the Signal Inputs with a Transformer

4.0 POWER SUPPLY CONSIDERATIONS

The power supply pin should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor a centimeter of each power pin. Leadless chip capacitors are preferred because they provide low lead inductance.

As is the case with all high-speed converters, the ADC14071 is sensitive to power supply noise. Accordingly the noise on the analog supply pin should be kept below 10 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power up.

The DR V_D pin provides power for the output drivers and may be operated from a supply in the range of 2.7V to the V_D supply (nominal 5V). This can simplify interfacing to 3.0V devices and systems. Powering the DR V_D from 3V will also reduce power consumption and noise generation due to output switching. **DO NOT operate the DR V_D pin at a voltage higher than V_D.**

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Separate analog and digital ground planes that are connected close to the ADC14071 are required to achieve specified performance. The analog and digital grounds may be in the same layer, but should be separated from each other and should never overlap each other. Separation should be at least ⅛ inch (3 mm), where possible.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should not be connected to system ground in close proximity to any of the ADC14071's other ground pins.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and from the digital ground plane, as well as to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by connecting the analog and digital ground planes together beneath the ADC with a copper trace that is very narrow compared with the rest of the ground plane. A typical width is about 1/16 inch (1.5 mm to 2 mm) but will depend upon the total analog ground current that will flow through it. This narrowing provides a fairly high impedance to the high edge rates of the digital switching currents, directing them away from the analog pins. The lower slew rate analog ground currents see a

Applications Information (Continued)

relatively low impedance across this narrow ground connection. This implies that the power supply ground should be connected to the digital ground plane.

Generally, analog and digital lines should cross each other at 90˚ to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep any clock line as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90˚ crossing should be avoided as even a little coupling can cause problems at high frequencies. This is because other lines can introduce phase noise (jitter) into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference pin and ground should be connected to a very clean point in the analog ground plane.

Figure 8 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog ground plane. All digital circuitry and I/O lines should be placed over the digital ground plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with traces and enter the analog ground plane at a single point.

All ground connections should have a low inductance path to ground.

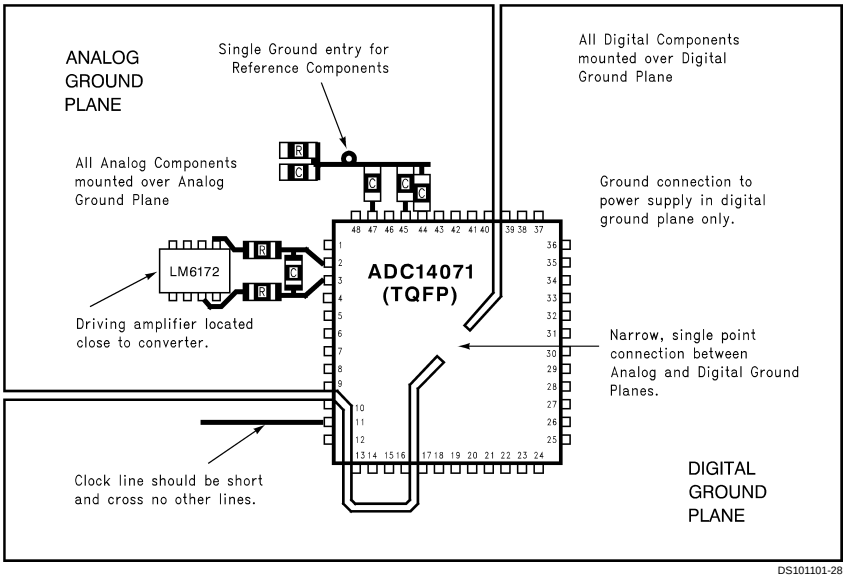


FIGURE 8. Example of A Suitable Layout

6.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance with the ADC14071, the clock source driving the CLK input must be free of jitter. For best ac performance, isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 9*.

As mentioned in Section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce phase noise (jitter) into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90˚ crossings have capacitive coupling, so try to avoid even these 90˚ crossings of the clock line.

Applications Information (Continued)

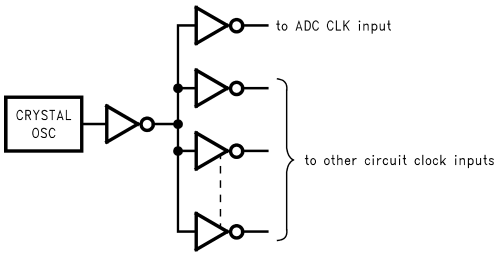


FIGURE 9. Isolating the ADC Clock from other Circuitry with A Clock Tree

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV beyond the supply rails (more than 300 mV below the ground pins or 300 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or more than a volt below ground. A resistor of about 50Ω to 100Ω in series with the offending digital input will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up.

Be careful not to overdrive the inputs of the ADC14071 with a device that is powered from supplies outside the range of the ADC14071 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through DR V_D and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem.

Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC14071, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω.

Using an inadequate amplifier to drive the analog input. As explained in Section 1.3, the capacitance seen at the input alternates between 14 pF and 5 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor across the analog inputs (as shown in *Figures 6, 7*) will improve performance. The LM6172 has been successfully used to drive the analog inputs of the ADC14071.

Also, it is important that te signals at the two inputs have exactly the same amplitude and be exactly 180° out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

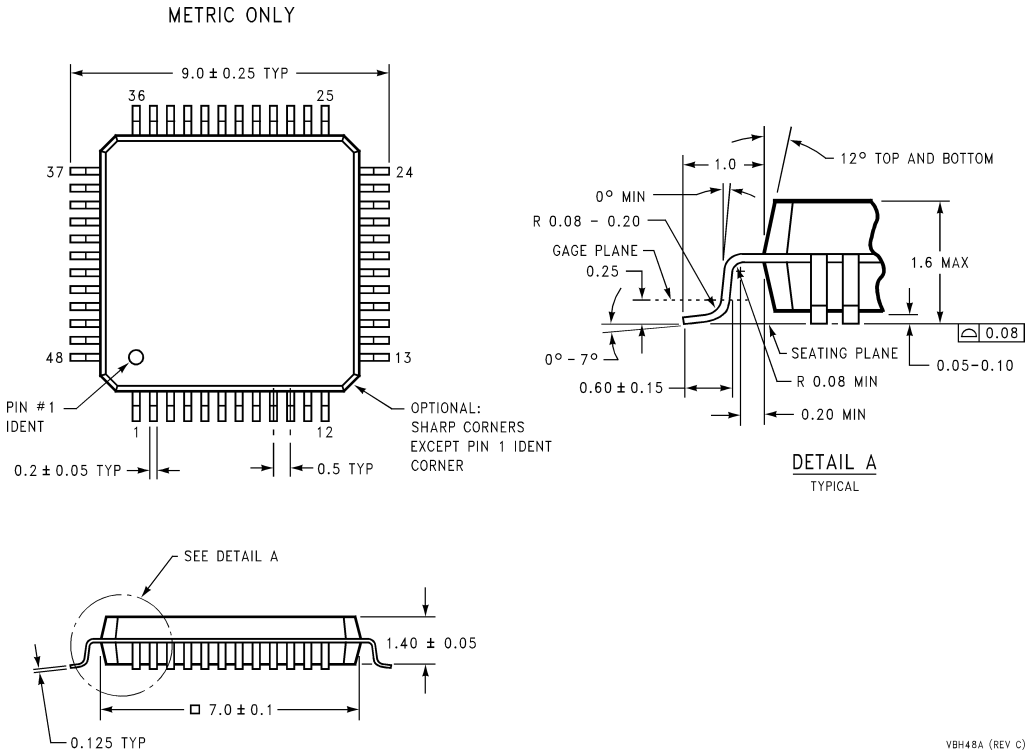
Operating with the reference pins outside of the specified range. As mentioned in Section 1.2, V_{REF} should be in the range of

$$1.0V \leq V_{REF} \leq 2.7V.$$

Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead TQFP Package
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