PRODUCT BRIEF

Z85C80

SCSCI SERIAL COMMUNICATIONS AND SMALL COMPUTER INTERFACE

FEATURES

- Low-Power CMOS
- Two Independent, 0 to 2.5 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop for Clock Recovery.
- Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character, Programmable Clock Factor, Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1s or 0s.
- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.
- Local Loopback and Auto Echo Modes
- Supports T1 Digital Trunk.
- Enhanced DMA Support:
  - 10 X 19-Bit Status FIFO
  - 14-Bit Byte Counter
- Supports SCSI ANSI-X3.131-1986 Standard.
- Arbitration Support
- DMA or Programmed I/O Data Transfers
- Supports Normal DMA
- Memory or I/O Mapped CPU Interface
- Asynchronous Interface Supports 3 Mbytes/sec
- Direct SCSI Bus Interface with On-Board 48 mA Drivers
- Supports Target and Initiator Roles
- Available in 68-pin PLCC, 10 MHz and 16 MHz, and 100-pin VQFP, 16 MHz

GENERAL DESCRIPTION

The Z85C80 CMOS SCSCI is an industry standard 85C30 dual channel Serial Communication Controller (SCC) and an industry standard 53C80 Small Computer System Interface (SCSI) integrated into one monolithic Integrated Circuit. The internal SCC and SCSI share the 8-bit data bus (D7 through D0) and read and write inputs (/RD and /WR).

The Z85C80 is offered in a 68-pin PLCC package in both 10 MHz and 16 MHz speed grades for the SCC interface, and in 100-pin VQFP in the 16 MHz speed grade. The SCSI interface data transfer rate is 3.0 MBytes/sec. With a few exceptions, all of the internal SCC and SCSI signals are connected to the outside pins.

The exceptions are:

- IEI input to SCC is internally connected to VDD.
- IEO output from SCC is not internally connected (N/C).
- READY output from SCSI is not internally connected (N/C).
- /SYNCB output from the SCC is not internally connected (N/C).
- /TRXCA and /CTSA inputs to the SCC are internally connected.
- /TRXCB and /CTSB inputs to the SCC are internally connected.

GENERAL DESCRIPTION *(Continued)*

The internal SCC is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPUs with non-multiplexed address/data buses. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features, including a 10x19-bit status FIFO and 14-bit byte counter, were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. The internal SCC can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. It also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls are used for general-purpose I/O. The daisy-chain interrupt hierarchy is also supported and is standard for Zilog peripheral components.

The internal SCSI is designed to implement the SCSI protocol as defined by the ANSI X3.131-1986 standard, and is fully compatible with the industry standard 53C80. It is capable of operating both as a target and as an initiator. Special high current open-drain outputs enable it to directly interface to, and drive, the SCSI bus. The internal SCSI has the necessary interface hook-ups so the system CPU can communicate with it like with any other peripheral device. The CPU can read from, or write to, the SCSI registers which are addressed as standard or memory-mapped I/Os.

The Internal SCSI increases the system performance by minimizing the CPU intervention in DMA operations which the SCSI controls. The CPU is interrupted by the SCSI when it detects a bus condition that requires attention. It also supports arbitration and reselection. The internal SCSI has the proper hand-shake signals to support normal DMA operations with most DMA controllers available.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056
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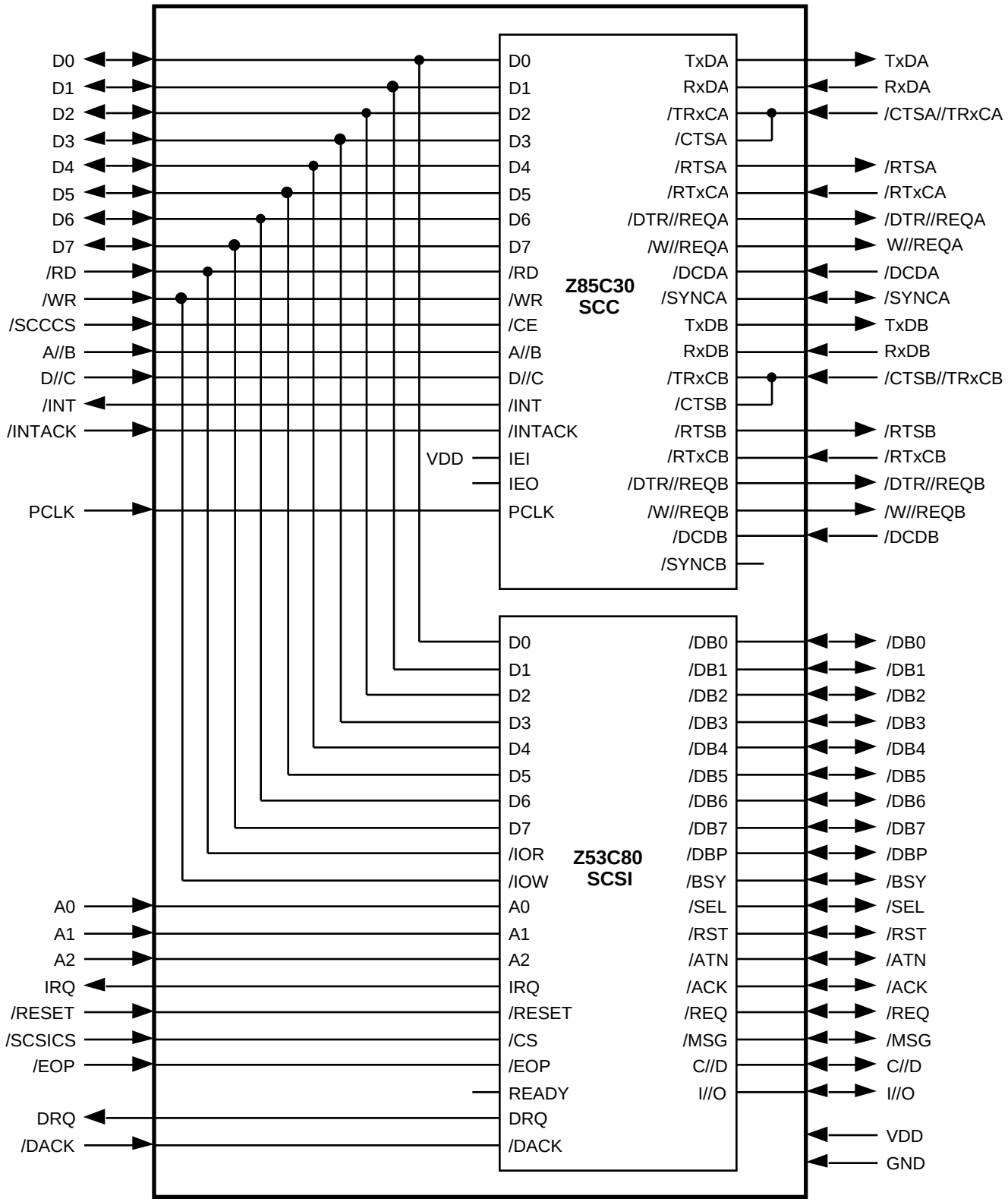

Z85C80 SCSCI Functional Block Diagram

Note: [1]: Pins /CTSB and /TRxCB are bonded out separately in the 100-pin VQFP package and should be externally tied together by the user to meet the pinout specification.