# LZ92E62 Timing Pulse Generator for 1/2″ CCD

## Description

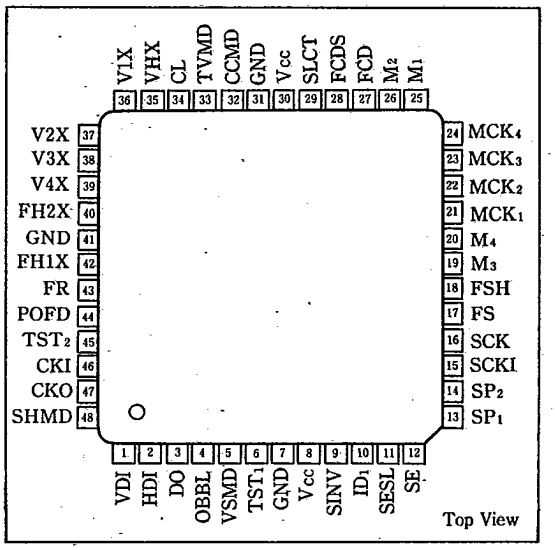
The LZ92E62 is a CMOS LSI which generates the drive timing pulses for CCD and the pulses required in processing the signals from CCD area sensors (LZ2111J, LZ2112J, LZ2121J, or LZ2122J).

It can be used in combination with the synchronous signal generator IC (LZ92E60 or LZ93N19).

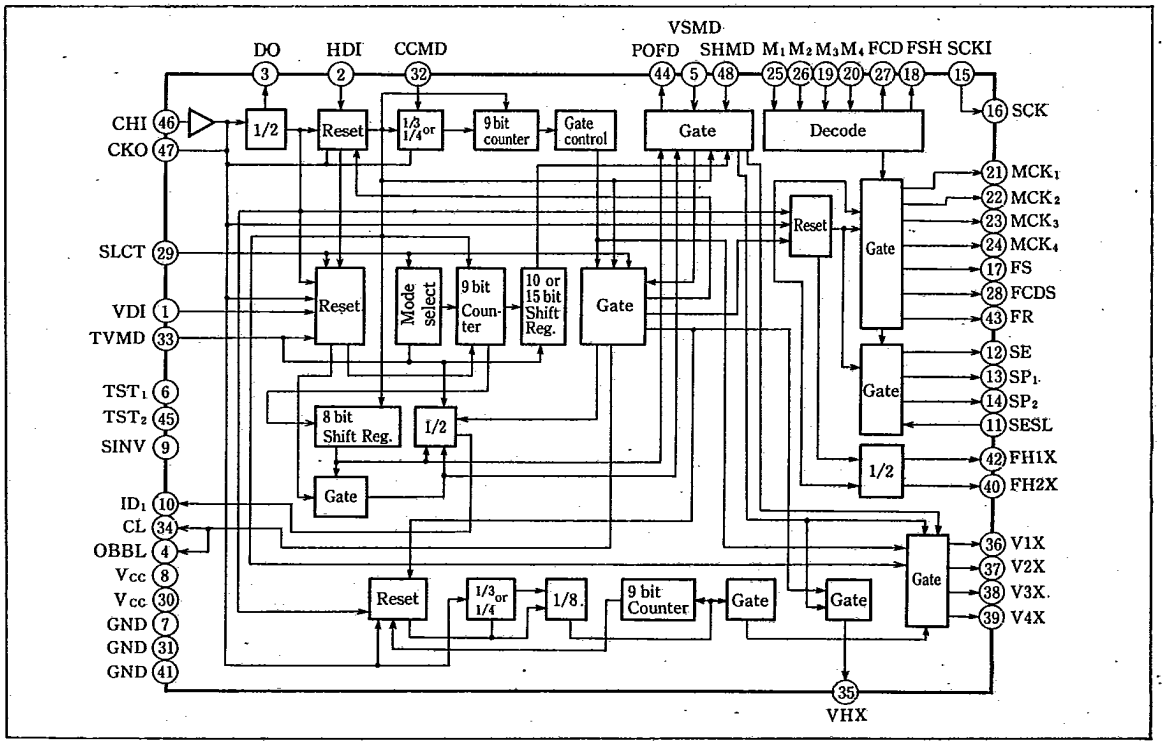
## Features

1. Switchable between NTSC and PAL mode.
2. Switchable between the 1/2″ CCDs of 542 horizontal pixels and 720 horizontal pixels.
3. Electronic shutter function (1/1000 and 1/2000 sec).
4. Single +5V power supply.
5. 48-pin quad flat package.

## Pin Connections




## Block Diagram



## ■ Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | −0.3 to +7 | V | 1 |
| Input voltage | $V_I$ | −0.3 to $V_{CC}$+0.3 | V | 2 |
| Output voltage | $V_O$ | −0.3 to $V_{CC}$+0.3 | V | |
| Output current 1 | $\lvert I_{O1} \rvert$ | 7.0 | mA | 3 |
| Output current 2 | $\lvert I_{O2} \rvert$ | 28.0 | mA | 4 |
| Osc. inverter input voltage | $V_{OSCI}$ | −1.0 to $V_{CC}$+1.0 | V | |
| Power dissipation | $P_D$ | 600 | mW | 5 |
| Oprating temprature | $T_{opr}$ | −10 to +70 | °C | |
| Storage temperature | $T_{stg}$ | −55 to +150 | °C | |

Note 1 : The maximum applicable voltage on $V_{CC}$ with respect to GND.
2 : The maximum applicable voltage on input pins except for $V_{CC}$ with respect to GND.
3 : The maximum current of output buffer with $I_{OL}$=4mA, $I_{OH}$=−2mA.
4 : The maximum current of output buffer with $I_{OL}$=16mA, $I_{OH}$=−8mA.
5 : Ta=60°C

## ■ Recommended Operating Conditions

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Operating temperature | $T_{opr}$ | −10 | | 70 | °C |

## ■ DC Characteristics

($V_{CC}$=5.0V±10%, Ta=−10 to +70°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | | | 1.5 | V | 1 |
| Input "High" voltage | $V_{IH}$ | | 3.5 | | | V | |
| Input "High" threshold voltage | $V_{T+}$ | | | | 3.7 | V | |
| Input "Low" threshold voltage | $V_{T-}$ | | 1.0 | | | V | 2 |
| Hysteresis voltage | $V_{T+}-V_{T-}$ | | 0.4 | | | V | |
| Output "Low" voltage | $V_{OL1}$ | $I_{OL}$=4mA | | | 0.4 | V | 3 |
| | $V_{OL2}$ | $I_{OL}$=16mA | | | 0.4 | V | 4 |
| Output "High" voltage | $V_{OH1}$ | $I_{OH}$=−2mA | 4.2 | | | V | 3 |
| | $V_{OH2}$ | $I_{OH}$=−8mA | 4.2 | | | V | 4 |
| | $V_{OH3}$ | $I_{OH}$=0mA | 4.7 | | | V | 5 |
| Input "High" current | $I_{IH1}$ | $V_I$=$V_{CC}$ | | | 1.0 | μA | 6 |
| | $I_{IH2}$ | $V_I$=$V_{CC}$ | 8.0 | | 50.0 | μA | 7 |
| Input "Low" current | $I_{IL1}$ | $V_I$=0V | | | 1.0 | μA | 8 |
| | $I_{IL2}$ | $V_I$=0V | −50.0 | | −8.0 | μA | 9 |
| Limit oscillation frequency | OSC | | 27.0 | | | MHz | |
| Oscillation inverter I/O capacitance | | | | 5.0 | | pF | |
| Current consumption 1 | $I_{CC1}$ | $V_I$=$V_{CC}$ or GND | | | 10.0 | μA | |
| Current consumption 2 | $I_{CC2}$ | f=10MHz, $V_{IN}$=$V_{CC}$ or GND When in pattern operation | | | 40.0 | mA | |

Note 1 : Applied to all inputs except for VDI, SCKI, $M_1$, $M_2$ inputs.
Note 2 : Applied to VDI, SCKI, $M_1$, $M_2$ inputs.
Note 3 : Applied to all outputs except for FH1X, FH2X outputs.
Note 4 : Applied to FH1X, FH2X outputs.
Note 5 : Applied to FH1X, FH2X, FR outputs. (at $V_{CC}$=5.0V±5%)
Note 6 : Applied to all inputs except for $TST_1$, $TST_2$, SESL inputs.
Note 7 : Applied to $TST_1$, $TST_2$, SESL inputs.
Note 8 : Applied to all inputs except for $M_1$, $M_2$, $M_3$, $M_4$ inputs.
Note 9 : Applied to $M_1$, $M_2$, $M_3$, $M_4$ inputs.

## Pin Function

| Pin No. | Symbol | I/O | Pin name | Function |
|---|---|---|---|---|
| 1 | $V_{DI}$ | ICS | V reference | An input pin for the V reference signal. Connect to $V_D$ (pin 34) of SSG IC (LZ92E60 or LZ93N19). |
| 2 | HDI | IC | Hor. reference | An input pin for the Hor. reference signal. Connect to HD (pin 31) of SSG IC (LZ92E60 or LZ93N19). |
| 3 | DO | O | 1/2 driving output | The frequency is 1/2 of the signal to CKI (pin 46) and connect to CLKI (pin 27) of SSG IC (LZ92E60 or LZ93N19). |
| 4 | OBBL | O | Optical black control output | The pulse to be used to stop $BCP_1$ (pin 37) signal and $BCP_2$ (pin 38) signal of SSG IC (LZ92E60 or LZ93N19). Connect to CPBL (pin 36) of SSG IC. |
| 5 | VSMD | IC | Shutter speed selection | An input pin for selecting shutter speed. L level : 1/1000 sec, H level : 1/2000 sec |
| 6 | $TST_1$ | ICD | Test pin 1 | A test pin. Set open or to L level in normal mode. |
| 7 | GND | — | Ground | A ground pin. |
| 8 | $V_{CC}$ | — | Power supply | Supply+5V power. |
| 9 | SINV | IC | Carrier polarity selection | An input pin for reversing polarity of color demodulation carrier at SE (pin 12). |
| 10 | $ID_1$ | O | Line index pulse | The pulse is used in color separator. The signal switches between H and L at every lines. It resets at the 14th line when in NTSC mode, and at the 9th line when in PAL mode. |
| 11 | SESL | ICD | Carrier phase selection | An input pin for selecting the phase of SE (pin 12). L level : synchronizes with the rising edge of FH2X (pin 36). H level : synchronizes with the rising edge of FH1X (pin 35). |
| 12 | SE | O | Carrier for demodulation | A pulse to demodulate the signal from CCD. A 1/4 dividing output of CKI (pin 46). The carrier phase selection can be made at SESL (pin 11) and SINV (pin 9). |
| 13 | $SP_1$ | O | Color sampling pulse 1 | A pulse to be used for the color separation circuit which sample-holds the signal from CCD. It is output when the SE (pin 12) is "Low". |
| 14 | $SP_2$ | O | Color sampling pulse 2 | A pulse to be used for the color separation circuit which sample-holds the signal from CCD. It is output when the SE (pin 12) is "High". |
| 15 | SCKI | ICS | Phase adjust input 1 | An input pin for phase adjustment. It is a Schmitt trigger input. |
| 16 | SCK | O | Phase adjust output 1 | An output pin of SCKI (pin 15). |
| 17 | FS | O | Sampling pulse 1 | A pulse to sample-hold the signal from CCD. |
| 18 | FSH | O | Sampling pulse 2 | A pulse to sample-hold the signal from CCD. The output is a logical AND of $M_3$ (pin 19) and $M_4$ (pin 20) input. |
| 19<br>20 | $M_3$<br>$M_4$ | ICSU<br>ICSU | FS phase control | Pins to control the phase between FH1X (pin 35) and FS (pin 17).<br>$M_3$: 1, 0, 0, 1<br>$M_4$: 1, 1, 0, 0<br>phase difference: $t_d$, $t_d$+1.5, $t_d$+3.0, $t_d$+4.5<br>Also control the phase of FSH (pin 18). |
| 21 | $MCK_1$ | O | 1/2 dividing output 1 | A 1/2 dividing output of CKI (pin 46). The output phase is approx. the same as FH2X (pin 36). |
| 22 | $MCK_2$ | O | 1/2 dividing output 2 | A 1/2 dividing output of CKI (pin 46). The output phase is delayed by approx. 90 degree from FH2X (pin 36). |
| 23 | $MCK_3$ | O | 1/2 dividing output 3 | A 1/2 dividing output of CKI (pin 46). The output phase is approx. the same as FH1X (pin 35). |
| 24 | $MCK_4$ | O | 1/2 dividing output 4 | A 1/2 dividing output for CKI (pin 46). The output phase is delayed by approx. 90 degree from FH1X (pin 35). |

| Pin No. | Symbol | I/O | Pin name | Function |
|---|---|---|---|---|
| 25<br>26 | $M_1$<br>$M_2$ | ICSU<br>ICSU | FCDS phase control<br>FCD input | Pins to control the phase between FH1X (pin 35) and FCDS (pin 28).<br>unit ($\mu$s)<br>$M_1$: 1 0 0 1<br>$M_2$: 1 1 0 0<br>phase difference: $t_d$ $t_d+1.5$ $t_d+3.0$ $t_d+4.5$<br>It is a Schmitt trigger input which also control the phase of FCD (pin 27). |
| 27 | FCD | O | FCDS pulse 2 | A pulse to clamp the output signal from CCD. The output is a logical AND of $M_1$ (pin 25) and $M_2$ (pin 26). |
| 28 | FCDS | O | FCDS pulse 1 | A pulse to clamp the output signal from CCD. |
| 29 | SLCT | IC | SSG selection | An input pin to select SSG IC.<br>Set to H level when LZ92E60 or LZ93N19 is used as SSG IC. |
| 30 | $V_{CC}$ | — | Power supply | Supply+5V power. |
| 31 | GND | — | Ground | A ground pin. |
| 32 | CCMD | IC | CCD selection | An input pin to select CCD types.<br>L level : CCD of 542 horizontal pixels.<br>H level : CCD of 720 horizontal pixels. |
| 33 | TVMD | IC | NTSC/PAL selection | A pin for select TV standards.<br>L level : NTSC system.<br>H level : PAL system. |
| 34 | CL | O | Cleaning pulse | The pulse becomes Low during the cease period of horizontal transter pulses. |
| 35 | VHX | O | Read out pulse | A pulse that transfers the charge of the photodiode to the vertical register.<br>Connect to $\overline{1B}$ (pin 14) and 2B (pin 20) of V-driver IC (LR36682). |
| 36 | V1X | O | Vertical transfer pulse 1 | A vertical transfer pulse for CCD. Connect to $\phi_{V1}$ through V-driver IC (LR36682). |
| 37 | V2X | O | Vertical transfer pulse 2 | A vertical transfer pulse for CCD. Connect to $\phi_{V2}$ through V-driver IC (LR36682). |
| 38 | V3X | O | Vertical transfer pulse 3 | A vertical transfer pulse for CCD. Connect to $\phi_{V3}$ through V-driver IC (LR36682). |
| 39 | V4X | O | Vertical transfer pulse 4 | A vertical transfer pulse for CCD. Connect to $\phi_{V4}$ through V-driver IC (LR36682). |
| 40 | FH2X | O | Hor.transfer pulse 2 | A horizontal transfer pulse for CCD. Connect to $\phi_{H1}$ of CCD. |
| 41 | GND | — | Ground | A ground pin. |
| 42 | FH1X | O | Hor. transfer pulse 1 | A horizontal transfer pulse for CCD. Connect to $\phi_{H2}$ of CCD. |
| 43 | FR | O | Reset pulse | A reset pulse for CCD.<br>Connect to $\phi_R$ of CCD through DC level shift circuit. |
| 44 | POFD | O | OFD control pulse | A pulse to control OFD voltage when 1/2000 sec electronic shutter is operated. |
| 45 | $TST_2$ | ICD | Test pin 2 | A test pin. Set open or to L level in normal mode. |
| 46 | CKI | ICK | Clock input | An input for reference clock.<br>The frequencies are as follows:<br>NTSC mode (TVMD=L)<br>1212fH(CCMD=L) for CCD of 542 hor. pixels<br>1616fH(CCMD=H) for CCD of 720 hor. pixels<br>PAL mode (TVMD=H)<br>1236fH(CCMD=L) for CCD of 542 hor. pixels<br>1648fH(CCMD=H) for CCD of 720 hor. pixels<br>fH=Hor. frequency |
| 47 | CKO | OCK | Clock output | The output is the inverse CKI (pin 46). |
| 48 | SHMD | IC | Shutter mode select | Select shutter mode.<br>L level : 1/60 sec. H level : 1/1000 or 1/2000 sec |

IC : Inputs (CMOS level).
O : Outputs.
ICD : Inputs (CMOS level, with pull-down resistor).
ICS : Schmitt-trigger Inputs (CMOS level).
ICSU : Schmitt-trigger Inputs (CMOS level, with pull-up resistor).
ICK : Oscillator Input.
OCK : Oscillator Output.

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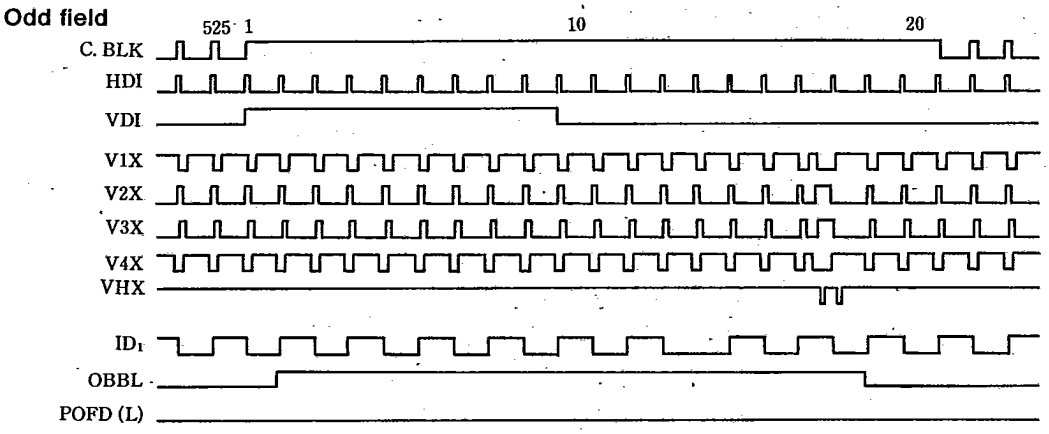
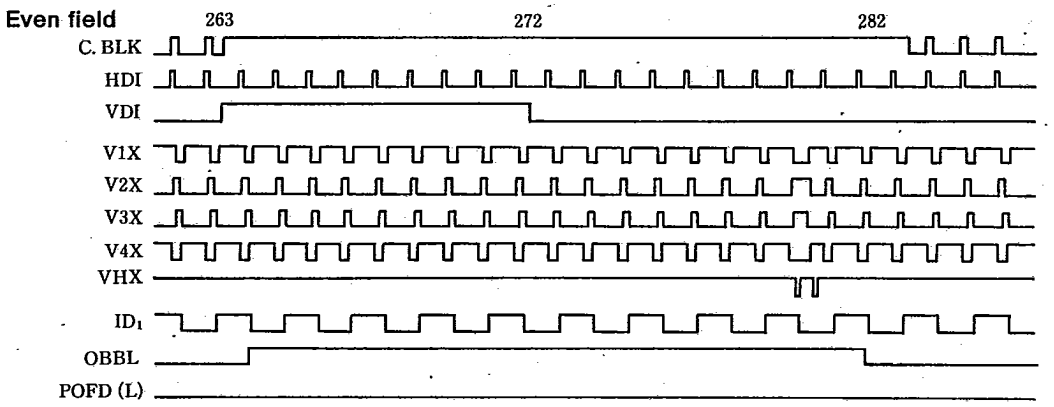
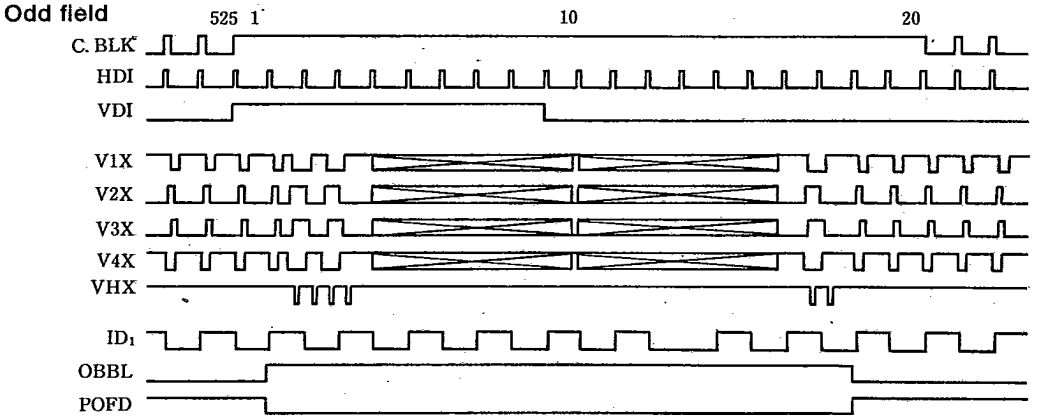
## ■ Timing Diagrams

### (1) NTSC vertical timing 1 (Electronic shutter speed : 1/60 sec)

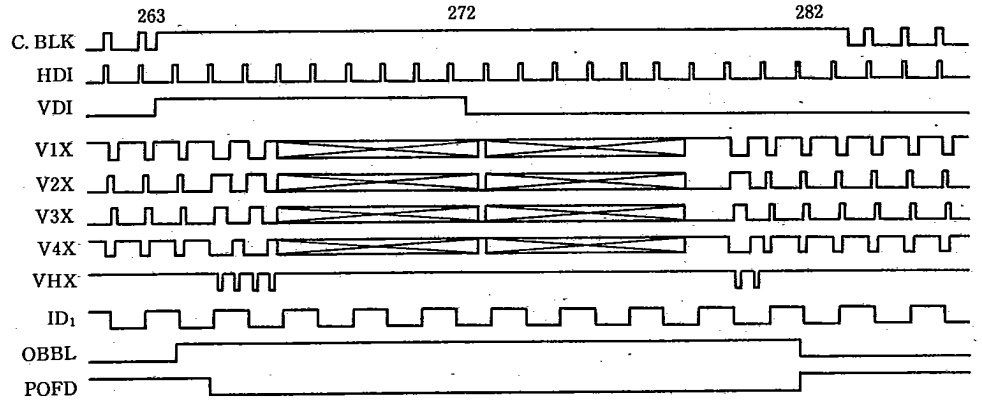



### (2) NTSC vertical timing 2 (Electronic shutter speed : 1/1000 sec)

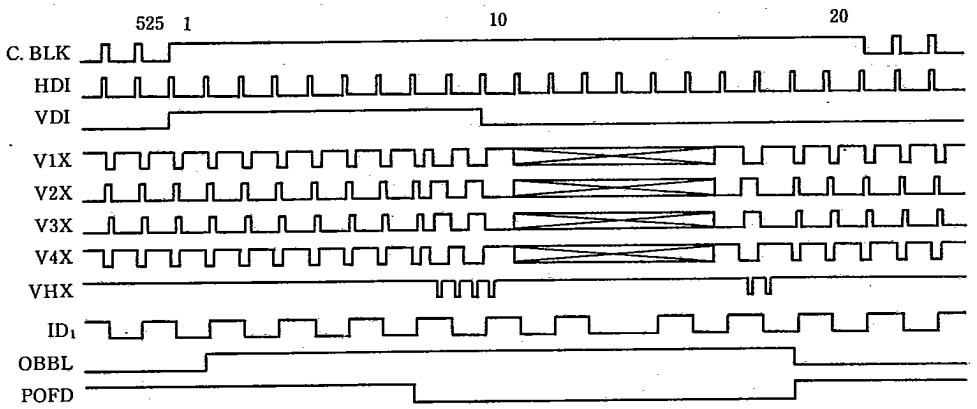


Even field

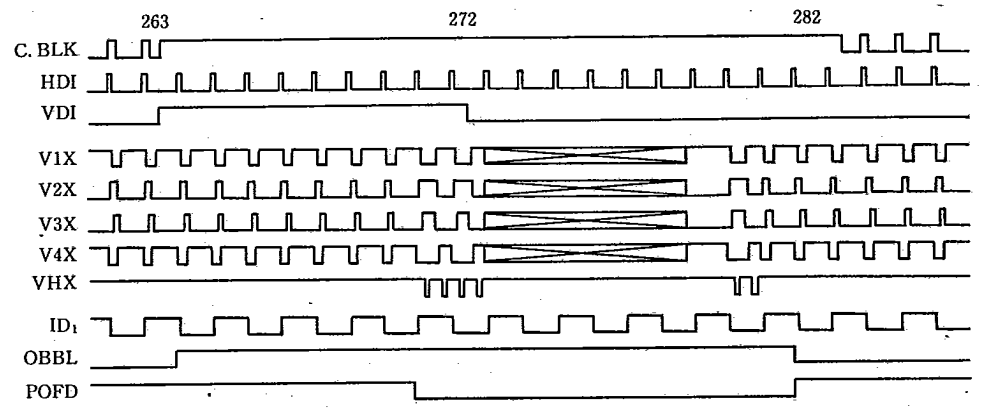



(3) NTSC vertical timing 3 (Electronic shutter speed : 1/2000 sec)

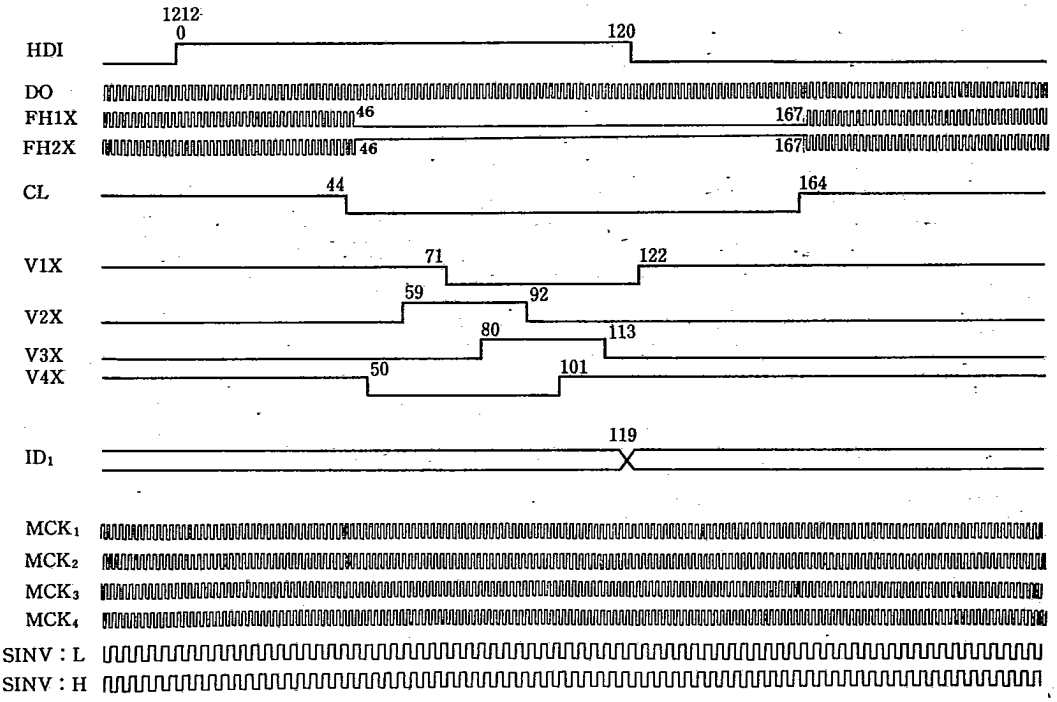
Odd field



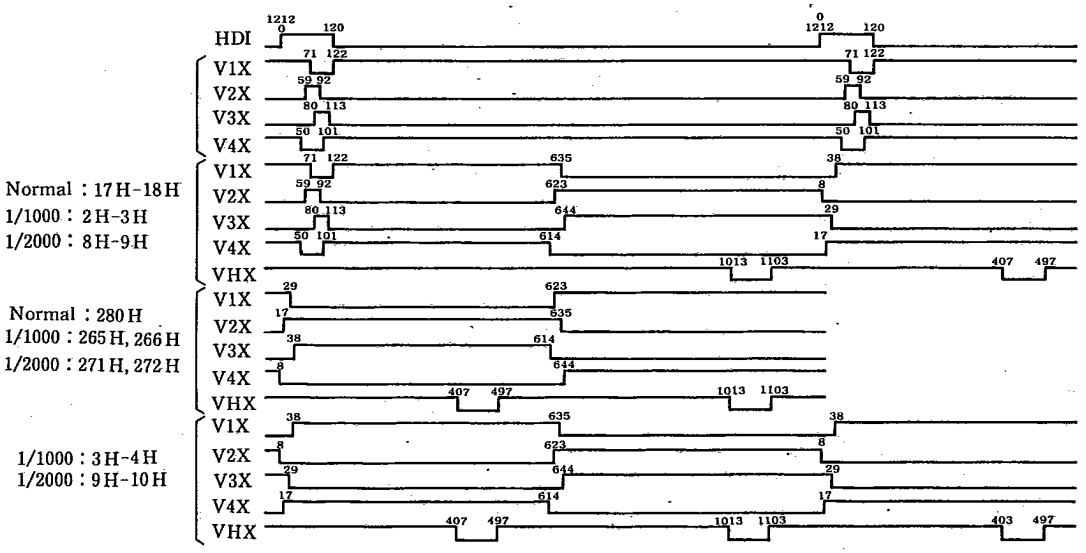

Even field



### (4) NTSC horizontal timing 1 (542 hor. pixels)

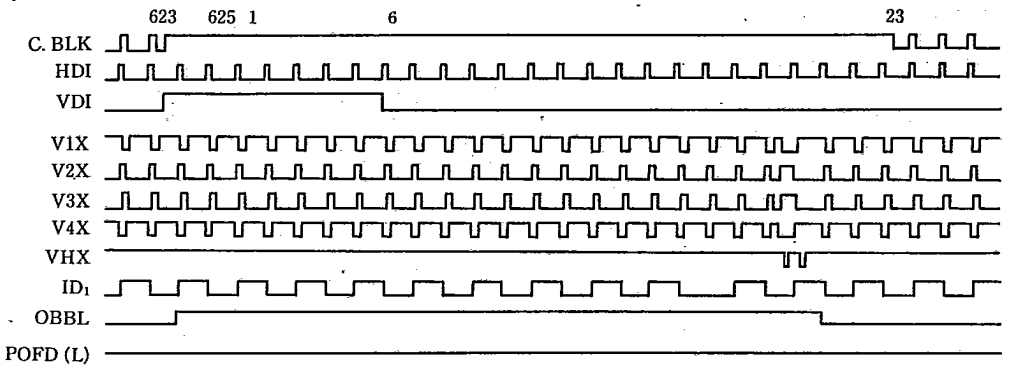



### (5) NTSC horizontal timing 2 (542 hor. pixels)

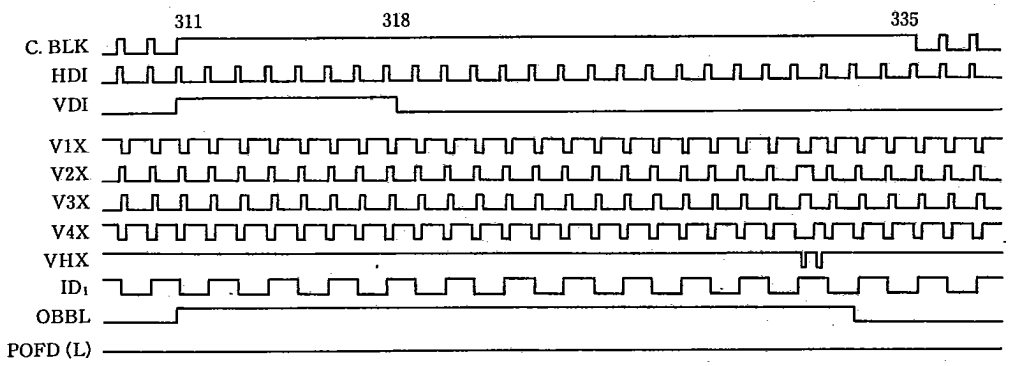


(6) PAL vertical timing 1 (Electronic shutter speed 1/60 sec) T-41-55

1st and 3rd field

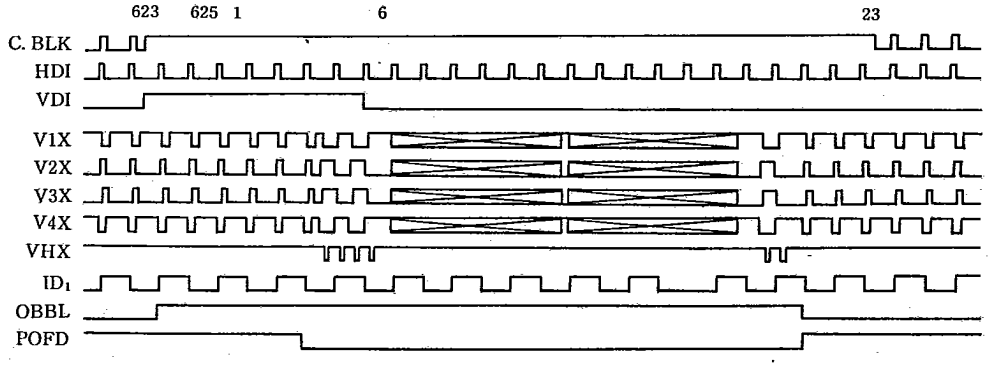



2nd and 4th field

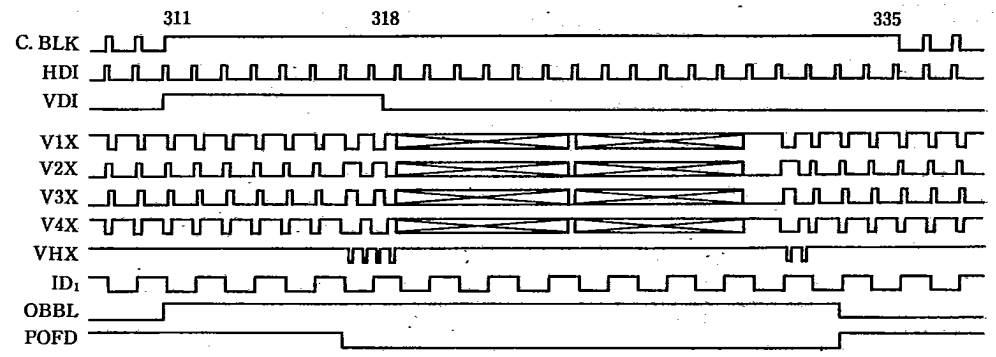



(7) PAL vertical timing 3 (Electronic shutter speed : 1/1000 sec)

1st and 3rd field

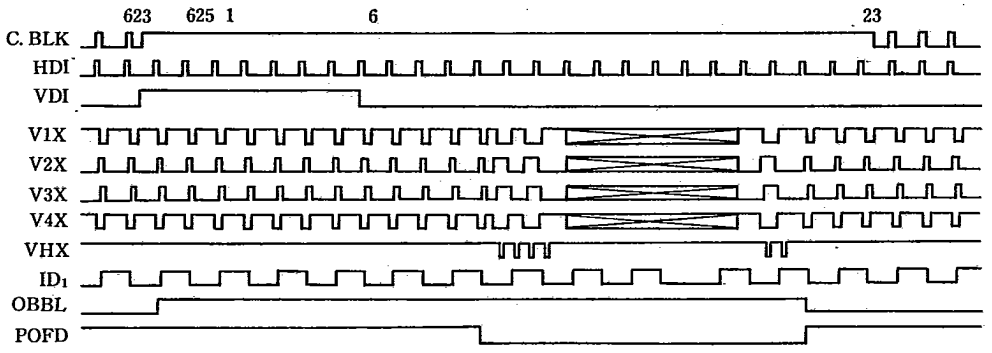


**2nd and 4th field**

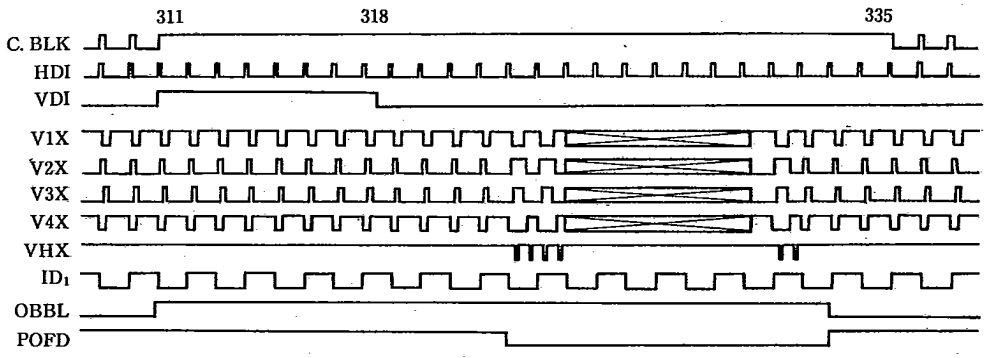



**(8) PAL vertical timing 3 (Electronic shutter speed : 1/2000 sec)**

**1st and 3rd field**




**2nd and 4th field**



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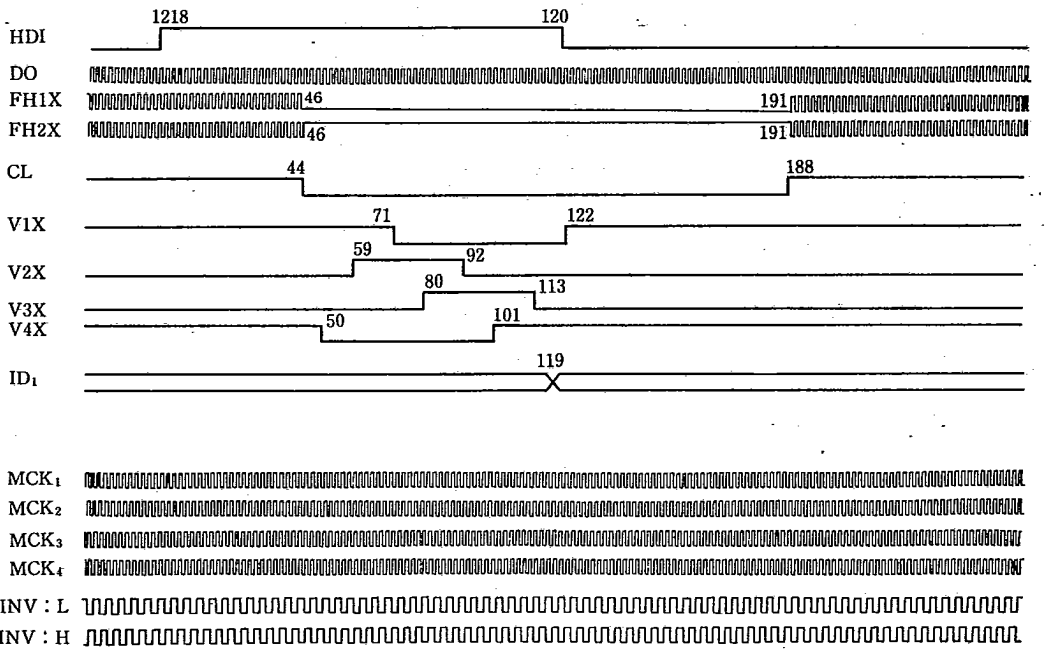
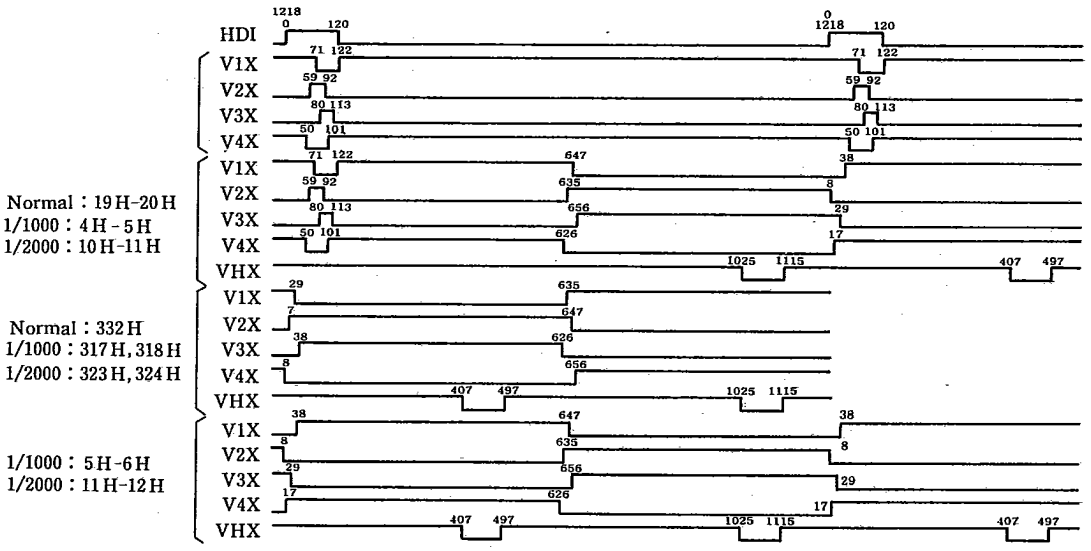
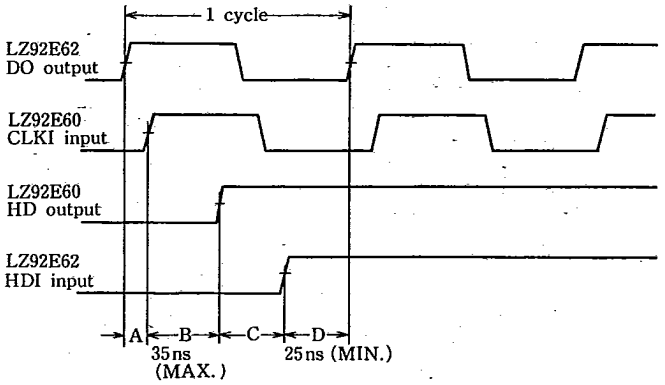
## (9) PAL horizontal timing 1

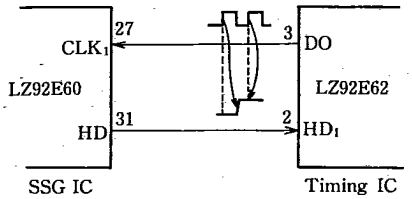



## (10) PAL horizontal timing 2 (542 hor. pixels)



### (11) Relationship of input phase among DO, HD and $HD_1$




One cycle of DO output is 104ns for a 512-pixel (H) CCD, and 79ns for a 760-pixel (H) CCD.

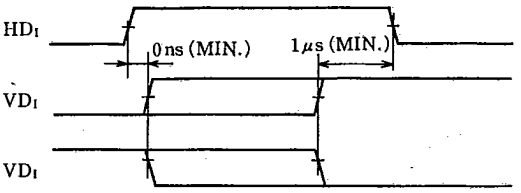
When a clock from the LZ92E62 is given to CLKI input of the LZ92E60, a horizontal drive pulse is output from HD output of the LZ92E60 after internal delay time of 35ns MAX. (B interval).

The pulse is input to $HD_1$ input of the LZ92E62. It is necessary to take a "D" interval for at least 25ns for making an H reference signal after one cycle of DO.

Accordingly, allowable delay time (A+C interval) caused by wiring between LSIs should be 44ns or less for a 512-pixel (H) CCD and 19ns or less for a 760-pixel (H) CCD.

### (12) Relationship of input phase between $HD_1$ and $VD_1$

①NTSC : Odd Field, PAL : 2nd and 4th Field




②NTSC : Even Field, PAL : 1st and 3rd Field