LZ92E60 Synchronizing Signal Generator for 1/2" CCD

Description

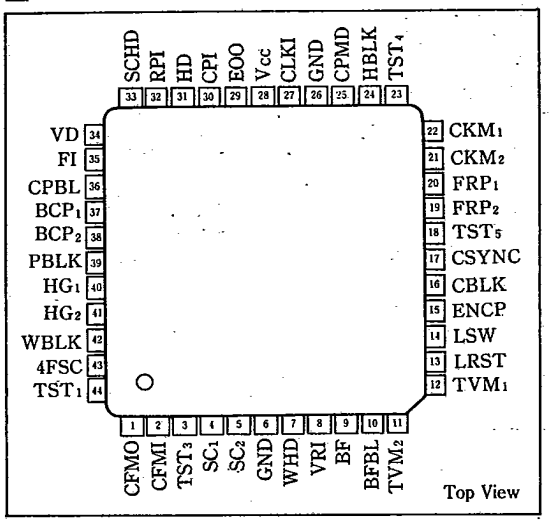
The LZ92E60 is a CMOS LSI which generates the synchronizing pulses conforming to two diffrent television standard and the pulses required in processing the signals from CCD area sensors (LZ2111J, LZ2112J, LZ2121J or LZ2122J).

It can be used in combination with the timing LSI (LZ92E62 or LZ93N25).

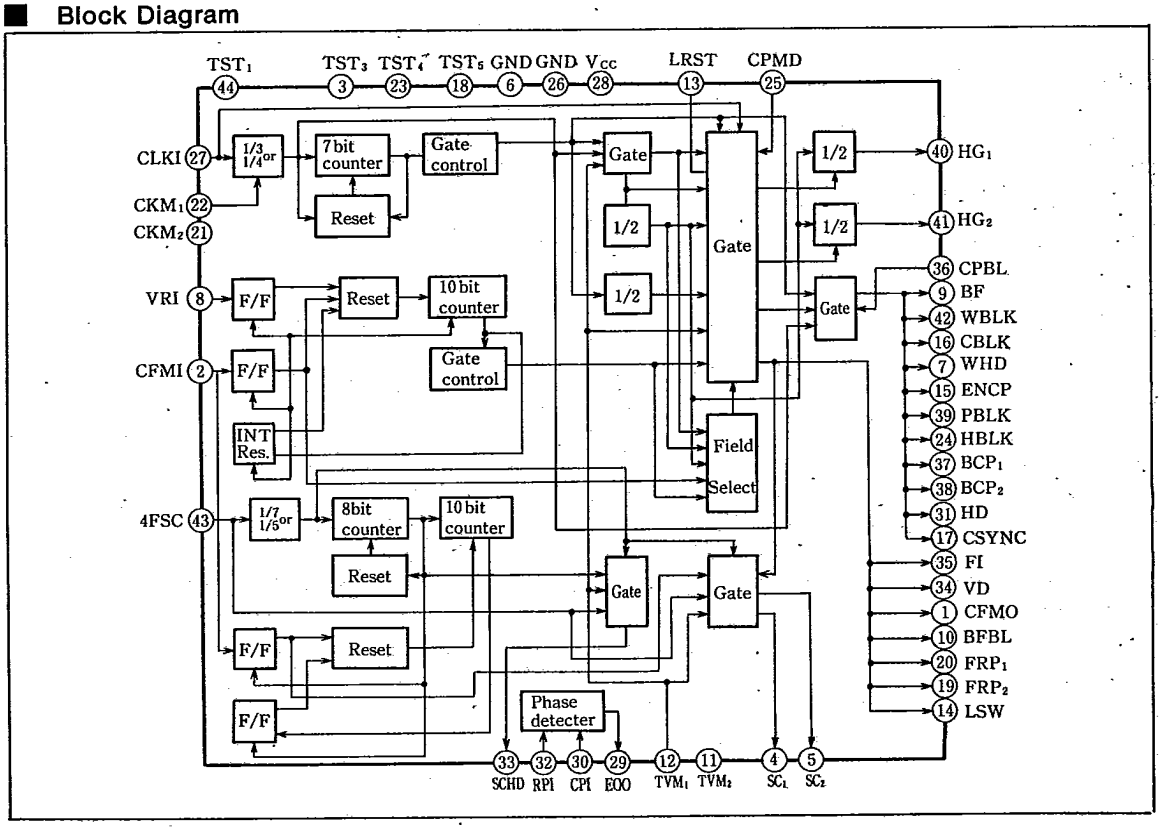
Features

1. Switchable between NTSC and PAL mode.
2. Switchable between the 1/2"CCDs of 542 horizontal pixels and 726 horizontal pixels.
3. Single +5V power supply.
4. 44-pin quad flat package.

Pin Connections



Block Diagram



5

T-41-55

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7	V
Input voltage	V_I	−0.3 to V_{CC}+0.3	V
Output voltage	V_O	−0.3 to V_{CC}+0.3	V
Output current	I_O	7	mA
Power dissipation	P_D	500	mW
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

* All voltages are in reference to the substrate voltage (GND).

Recommemded Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	T_{opr}	−10		+70	℃

DC Characteristics

(V_{DD}=5V±10%, Ta=−10 to +70℃)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V_{IL}				1.5	V	1
Input "High" voltage	V_{IH}		3.5			V	
Input "High" threshold voltage	V_{T+}	Schmitt buffer			3.7	V	2
Input "Low" threshold voltage	V_{T-}	Schmitt buffer	1.0			V	
Hysteresis voltage	V_{T+}-V_{T-}	Schmitt buffer	0.4		2.0	V	
Output "Low" voltage	V_{OL1}	I_{OL}=4mA			0.4	V	3
Output "High" voltage	V_{OH1}	I_{OH}=−2mA	4.0			V	
Output "Low" voltage	V_{OL2}	I_{OL}=0mA			0.1	V	
Output "High" voltage	V_{OH2}	I_{OH}=0mA	V_{CC}−0.1V			V	
Current consumption 1	I_{CC1}	V_{IN}=V_{CC} or GND			10.0	μA	
Current consumption 2	I_{CC2}	V_{IN}=V_{CC} or 0V f=10MHz			30.0	mA	
Operating frequency	f			27		MHz	
Input "High" current	I_{IH1}	V_{IH}=V_{CC}	−1.0		1.0	μA	4
	I_{IH2}	V_{IH}=V_{CC}	8.0		50.0	μA	5
Input "Low" current	I_{IL1}	V_{IL}=0V	−1.0		1.0	μA	4
	I_{IL2}	V_{IL}=0V	−50.0		−8.0	μA	6
Output leakage current	I_{OZ}	High impedance state	−1.0		1.0	μA	7

Note 1 : Applied to all inputs except for VRI inputs.
Note 2 : Applied to all pins which have Schmitt input buffers at CMOS level.
Note 3 : Applied to all outputs.
Note 4 : Applied to all inputs which have no pull-up and pull-down resistors.
Note 5 : Applied to all inputs which have input buffers with pull-down resistors.
Note 6 : Applied to all inputs which have input buffers with pull-up resistors.
Note 7 : Applied to EOO output.

Pin Function

Pin No.	Symbol	I/O	Pin name	Function
1	CFMO	O	Color frame output	A pulse to control color frame ; Occurs at every 4 fields in NTSC mode, occurs at every 8 fields in PAL mode.
2	CFMI	IC	Color frame input	An input pin for color frame pulses ; Connect to CFMO (pin 1) in internal sync. mode. Connect to L level when 4FSC (pin 43) is set to L level.
3	TST_3	ICD	Test pin 3	A test pin. Set open or to L level in the normal mode.
4	SC_1	O	Subcarrier output 1	An output pin for color subcarrier. The frequency of the signal is 1/4 the 4FSC frequency (pin 43). The signal is reset by color frame pulses CFMI (pin 2).
5	SC_2	O	Subcarrier output 2	An output pin for color subcarrier. When the phase of SC_1(pin 4) is 180 degree, the phase of SC_2 is 90 degree in NTSC mode ; in PAL mode, the phase of SC_2 is 90 degree when LSW (pin 14) is Low and 270 degree when LSW is High.
6	GND		Ground	A ground pin.
7	WHD	O	Wide Hor. drive output	An output pin for wide Hor. drive pulse. The pulse width is equal to that of PBLK (pin 39) and is the repetition of horizontal frequency.
8	VRI	ICSU	Vertical reset	An external reset signal input pin to reset the internal vertical counter. Set to H level in normal mode.
9	BF	O	Burst flag	A pulse to define burst period.
10	BFBL	O	Burst flag blanking	NTSC mode : H level. PAL mode : L level during the blanking period of BF (pin 9) otherwise, stays at H level.
11	TVM_2	IC	TV mode 2	Set to level.
12	TVM_1	IC	TV mode 1	An input pin to select TV standards. NTSC mode : L level, PAL mode : H level
13	LRST	ICU	Line switch reset	An input pin to reset the output from LSW (pin 14). Set to H level in normal mode.
14	LSW	O	Line switch	The signal switches between H and L at every line. It is set to low level at the 1st line of the 1st field, when in internal sync.
15	ENCP	O	Encoder DC clamp	A clamp pluse that is used for recovering DC level. The repetition is at a horizontal frequency.
16	CBLK	O	Composite blanking	Composite blanking pulses. in NTSC mode ; H : 11.01 μs, V : 20H period in PAL mode ; H : 12.12 μs, V : 25H period
17	CSYNC	O	Composite synchronizing signal	A composite sync. signal that comforms to RS-170 in NTSC mode and to CCIR in PAL mode.
18	TST_5	I	Test pin 5	A test pin. Set open or to L level in normal mode.
19	FRP_2	O	Frame read pulse 2	A clock output that is used for video servo. The pulse occurs at 2nd field and its repetition is frame period.
20	FRP_1	O	Frame read pulse 1	A clock output that is used for video servo. The pulse occurs at 1st field and its repetition is frame period.
21	CKM_2	IC	Clock mode 2	Set to L level.
22	CKM_1	IC	Clock mode 1	A pin to select the factor of frequency division. Division: 1/3 / 1/4 CKM_1: Low / High Pixels — NTSC: 270,000 / 360,000; PAL: 320,000 / 420,000
23	TST_4	ICD	Test pin 4	A test pin. Set open or to L level in normal mode.
24	HBLK	O	Hor.blanking pulse	A pulse that corresponds to the cease period of the horizontal transfer pulse.

Pin No.	Symbol	I/O	Pin name	Function
25	CPMD	IC	Clamp pulse mode select	An input pin to stop or continue BCP_1 (pin 37) and BCP_2 (pin 38) pulses within the vertical blanking period. L level : continuous output of BCP_1 and BCP_2. H level : becomes low level during the absence of effective pixels within V blanking period.
26	GND		Ground	A ground pin.
27	CLKI	IC	Main clock	An input pin for reference clock. Connect to DO (pin 3) of timing IC (LZ92E62) ; following frequencies appear on this pin ; NTSC mode : 9.534964MHz when CKM_1=Low 12.713285MHz when CKM_1=High PAL mode: 9.656250MHz when CKM_1=Low 12.875000MHz when CKM_1=High
28	V_{CC}	—	Power supply	Supply +5V power.
29	EOO	TO	Phase comparator output	Phase comparator output for input signals RPI (pin 32) and CPI (pin 30). When CPI is advanced, output is Low. When CPI is delayed, output is High. When phases are equal, output is high impedance.
30	CPI	IC	Hor. comparison input	An input pin for comparison Hor. signal to the phase comparator. Connect to SCHD (pin 33) when comparator is used. Set to Low when comparator is not used.
31	HD	O	Hor.drive pulse	The pulse occurs at the start of lines. Connect to HDI (pin 2) of timing IC (LZ92E62).
32	RPI	IC	Hor. reference input	An input pin for the reference Hor. signal to the phase comparator. Connect to HD (pin 31) when comparator is used. Set to Low when comparator is not used.
33	SCHD	O	Subcarrier H	A Hor. sync. pulse obtained by dividing 4FSC (pin 43) NTSC mode : dividing into 1/910 4FSC. PAL mode : dividing into 1/1135 4FSC ordinarilly and dividing into 1/1137 4FSC during one Hor. period within the V blanking. When the PLL is composed of SCHD and HD, sufficient time constant of low pass filter should be taken due to they include f_H and min. $f_V/2$ of frequency components.
34	VD	O	V drive pulse	The pulse occurs at the start of every fields. Connect to VDI (pin 1) of timing IC (LZ92E62).
35	FI	O	Field index pulse	The pulse is used for detecting field. NTSC 1st field : L level. 2nd field : H level PAL 1st and 3rd fields : L level 2nd and 4th fields : H level
36	CPBL	IC	Blanking clamp pulses	The pulse input pin is used to cease the BCP_1 (pin 37) and BCP_2 (pin 38) outputs. When the input is high, BCP_1 (pin 37) and BCP_2 (pin 38) are Low.
37	BCP_1	O	Optical black clamp pulse 1	A pulse to clamp the optical black signal. This pulse is continuous at Hor. cycle. When CPMD is high, output stays low during the absence of effective pixels within the Ver. blanking, otherwise is continuous at Hor. cycle.
38	BCP_2	O	Optical black clamp pulse 2	BCP_2 is the same as BCP_1 (pin 37) excepting that BCP_2 is delayed by 9 μs from BCP_1.

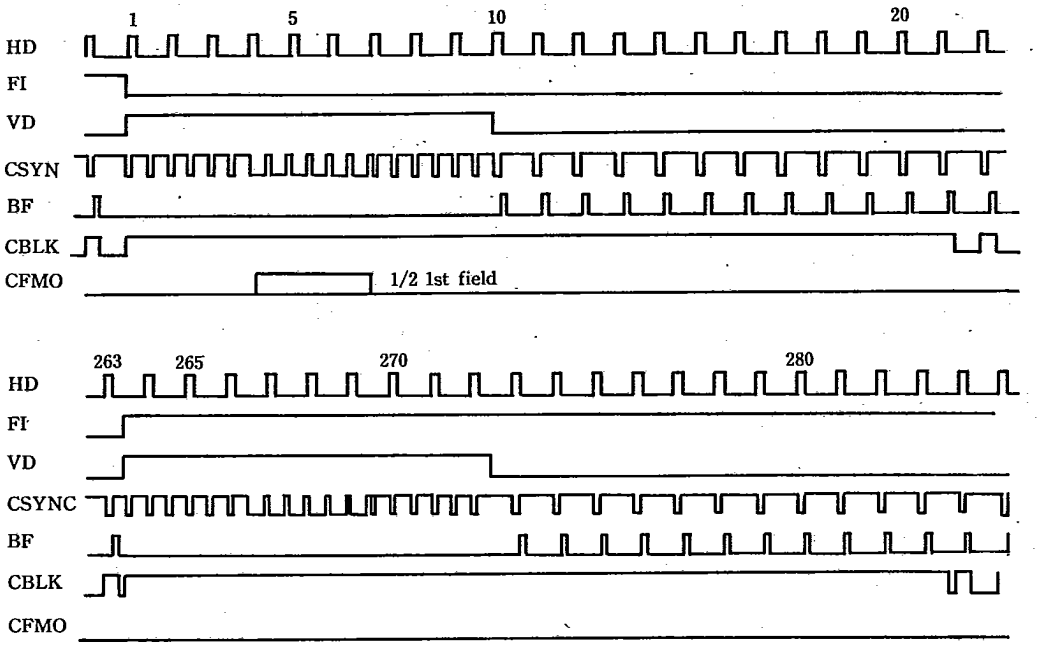
Pin No.	Symbol	I/O	Pin name	Function
39	PBLK	O	Pre-blanking pulse output	Equivalent to CBLK (pin 16) pulse except for shorter pulse width with cut-off trailing edge.
40	HG_1	O	Line index pulse 1	The pulse is used in color separator. The signal switches between H and L at every lines. It resets at the 14th line when in NTSC mode, and at the 9th line when in PAL mode.
41	HG_2	O	Line index pulse 2	The pulse is used in color separator. The signal switches between H and L at every lines. It resets at the 277th line when in NTSC mode, and at the 322nd line when in PAL mode.
42	WBLK	O	Wide blanking output	Equivalent to CBLK (pin 16) excepting that its pulse width is wider than that of CBLK.
43	4FSC	IC	4FSC input	An input pin for the signal 4 times the color subcarrier frequency. NTSC mode : 14.318180 MHz PAL mode : 17.734475 MHz Connect to L level, when SC_1 (pin 4) and SC_2 (pin 5) signals are not required.
44	TST_1	ICD	Test pin 1	A test pin. Set open or to L level in the normal mode.

IC : Inputs (CMOS level).
ICD : Inputs (CMOS level, with pull-down resistor).
ICSU : Schmitt-trigger Inputs (CMOS level, with pull-up resistor).
ICU : Inputs (CMOS level, with pull-up resistor).
O : Outputs.
TO : Tri-state-Output.

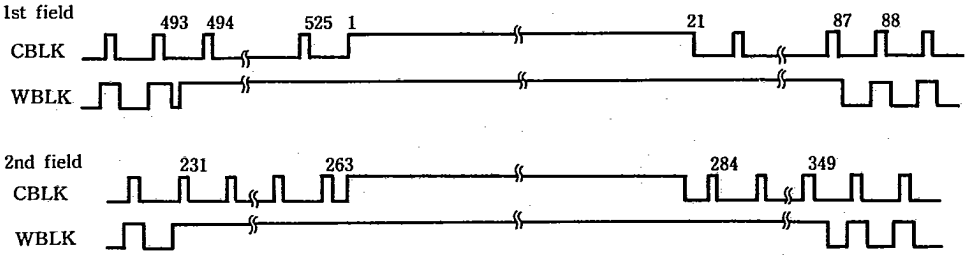
5

■ Timing Diagram

(1) NTSC vertical timing



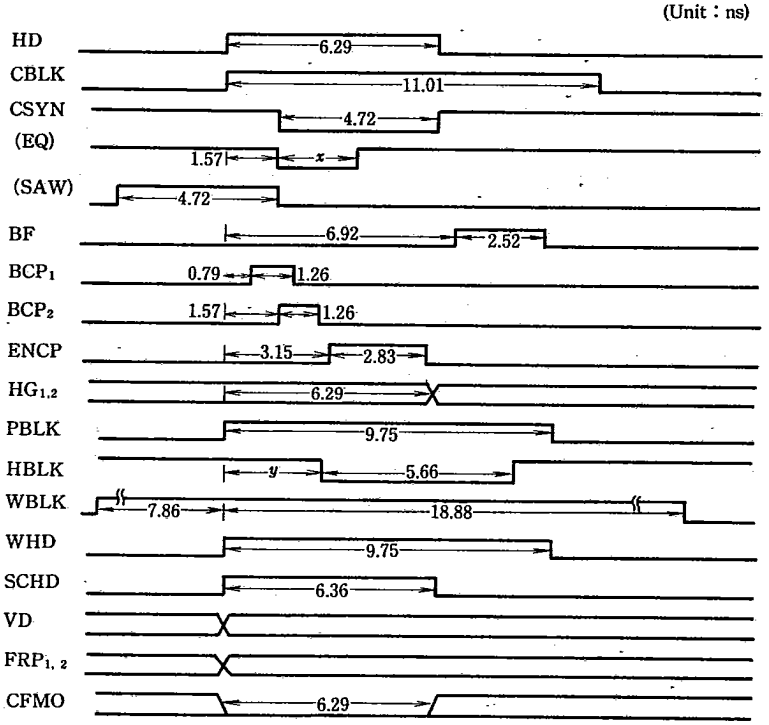
(2) NTSC WBLK vertical timing



T-41-55

(3) NTSC horizontal timing

(Unit : ns)

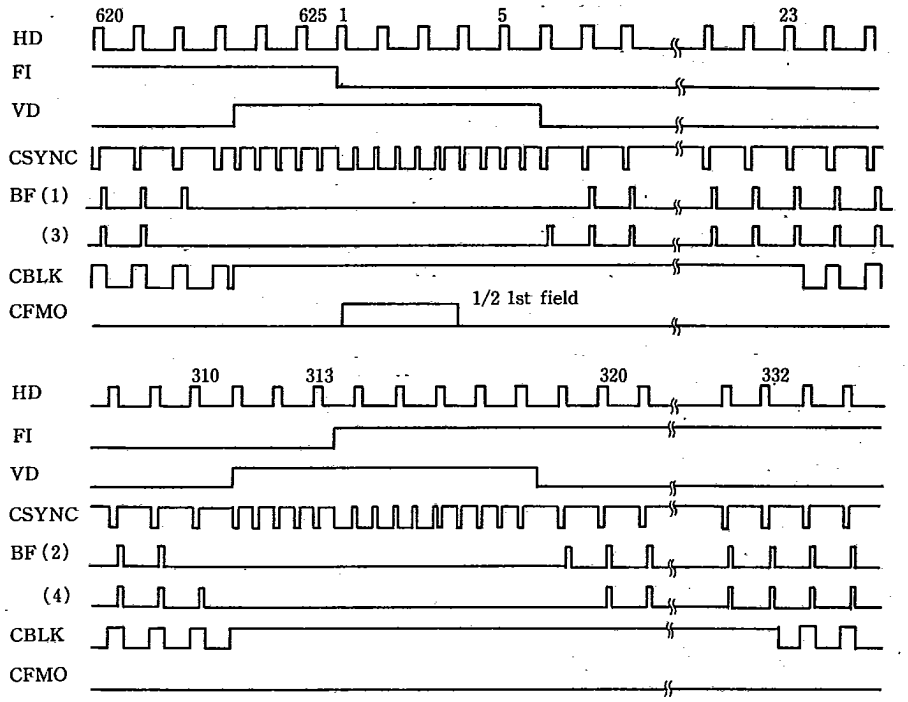


$x = 2.31$: 542 pixels (CKM_1 = "Low")
2.36 : 726 pixels (CKM_1 = "High")
$y = 2.94$: 542 pixels (CKM_1 = "Low")
2.91 : 726 pixels (CKM_1 = "High")

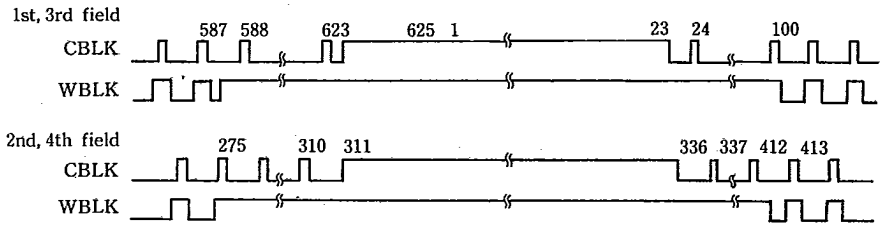
5

T-41-55

(4) PAL vertical timing

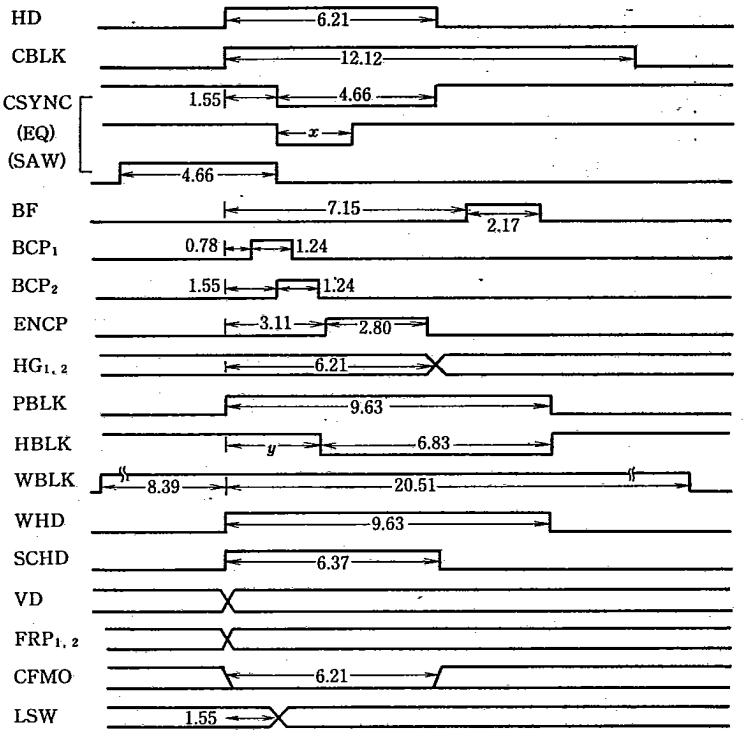


(5) PAL WBLK vertical timing



(6) PAL horizontal timing

(Unit : μs)



x = 2.28 : 512 pixels (CKM$_1$ = "Low")
2.33 : 680 pixels (CKM$_1$ = "High")

y = 2.90 : 512 pixels (CKM$_1$ = "Low")
2.87 : 680 pixels (CKM$_1$ = "High")

5