LZ92B31 Defect Compensator LSI for 2/3" CCD

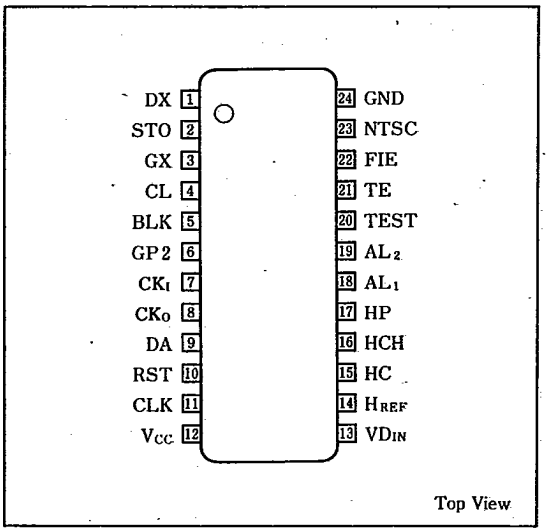
■ Description

The LZ92B31 is a defect compensator CMOS LSI controls the MB8541 defect compensation ROM and the LZ92E19 timing IC to compensate defects of pixels and provides 1/1218 dividing pulses.

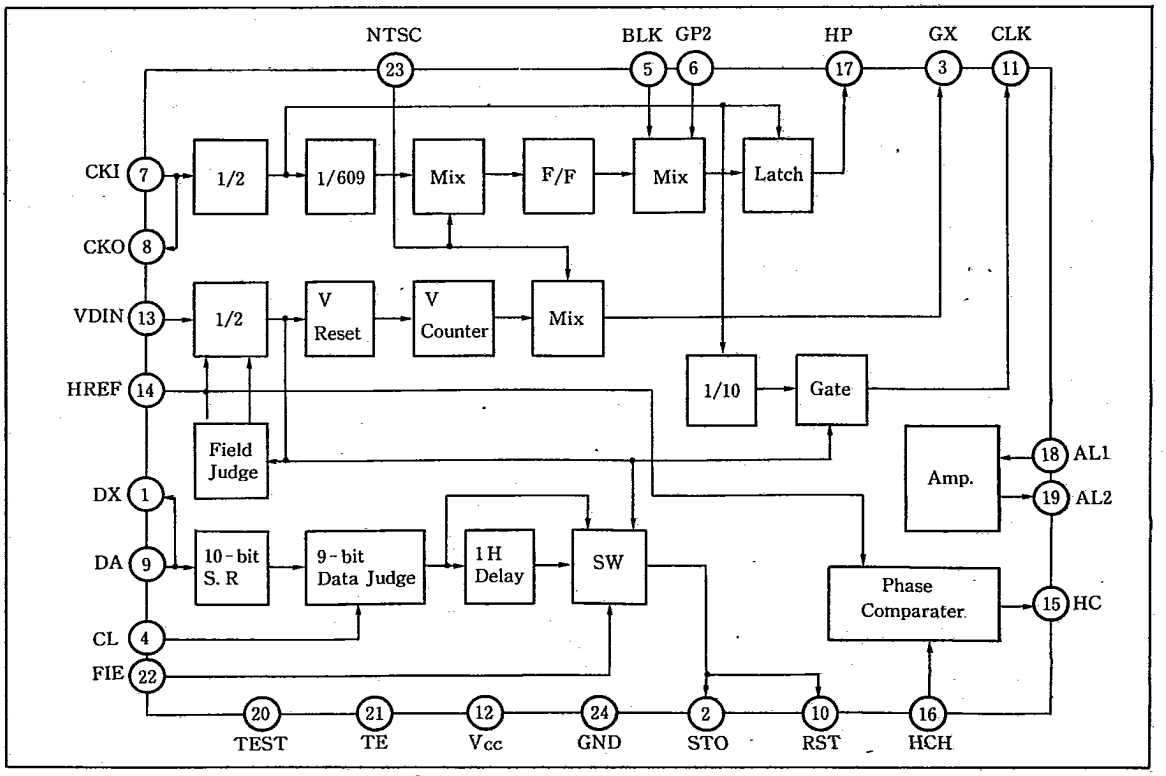
■ Features

1. 5V single power supply
2. Applicable to both field and frame integration modes
3. Built-in 1/1218 divider circuit
4. Built-in phase compensator
5. Built-in amplifier for PLL active low pass filter Gain : 20dB TYP.
6. 24-pin dual-in-line package

■ Pin Connections



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	7	V	1
Input voltage	V_I	−0.3 to V_{CC}+0.3	V	2
Output voltage	V_O	−0.3 to V_{CC}+0.3	V	
Operating temperature	T_{opr}	−10 to+70	℃	
Storage temperature	T_{stg}	−55 to+150	℃	

Note 1 : The maximum applicable valtage on V_{CC} pin with respect to GND.
Note 2 : The maximum applicable voltage on input pins excepting V_{CC} with respect to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	T_{opr}	−10		+70	℃

■ Electrical Characteristics

(V_{CC}=5V±10%, Ta=10 to+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V_{IL}				1.5	V	1
Input "High" voltage	V_{IH}		3.5			V	1
Output "Low" voltage	V_{OL}	I_{OL}=4mA			0.4	V	2
Output "High" voltage	V_{OH}	I_{OH}=−2mA	4.0			V	2
Input "High" current	$\lvert I_{IH} \rvert$	V_I=V_{CC}			10	μA	1
Input "Low" current	$\lvert I_{IL1} \rvert$	V_I=0V			10	μA	3
	$\lvert I_{IL2} \rvert$	V_I=0V	8		50	μA	4
Output leakage current	$\lvert I_{OZ} \rvert$	High impedance state			10	μA	5
Current consumption 1	I_{CC1}	V_{IN}=V_{CC} or GND			10	μA	
Current consumption 2	I_{CC2}	V_{IN}=V_{CC}, 0V, f=10MHz during pattern operation			30	mA	

(Current flowing into LSI is defined as positive.)

Note 1 : Applied to all input pins.
Note 2 : Applied to all output pins.
Note 3 : Applied to input pins CL, CK_I, VD_{IN}, H_{REF}, HCH and AL_1.
Note 4 : Applied to input pins BLK, GP_2, DA, TEST, TE, FIE and NTSC.
Note 5 : Applied to output pin HC.

Pin Functions

Pin No.	Symbol	I/O	Pin name	Description
1	DX	O	ROM data output	The DX pin outputs the address data for the position of a defective pixel which was input from the defect compensation ROM to the DA (pin 9). It is connected to the DX (pin 13) of the LZ92E19 timing IC.
2	ST_O	O	Strobe output	The ST_O pin outputs the synchronous pulse used to transfer the address data for the position of a defective pixel in the horizontal direction to the LZ92E19 timing IC, and outputs at 1H before the defect. It is connected to the ST_O (pin 14).
3	GX	O		The GX is a test pin.
4	CL	I	V counter clock	The CL pin inputs a V counter clock for defect compensation. It is connected to the CL (pin 36) of the LZ92E19 timing IC.
5	BLK	IU	Pre-blanking pulse	The BLK input pin controls the pulse width of the HP (pin 17). It is kept High or open and connected to the BLK (pin 42) of the LZ92E19 timing IC.
6	GP_2	I	Optical black clamp pulse 2	The GP_2 input pin controls the pulse width of the HP (pin 17). It is kept Low and connected to the GP_2 (pin 48) of the LZ92E19 timing IC.
7	CK_I	IB	Clock input	The CK_I pin inputs the reference clock. NTSC system : 19.164333MHz PAL system : 19.031250MHz
8	CK_O	OB	Clock output	The CK_O pin outputs a reference clock.
9	DA	IU	ROM data input	The DA pin inputs the address data for the position of a defective pixel from the defect compensation ROM.
10	RST	O	Restart pulse	The RST pin outputs a pulse to restart from the address 0 of the defect compensation ROM.
11	CLK	O	Clock pulse	The CLK pin outputs a clock pulse to read the address data for the position of a defective pixel at the horizontal and vertical directions from the defect compensation ROM.
12	V_{CC}	—	+5V power supply	The V_{CC} is a +5V power supply pin.
13	VD_{IN}	I	V reference input	The VD_{IN} pin inputs a vertical reference signal from SSG. NTSC system : LR3740N-VD LR3740-VD MN6064R-VP PAL system : MN6160PB-VP It inputs the above signals without changing the polarity. However, the MN system requires the level change.
14	H_{REF}	I	H reference input	The H_{REF} pin inputs a horizontal reference signal from SSG. NTSC system : LR3740N-WHD1 LR3740-HBL MN6064R-WHD PAL system : MN6160PB-WHD It inputs the HBL of the LR3740 with the polarity to be inverted, and the others without changing the polarity. However, the MN system requires the the level change.
15	HC	TO	Phase comparator output	The HC output pin is used to compare the phase of signals input to the HREF (pin 14) and HCH (pin 16). It outputs High level when the signal input to the HCH is in advanced phase, and Low level when the signal is in delayed phase. It goes into the high impedance state when both signals coincide with each other.
16	HCH	I	Comparator input	The HCH pin inputs the H signal of a phase comparator. It is connected to the HP (pin 17).
17	HP	O	H pulse	The HP pin outputs a 1/1218 dividing signal of a clock input to the CK_I (pin 7). It is connected to the HCH (pin 16) to compare with the H_{REF} (pin 14) in phase. It is connected to the HD_{IN} (pin 34) of the LZ92E19 timing IC.

Pin No.	Symbol	I/O	Pin name	Description
18	AL_1	IB	Amp. input	The AL_1 pin is used to input from the amplifier which comprises an active low pass filter for PLL.
19	AL_2	OB	Amp. output	The AL_2 pin is used to output to the amplifier which comprises an active low pass filter for PLL.
20	TEST	IU	Test	The TEST input pin is normally kept open or High.
21	TE	IU	Test	The TE input pin is normally kept open or High.
22	FIE	IU	Field/Frame selection	The FIE input pin controls the number of H line for the defect compensation according to the integration mode of the LZ22250G and the LZ22251 CCD area sensor. Field integration : it is kept High or open. Frame integration : it is kept Low.
23	NTSC	IU	NTSC/PAL selection	The NTSC input pin selects the TV system. NTSC system : it is kept High or open. PAL system : it is kept Low.
24	GND	—	Ground	The GND is a ground pin.

* A proper defect compensation ROM must be selected according to the integration mode of CCD.

I : Input pin
IU : Input pin with a pull-up resistor
IB : Input pin for oscillator
O : Output pin
OB : Output pin for oscillator
TO : Tri-state output pin

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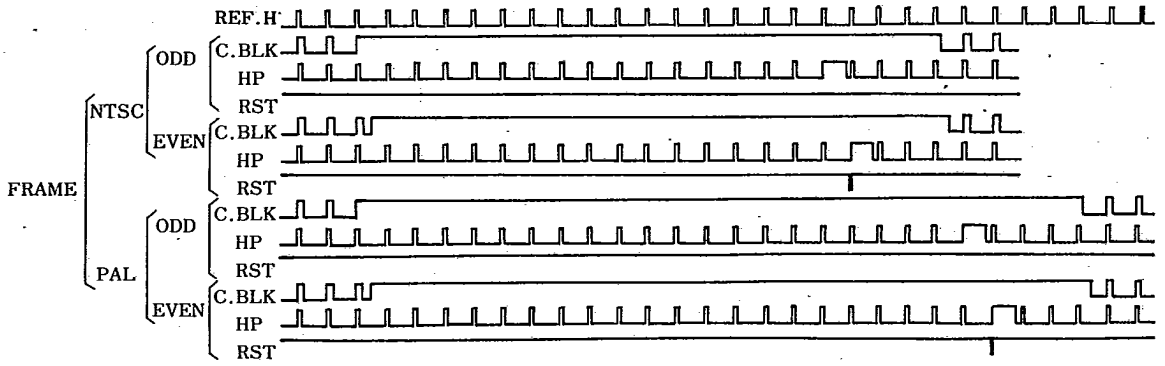
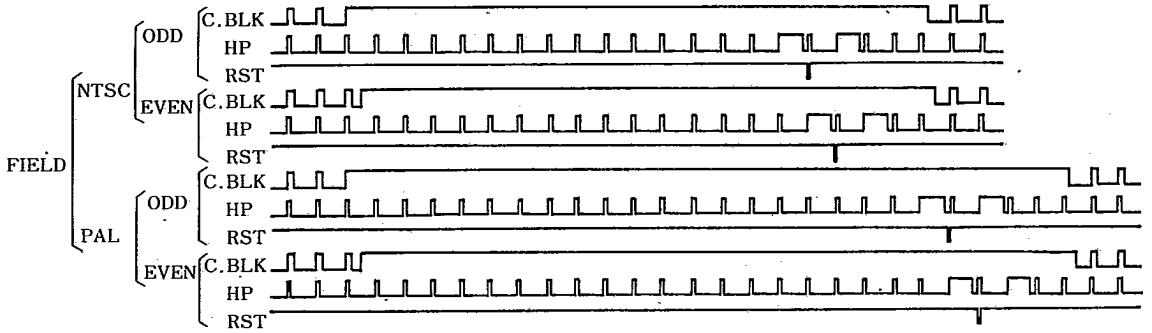
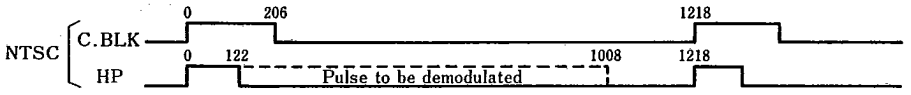
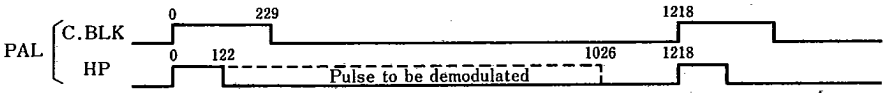
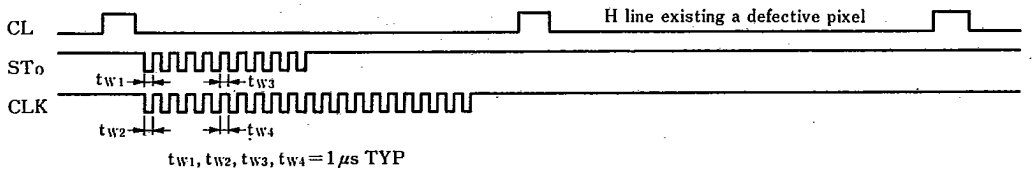
■ Timing Diagram











■ Application Circuit Example (Complementary color video camera for NTSC TV system with field integration mode)