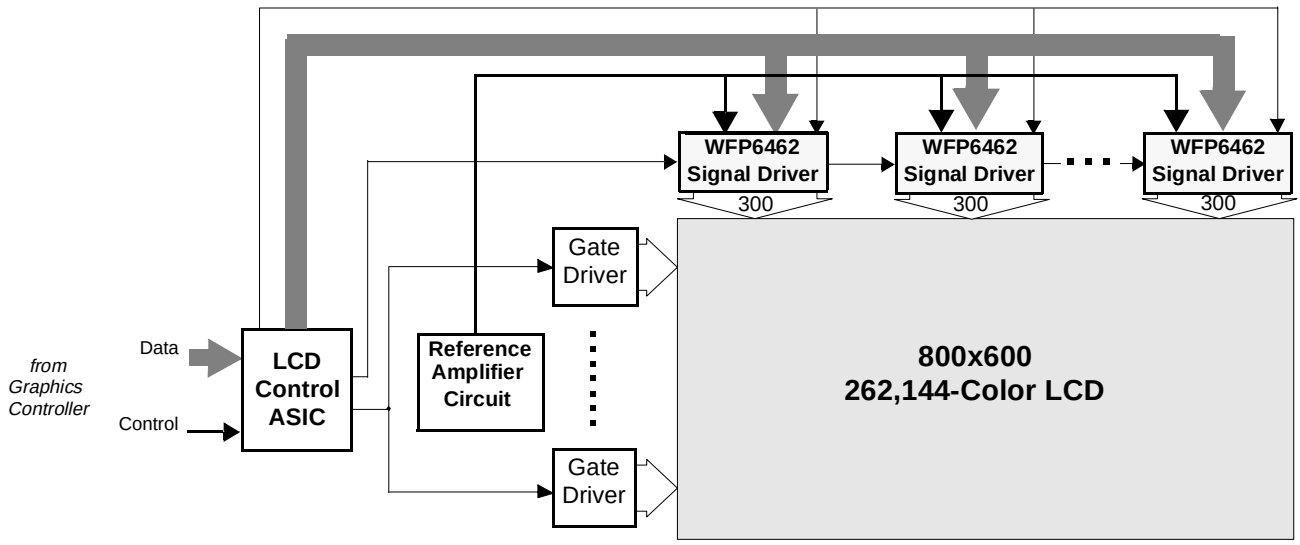
1. PRODUCT DESCRIPTION

Signal Driver

300-Channel, 6-Bit Dot Inversion Driver for TFT-LCD Applications

The WFP6462 is a 6-bit, 300-channel signal driver designed for low power SVGA TFT-LCD panel applications. The WFP6462 accepts 2 sets of reference voltages EV0..EV8 and OV0..OV8. Channels V_{S2n} use EV0..EV8, and channels V_{S2n-1} use OV0..OV8 (n = 1..150). This allows column or dot inversion to be easily implemented in single bank applications.

The WFP6462's internal architecture provides separate resistor-string DACs for both the odd and even channels. The value of the individual resistor segments is weighted to reduce signal driver power dissipation by as much as 20% to 60% when compared to non-weighted resistor string DAC architectures.



2. FEATURES & BENEFITS

Features	Benefits
• Weighted R-String: See Figure 2-1 & Table 2-1	• Reduces Power Dissipation 20-60% or more. • Reduces dc current drive requirements of external reference amplifiers
• Low-power operation • Logic Supply: 2.5 or 3.3 Volts • Analog Supply: 3.3±0.3 to 5.0±0.5 Volts	• Extends battery-based operation • Low power and EMI from 3.3 V operation • Minimum dynamic-power dissipation
• High Speed Operation • 65 MHz (3.3 Volt logic supply) • 45 MHz (2.5 Volt logic supply)	• Support for wide range of color LCD resolutions • Reduce EMI & power dissipation in SVGA systems
• Data Inversion Feature	• Data inversion capability enables a complete internal solution for Vcom modulation by data inversion. • Can reduce data transitions for lower EMI & power
• Full Color Display	• 64 gray scales per primary color • 262,144 (256K) color palette
• Excellent Output Uniformity	• Output Error = 0.15 LSB (12 mV @5V, 8 mV @3V)

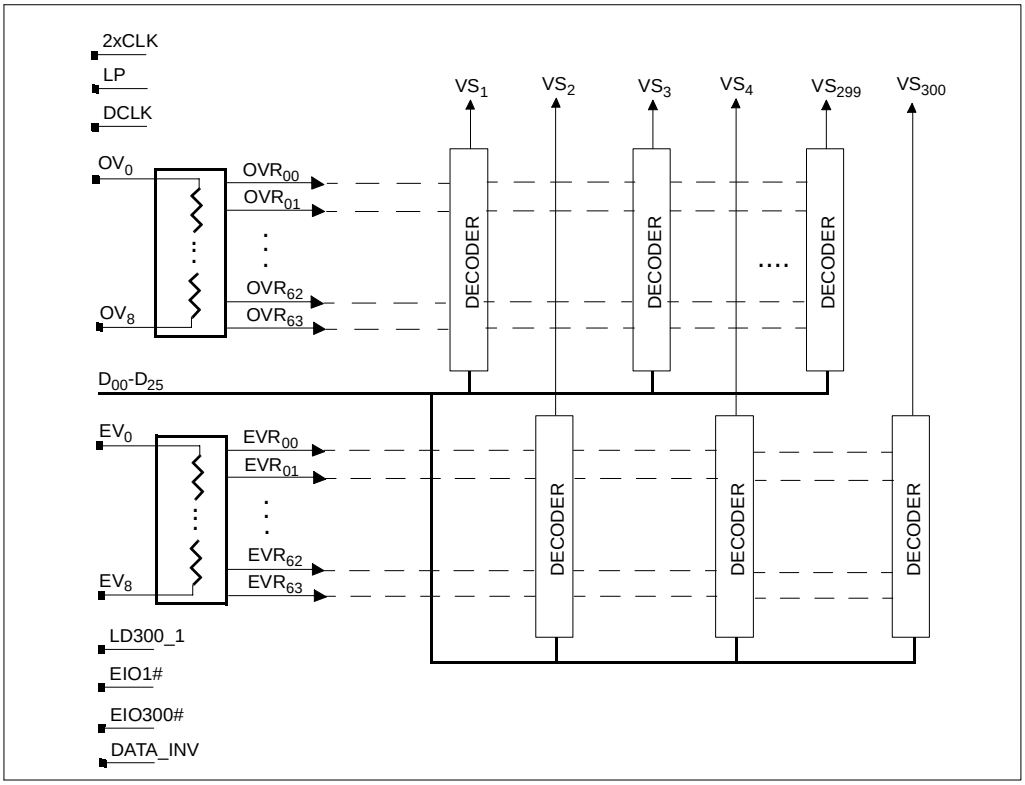


Figure 2-1: Block Diagram

- Internal weighted R-String for low power operation (see Table 2-1 and Figure 2-1).

Table 2-1: Weighted R_{SEG} Values for WFP6462 (ignoring bus resistance)

R-Segment	Value
EV_7~EV_8, OV_7~OV_8	51Ω,51Ω,51Ω,51Ω,51Ω,51Ω,102Ω,204Ω
EV_6~EV_7, OV_6~OV_7	38 Ω X 8
EV_5~EV_6, OV_5~OV_6	32 Ω X 8
EV_4~EV_5, OV_4~OV_5	32 Ω X 8
EV_3~EV_4, OV_3~OV_4	32 Ω X 8
EV_2~EV_3, OV_2~OV_3	32 Ω X 8
EV_1~EV_2, OV_1~OV_2	38 Ω X 8
EV_0~EV_1, OV_0~OV_1	204Ω,102Ω,51Ω,51Ω,51Ω,51Ω,51Ω

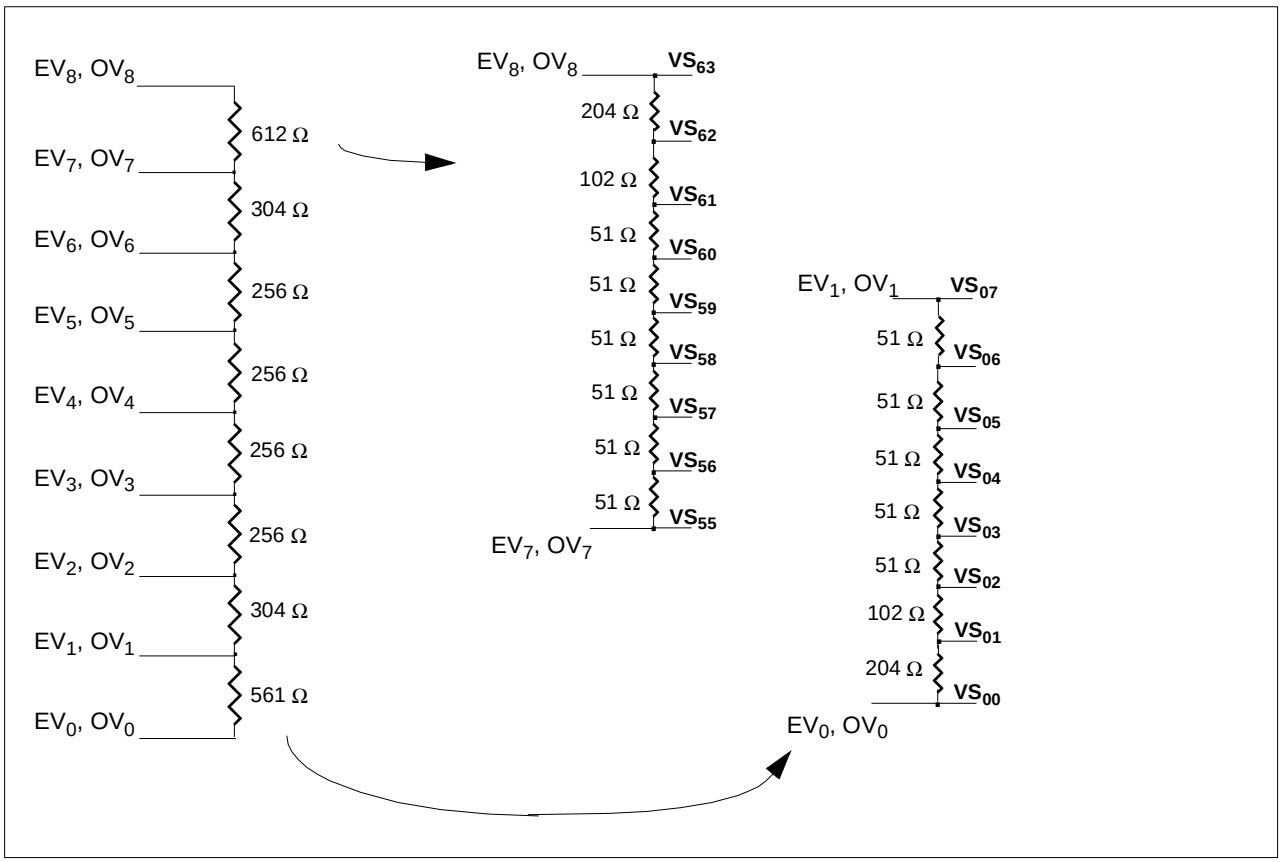


Figure 2-2: R-String Detail

2.1. Low SVGA Power Dissipation

The WFP6462 provides a very low power dissipation solution of < 300 mW for module electronics (not including backlight power) for an all black image.

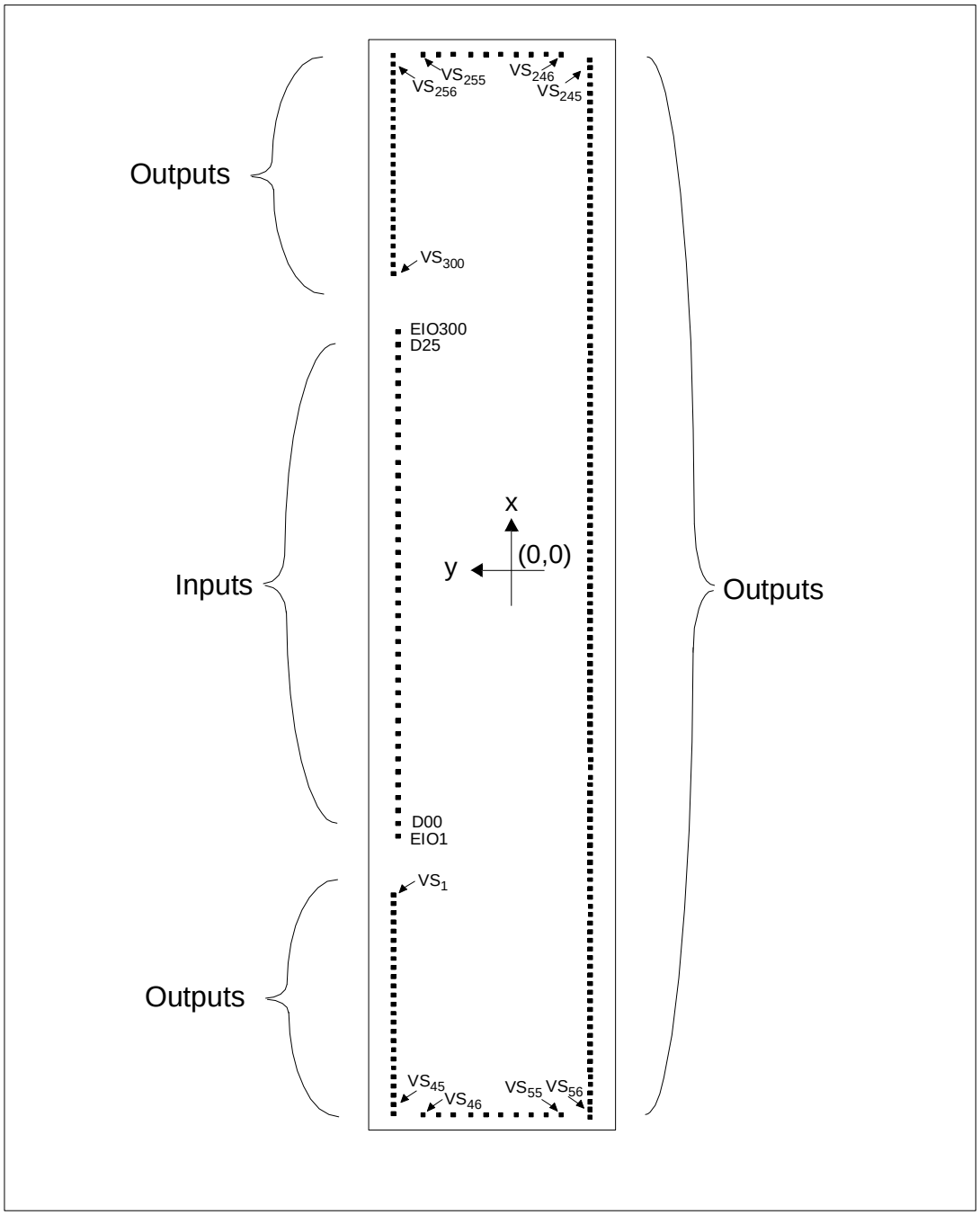
Table 2-2 shows the power dissipation for a typical SVGA system consisting of 8 WFP6462's and 2 CL-FP6131's (to provide 18 voltage references). 60 Hz polarity inversion is assumed, resulting in negligible power dissipation for charging and discharging the panel capacitance.

Table 2–2.

Dissipation Term	mW
due to Amplifier IDDA: 18 x 400 uA x 5.0V	36
due to Amplifier headrooms x load currents	37
due to WFP6462 R-String	28
due to WFP6462 IDDD (active + standby)	30
Charge Digital Lines & DCLK	43
TCON ASIC: 30 mA x 3.3V	100
Total	274

3. DIE DIAGRAM & PAD COORDINATES

3.1. DIE DIAGRAM



3.2. Input Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
1	EIO300#	2649.0	583.30
2	D25	2529.2	583.30
3	D24	2429.2	583.30
4	D23	2329.2	583.30
5	2xCLK	2229.2	583.30
6	DCLK	2129.2	583.30
7	LD300_1	2029.2	583.30
8	OV0	1909.4	583.30
9	OV8	1809.4	583.30
10	EV8	1709.4	583.30
11	EV0	1609.4	583.30
12	D22	1489.6	583.30
13	D21	1389.6	583.30
14	D20	1289.6	583.30
15	D15	1189.6	583.30
16	D14	1089.6	583.30
17	D13	989.6	583.30
18	VDDD	869.8	583.30
19	VDDA	769.8	583.30
20	EV1	650.0	583.30
21	EV7	550.0	583.30
22	EV3	450.0	583.30
23	EV5	350.0	583.30
24	EV6	250.0	583.30
25	EV4	150.0	583.30
26	EV2	50.0	583.30
27	OV2	-50.0	583.30
28	OV4	-150.0	583.30
29	OV6	-250.0	583.30
30	OV5	-350.0	583.30
31	OV3	-450.0	583.30
32	OV7	-550.0	583.30
33	OV1	-650.0	583.30
34	AGND	-769.8	583.30
35	DGND	-869.8	583.30
36	D12	-989.6	583.30
37	D11	-1089.6	583.30
38	D10	-1189.6	583.30
39	D05	-1289.6	583.30
40	D04	-1389.6	583.30
41	DATA_INV	-1489.6	583.30
42	EV0	-1609.4	583.30
43	EV8	-1709.4	583.30
44	OV8	-1809.4	583.30
45	OV0	-1909.4	583.30
46	LP	-2029.2	583.30
47	D03	-2129.2	583.30
48	D02	-2229.2	583.30
49	D01	-2329.2	583.30
50	D00	-2429.2	583.30
51	EIO1#	-2549.0	583.30

Table 3–1. Input bond Pad Coordinates

3.3. Output Bond Pad Coordinates

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
52	VS1	-3030.0	594.1
53	VS2	-3090.0	594.1
54	VS3	-3150.0	594.1
55	VS4	-3210.0	594.1
56	VS5	-3270.0	594.1
57	VS6	-3330.0	594.1
58	VS7	-3390.0	594.1
59	VS8	-3450.0	594.1
60	VS9	-3510.0	594.1
61	VS10	-3570.0	594.1
62	VS11	-3630.0	594.1
63	VS12	-3690.0	594.1
64	VS13	-3750.0	594.1
65	VS14	-3810.0	594.1
66	VS15	-3870.0	594.1
67	VS16	-3930.0	594.1
68	VS17	-3990.0	594.1
69	VS18	-4050.0	594.1
70	VS19	-4110.0	594.1
71	VS20	-4170.0	594.1
72	VS21	-4230.0	594.1
73	VS22	-4290.0	594.1
74	VS23	-4350.0	594.1
75	VS24	-4410.0	594.1
76	VS25	-4470.0	594.1
77	VS26	-4530.0	594.1
78	VS27	-4590.0	594.1
79	VS28	-4650.0	594.1
80	VS29	-4710.0	594.1
81	VS30	-4770.0	594.1
82	VS31	-4830.0	594.1
83	VS32	-4890.0	594.1
84	VS33	-4950.0	594.1
85	VS34	-5010.0	594.1
86	VS35	-5070.0	594.1
87	VS36	-5130.0	594.1
88	VS37	-5190.0	594.1
89	VS38	-5250.0	594.1
90	VS39	-5310.0	594.1
91	VS40	-5370.0	594.1
92	VS41	-5430.0	594.1
93	VS42	-5490.0	594.1
94	VS43	-5550.0	594.1
95	VS44	-5610.0	594.1
96	VS45	-5670.0	594.1
97	dummy	-5743.0	598.1
98	VS46	-5739.1	409.5
99	VS47	-5739.1	318.5
100	VS48	-5739.1	227.5
101	VS49	-5739.1	136.5
102	VS50	-5739.1	45.5
103	VS51	-5739.1	-45.5

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
104	VS52	-5739.1	-136.5
105	VS53	-5739.1	-227.5
106	VS54	-5739.1	-318.5
107	VS55	-5739.1	-409.5
108	dummy	-5743.0	-598.1
109	VS56	-5670.0	-594.1
110	VS57	-5610.0	-594.1
111	VS58	-5550.0	-594.1
112	VS59	-5490.0	-594.1
113	VS60	-5430.0	-594.1
114	VS61	-5370.0	-594.1
115	VS62	-5310.0	-594.1
116	VS63	-5250.0	-594.1
117	VS64	-5190.0	-594.1
118	VS65	-5130.0	-594.1
119	VS66	-5070.0	-594.1
120	VS67	-5010.0	-594.1
121	VS68	-4950.0	-594.1
122	VS69	-4890.0	-594.1
123	VS70	-4830.0	-594.1
124	VS71	-4770.0	-594.1
125	VS72	-4710.0	-594.1
126	VS73	-4650.0	-594.1
127	VS74	-4590.0	-594.1
128	VS75	-4530.0	-594.1
129	VS76	-4470.0	-594.1
130	VS77	-4410.0	-594.1
131	VS78	-4350.0	-594.1
132	VS79	-4290.0	-594.1
133	VS80	-4230.0	-594.1
134	VS81	-4170.0	-594.1
135	VS82	-4110.0	-594.1
136	VS83	-4050.0	-594.1
137	VS84	-3990.0	-594.1
138	VS85	-3930.0	-594.1
139	VS86	-3870.0	-594.1
140	VS87	-3810.0	-594.1
141	VS88	-3750.0	-594.1
142	VS89	-3690.0	-594.1
143	VS90	-3630.0	-594.1
144	VS91	-3570.0	-594.1
145	VS92	-3510.0	-594.1
146	VS93	-3450.0	-594.1
147	VS94	-3390.0	-594.1
148	VS95	-3330.0	-594.1
149	VS96	-3270.0	-594.1
150	VS97	-3210.0	-594.1
151	VS98	-3150.0	-594.1
152	VS99	-3090.0	-594.1
153	VS100	-3030.0	-594.1
154	VS101	-2970.0	-594.1
155	VS102	-2910.0	-594.1
156	VS103	-2850.0	-594.1
157	VS104	-2790.0	-594.1
158	VS105	-2730.0	-594.1

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
159	VS106	-2670.0	-594.1
160	VS107	-2610.0	-594.1
161	VS108	-2550.0	-594.1
162	VS109	-2490.0	-594.1
163	VS110	-2430.0	-594.1
164	VS111	-2370.0	-594.1
165	VS112	-2310.0	-594.1
166	VS113	-2250.0	-594.1
167	VS114	-2190.0	-594.1
168	VS115	-2130.0	-594.1
169	VS116	-2070.0	-594.1
170	VS117	-2010.0	-594.1
171	VS118	-1950.0	-594.1
172	VS119	-1890.0	-594.1
173	VS120	-1830.0	-594.1
174	VS121	-1770.0	-594.1
175	VS122	-1710.0	-594.1
176	VS123	-1650.0	-594.1
177	VS124	-1590.0	-594.1
178	VS125	-1530.0	-594.1
179	VS126	-1470.0	-594.1
180	VS127	-1410.0	-594.1
181	VS128	-1350.0	-594.1
182	VS129	-1290.0	-594.1
183	VS130	-1230.0	-594.1
184	VS131	-1170.0	-594.1
185	VS132	-1110.0	-594.1
186	VS133	-1050.0	-594.1
187	VS134	-990.0	-594.1
188	VS135	-930.0	-594.1
189	VS136	-870.0	-594.1
190	VS137	-810.0	-594.1
191	VS138	-750.0	-594.1
192	VS139	-690.0	-594.1
193	VS140	-630.0	-594.1
194	VS141	-570.0	-594.1
195	VS142	-510.0	-594.1
196	VS143	-450.0	-594.1
197	VS144	-390.0	-594.1
198	VS145	-330.0	-594.1
199	VS146	-270.0	-594.1
200	VS147	-210.0	-594.1
201	VS148	-150.0	-594.1
202	VS149	-90.0	-594.1
203	VS150	-30.0	-594.1
204	VS151	30.0	-594.1
205	VS152	90.0	-594.1
206	VS153	150.0	-594.1
207	VS154	210.0	-594.1
208	VS155	270.0	-594.1
209	VS156	330.0	-594.1
210	VS157	390.0	-594.1
211	VS158	450.0	-594.1
212	VS159	510.0	-594.1
213	VS160	570.0	-594.1

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
214	VS161	630.0	-594.1
215	VS162	690.0	-594.1
216	VS163	750.0	-594.1
217	VS164	810.0	-594.1
218	VS165	870.0	-594.1
219	VS166	930.0	-594.1
220	VS167	990.0	-594.1
221	VS168	1050.0	-594.1
222	VS169	1110.0	-594.1
223	VS170	1170.0	-594.1
224	VS171	1230.0	-594.1
225	VS172	1290.0	-594.1
226	VS173	1350.0	-594.1
227	VS174	1410.0	-594.1
228	VS175	1470.0	-594.1
229	VS176	1530.0	-594.1
230	VS177	1590.0	-594.1
231	VS178	1650.0	-594.1
232	VS179	1710.0	-594.1
233	VS180	1770.0	-594.1
234	VS181	1830.0	-594.1
235	VS182	1890.0	-594.1
236	VS183	1950.0	-594.1
237	VS184	2010.0	-594.1
238	VS185	2070.0	-594.1
239	VS186	2130.0	-594.1
240	VS187	2190.0	-594.1
241	VS188	2250.0	-594.1
242	VS189	2310.0	-594.1
243	VS190	2370.0	-594.1
244	VS191	2430.0	-594.1
245	VS192	2490.0	-594.1
246	VS193	2550.0	-594.1
247	VS194	2610.0	-594.1
248	VS195	2670.0	-594.1
249	VS196	2730.0	-594.1
250	VS197	2790.0	-594.1
251	VS198	2850.0	-594.1
252	VS199	2910.0	-594.1
253	VS200	2970.0	-594.1
254	VS201	3030.0	-594.1
255	VS202	3090.0	-594.1
256	VS203	3150.0	-594.1
257	VS204	3210.0	-594.1
258	VS205	3270.0	-594.1
259	VS206	3330.0	-594.1
260	VS207	3390.0	-594.1
261	VS208	3450.0	-594.1
262	VS209	3510.0	-594.1
263	VS210	3570.0	-594.1
264	VS211	3630.0	-594.1
265	VS212	3690.0	-594.1
266	VS213	3750.0	-594.1
267	VS214	3810.0	-594.1
268	VS215	3870.0	-594.1

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
269	VS216	3930.0	-594.1
270	VS217	3990.0	-594.1
271	VS218	4050.0	-594.1
272	VS219	4110.0	-594.1
273	VS220	4170.0	-594.1
274	VS221	4230.0	-594.1
275	VS222	4290.0	-594.1
276	VS223	4350.0	-594.1
277	VS224	4410.0	-594.1
278	VS225	4470.0	-594.1
279	VS226	4530.0	-594.1
280	VS227	4590.0	-594.1
281	VS228	4650.0	-594.1
282	VS229	4710.0	-594.1
283	VS230	4770.0	-594.1
284	VS231	4830.0	-594.1
285	VS232	4890.0	-594.1
286	VS233	4950.0	-594.1
287	VS234	5010.0	-594.1
288	VS235	5070.0	-594.1
289	VS236	5130.0	-594.1
290	VS237	5190.0	-594.1
291	VS238	5250.0	-594.1
292	VS239	5310.0	-594.1
293	VS240	5370.0	-594.1
294	VS241	5430.0	-594.1
295	VS242	5490.0	-594.1
296	VS243	5550.0	-594.1
297	VS244	5610.0	-594.1
298	VS245	5670.0	-594.1
299	dummy	5743.0	-598.1
300	VS246	5739.1	-409.5
301	VS247	5739.1	-318.5
302	VS248	5739.1	-227.5
303	VS249	5739.1	-136.5
304	VS250	5739.1	-45.5
305	VS251	5739.1	45.5
306	VS252	5739.1	136.5
307	VS253	5739.1	227.5
308	VS254	5739.1	318.5
309	VS255	5739.1	409.5
310	dummy	5743.0	598.1
311	VS256	5670.0	594.1
312	VS257	5610.0	594.1
313	VS258	5550.0	594.1
314	VS259	5490.0	594.1
315	VS260	5430.0	594.1
316	VS261	5370.0	594.1
317	VS262	5310.0	594.1
318	VS263	5250.0	594.1
319	VS264	5190.0	594.1
320	VS265	5130.0	594.1
321	VS266	5070.0	594.1
322	VS267	5010.0	594.1
323	VS268	4950.0	594.1

Table 3–2. Output Bond Pad Coordinates

Pad #	Signal	X (um)	Y (um)
324	VS269	4890.0	594.1
325	VS270	4830.0	594.1
326	VS271	4770.0	594.1
327	VS272	4710.0	594.1
328	VS273	4650.0	594.1
329	VS274	4590.0	594.1
330	VS275	4530.0	594.1
331	VS276	4470.0	594.1
332	VS277	4410.0	594.1
333	VS278	4350.0	594.1
334	VS279	4290.0	594.1
335	VS280	4230.0	594.1
336	VS281	4170.0	594.1
337	VS282	4110.0	594.1
338	VS283	4050.0	594.1
339	VS284	3990.0	594.1
340	VS285	3930.0	594.1
341	VS286	3870.0	594.1
342	VS287	3810.0	594.1
343	VS288	3750.0	594.1
344	VS289	3690.0	594.1
345	VS290	3630.0	594.1
346	VS291	3570.0	594.1
347	VS292	3510.0	594.1
348	VS293	3450.0	594.1
349	VS294	3390.0	594.1
350	VS295	3330.0	594.1
351	VS296	3270.0	594.1
352	VS297	3210.0	594.1
353	VS298	3150.0	594.1
354	VS299	3090.0	594.1
355	VS300	3030.0	594.1

4. DETAILED PAD DESCRIPTIONS

The following abbreviations are used for pad types in the following sections: (I) input; (O) output; (I/O) Input/Output, (#) active 'low' signal.

Name	Pad #	Type	Description
LD300_1	7	I	**LOAD DIRECTION:** Controls the direction in which the data is loaded into the Input Register: When LD300_1 = '0', data is loaded from Channel V_{S1} to V_{S300}. When LD300_1 = '1', data is loaded from Channel V_{S300} to V_{S1}.
EIO1#, EIO300#	51,1	I/O	**ENABLE IN/OUT**: The EIO1# and EIO300# active 'low' signals initiate the loading of data into the Input Register of the WFP6462. When one of the EIOx# 's is configured as an input, the other is configured as an output, with the direction determined by the LD300_1 input (see Table 4-1). The EIOx# outputs are designed to be connected to the EIOx# inputs of adjacent devices to allow a series of drivers to operate sequentially. When a 'low' is applied to the EIOx# pin configured as an input on the first device in the series, data is loaded from the three sets of 6-bit Data Inputs into the first three 6-bit Input-Register locations. On subsequent transitions of the DCLK, data continues to be loaded into the remaining 6-bit Input-Register locations. When the register is full (300 words), the EIOx# pin configured as an output goes 'low', enabling the next driver. The data load sequence is summarized in Table 4-1, Figure 4-1 and Figure 4-2.

Table 4-1: Input/Output Selection for EIO1# and EIO300#

LD300_1 Input	EIO1#, EIO300# Functionality		Data Loading Sequence
	EIO1#	EIO300#	
'0'	Input	Output	Channel 1 to 300
'1'	Output	Input	Channel 300 to 1

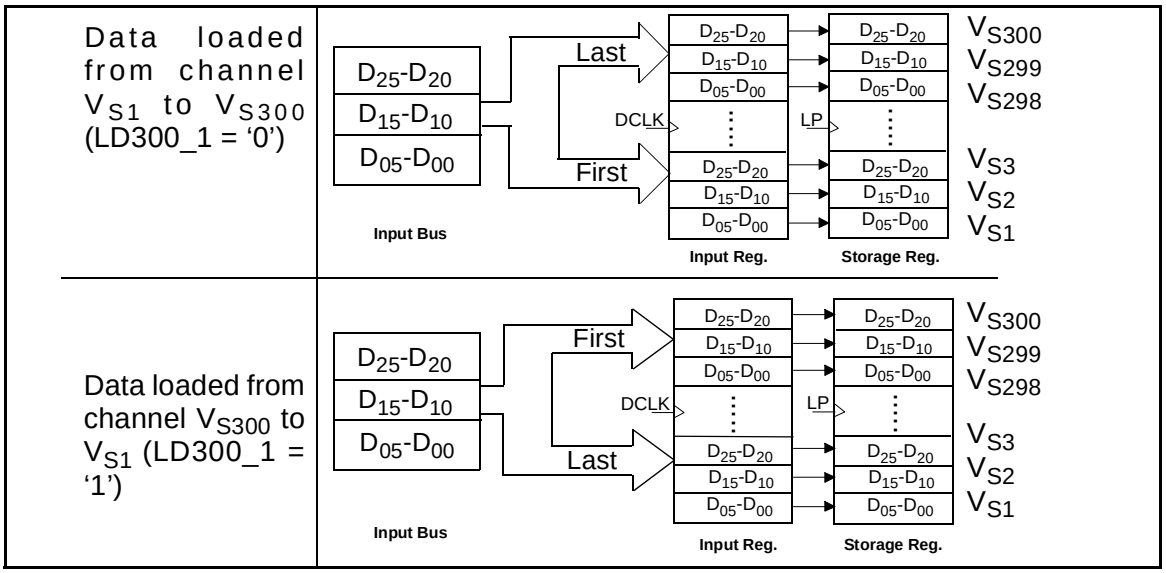


Figure 4–1. Display Data Sampling and Output Direction

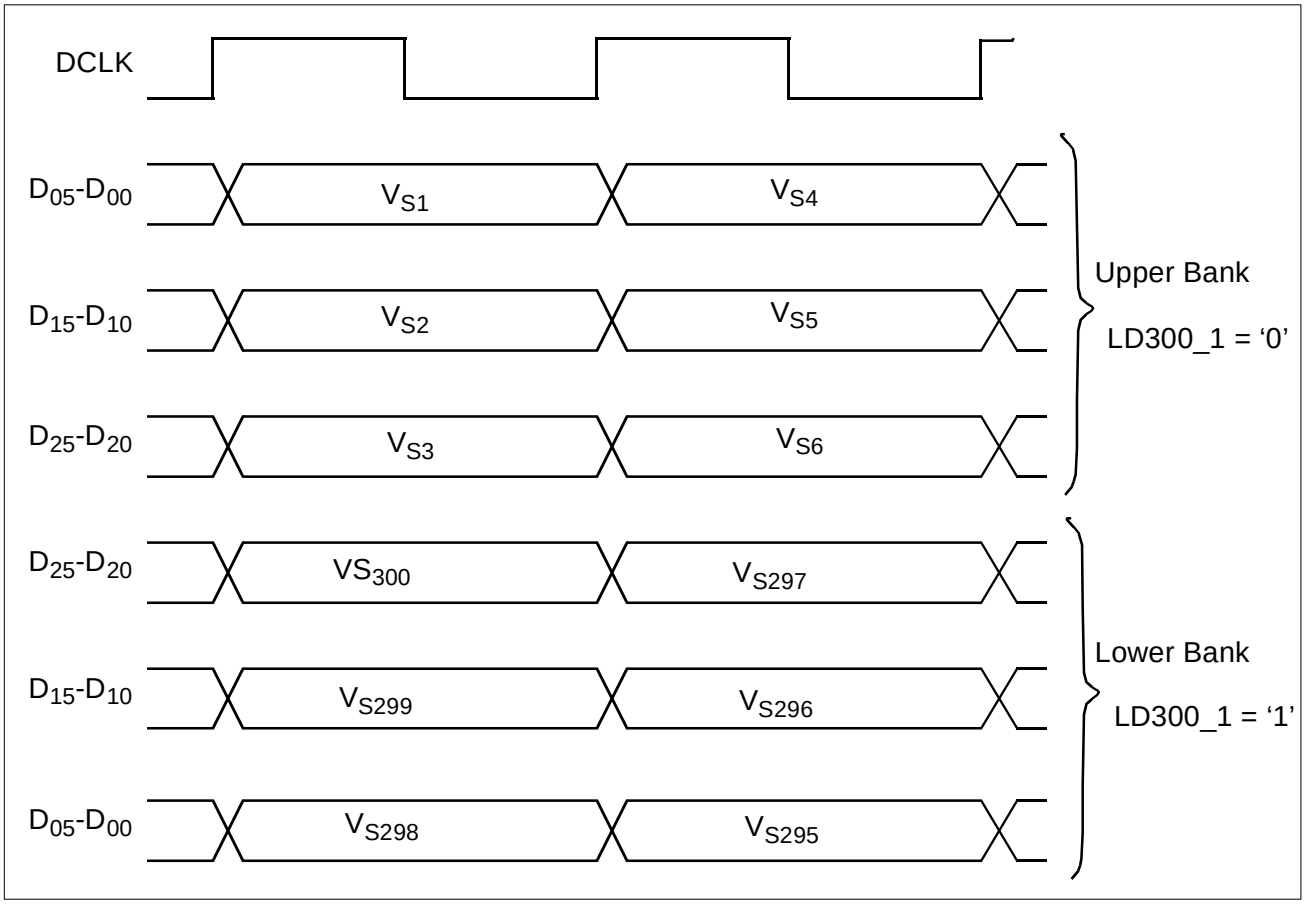


Figure 4–2. Display Data Channel Assignment and Output Sequence

Name	Pad #	Type	Description (*Cont.*)
V_{S1}-V_{S300}	see Table 3-2	O	**VOLTAGE OUTPUTS**: These outputs drive all 300 pixel inputs of the LCD simultaneously after the high-to-low transition of LP. **Outputs are high impedance while LP is high**.
D_{05}-D_{00} D_{15}-D_{10} D_{25}-D_{20}	39,40,47-50 15-17,36-38 2-4,12-14	I	**DATA**: The Data inputs consist of 6-bit words for each of three channels. At the falling edge of DCLK, three 6-bit words for three adjacent channels are loaded in parallel. Each data bit is represented as Dij where: i = 2-0 indicates the channel j = 5-0 indicates the significance of the bit in each word. D_{i5} indicates the MSB and D_{i0} indicates the LSB of the input word.
LP	46	I	**Latch Pulse**: When LP is driven high, the data is transferred from the Input Register into the Storage Register, and the selected analog voltages drive the LCD. Also, the EIOx# output is reset to the 'high' level.
DCLK	6	I	**DATA CLOCK**: Data is loaded into the input registers on the high-to-low transition of DCLK for 2xCLK= low and on both rising and falling edges of the DCLK input for 2xCLK = high.
OV_8 OV_7 OV_6 OV_5 OV_4 OV_3 OV_2 OV_1 OV_0	9,44 32 29 30 28 31 27 33 8,45	I	**ODD REFERENCE VOLTAGE INPUTS:** These 9 inputs supply the reference voltage inputs to the r-string DAC for the odd channels VS_1, VS_3, ..VS_{299} Note: both OV_8 inputs must be connected to each other and to the same potential; also, both OV_0 inputs must be . connected to each other and to the same potential
EV_8 EV_7 EV_6 EV_5 EV_4 EV_3 EV_2 EV_1 EV_0	10,43 21 24 23 25 22 26 20 11,42	I	**EVEN REFERENCE VOLTAGE INPUTS:** These 9 inputs supply the reference voltage inputs to the r-string DAC for the even channels VS_2, VS_4, ..VS_{300} Note: both EV_8 inputs must be connected to each other and to the same potential; also, both EV_0 inputs must be . connected to each other and to the same potential
V_{DDD}	18	I	**DIGITAL SUPPLY VOLTAGE**: 2.5 V ± 0.2 or 3.3 V ± 0.3 should be provided on this pin to supply digital power to the device.
V_{DDA}	19	I	**ANALOG SUPPLY VOLTAGE**: Up to 5.5 V should be provided on this pin to supply analog power to the device. **Also, must have V_{DDA} >= V_{DDD}.**

Name	Pad#	Type	Description (*Cont.*)
AGND	34	I	**ANALOG GROUND**
DGND	35	I	**DIGITAL GROUND**
DATA_INV	41	I	**DATA INVERSION**: The data inversion input signal, when logic high, enables inversion of the input display data (D_{ij}). This pad should be tied “low” or allowed to float if data inversion is not used. This signal may also be used in coordination with the control ASIC to reduce data transitions.
2xCLK	5	I	**2xCLK**: When logic high, the 2xCLK input enables sampling of input display data (D_{ij}) on both rising and falling edges of the DCLK input (see Figure 5-2). When logic low, input display data is sampled on the falling edge of DCLK only (see Figure 5-1).

Table 4-2: Input Data vs. Output Voltage

MSB	Display Data					LSB	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0		$V_n = EV_n$ or OV_n
0	0	0	0	0	0		V_0
0	0	0	0	0	1		$V_0 + 204/561 \times (V_1 - V_0)$
0	0	0	0	1	0		$V_0 + 306/561 \times (V_1 - V_0)$
0	0	0	0	1	1		$V_0 + 357/561 \times (V_1 - V_0)$
0	0	0	1	0	0		$V_0 + 408/561 \times (V_1 - V_0)$
0	0	0	1	0	1		$V_0 + 459/561 \times (V_1 - V_0)$
0	0	0	1	1	0		$V_0 + 510/561 \times (V_1 - V_0)$
0	0	0	1	1	1		V_1
0	0	1	0	0	0		$V_1 + 1/8 \times (V_2 - V_1)$
0	0	1	0	0	1		$V_1 + 2/8 \times (V_2 - V_1)$
0	0	1	0	1	0		$V_1 + 3/8 \times (V_2 - V_1)$
0	0	1	0	1	1		$V_1 + 4/8 \times (V_2 - V_1)$
0	0	1	1	0	0		$V_1 + 5/8 \times (V_2 - V_1)$
0	0	1	1	0	1		$V_1 + 6/8 \times (V_2 - V_1)$
0	0	1	1	1	0		$V_1 + 7/8 \times (V_2 - V_1)$
0	0	1	1	1	1		V_2
0	1	0	0	0	0		$V_2 + 1/8 \times (V_3 - V_2)$
0	1	0	0	0	1		$V_2 + 2/8 \times (V_3 - V_2)$
0	1	0	0	1	0		$V_2 + 3/8 \times (V_3 - V_2)$
0	1	0	0	1	1		$V_2 + 4/8 \times (V_3 - V_2)$
0	1	0	1	0	0		$V_2 + 5/8 \times (V_3 - V_2)$
0	1	0	1	0	1		$V_2 + 6/8 \times (V_3 - V_2)$
0	1	0	1	1	0		$V_2 + 7/8 \times (V_3 - V_2)$
0	1	0	1	1	1		V_3
0	1	1	0	0	0		$V_3 + 1/8 \times (V_4 - V_3)$
0	1	1	0	0	1		$V_3 + 2/8 \times (V_4 - V_3)$
0	1	1	0	1	0		$V_3 + 3/8 \times (V_4 - V_3)$
0	1	1	0	1	1		$V_3 + 4/8 \times (V_4 - V_3)$
0	1	1	1	0	0		$V_3 + 5/8 \times (V_4 - V_3)$
0	1	1	1	0	1		$V_3 + 6/8 \times (V_4 - V_3)$
0	1	1	1	1	0		$V_3 + 7/8 \times (V_4 - V_3)$
0	1	1	1	1	1		V_4
1	0	0	0	0	0		$V_4 + 1/8 \times (V_5 - V_4)$
1	0	0	0	0	1		$V_4 + 2/8 \times (V_5 - V_4)$
1	0	0	0	1	0		$V_4 + 3/8 \times (V_5 - V_4)$
1	0	0	0	1	1		$V_4 + 4/8 \times (V_5 - V_4)$
1	0	0	1	0	0		$V_4 + 5/8 \times (V_5 - V_4)$
1	0	0	1	0	1		$V_4 + 6/8 \times (V_5 - V_4)$
1	0	0	1	1	0		$V_4 + 7/8 \times (V_5 - V_4)$
1	0	0	1	1	1		V_5
1	0	1	0	0	0		$V_5 + 1/8 \times (V_6 - V_5)$
1	0	1	0	0	1		$V_5 + 2/8 \times (V_6 - V_5)$
1	0	1	0	1	0		$V_5 + 3/8 \times (V_6 - V_5)$
1	0	1	0	1	1		$V_5 + 4/8 \times (V_6 - V_5)$
1	0	1	1	0	0		$V_5 + 5/8 \times (V_6 - V_5)$
1	0	1	1	0	1		$V_5 + 6/8 \times (V_6 - V_5)$
1	0	1	1	1	0		$V_5 + 7/8 \times (V_6 - V_5)$
1	0	1	1	1	1		V_6
1	1	0	0	0	0		$V_6 + 1/8 \times (V_7 - V_6)$
1	1	0	0	0	1		$V_6 \times 2/8 \times (V_7 - V_6)$
1	1	0	0	1	0		$V_6 + 3/8 \times (V_7 - V_6)$
1	1	0	0	1	1		$V_6 + 4/8 \times (V_7 - V_6)$
1	1	0	1	0	0		$V_6 + 5/8 \times (V_7 - V_6)$
1	1	0	1	0	1		$V_6 + 6/8 \times (V_7 - V_6)$
1	1	0	1	1	0		$V_6 + 7/8 \times (V_7 - V_6)$
1	1	0	1	1	1		V_7
1	1	1	0	0	0		$V_7 + 51/612 \times (V_8 - V_7)$
1	1	1	0	0	1		$V_7 + 102/612 \times (V_8 - V_7)$
1	1	1	0	1	0		$V_7 + 153/612 \times (V_8 - V_7)$
1	1	1	0	1	1		$V_7 + 204/612 \times (V_8 - V_7)$
1	1	1	1	0	0		$V_7 + 255/612 \times (V_8 - V_7)$
1	1	1	1	0	1		$V_7 + 306/612 \times (V_8 - V_7)$
1	1	1	1	1	0		$V_7 + 408/612 \times (V_8 - V_7)$
1	1	1	1	1	1		V_8

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DDD}	Digital Power Supply Voltage	-0.3	smaller of 6.0 or V_{DDA}	Volts	1,2,4
V_{DDA}	Analog Power Supply Voltage	-0.3	6.0	Volts	1,2,4
EV_8 - EV_0 OV_8 - OV_0	Analog Reference Voltage Inputs	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{S300}-V_{S1}	Output Voltage	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{IN}	Voltage on any Digital Input	-0.3	V_{DDD} + 0.3	Volts	1,2,3
P_D	Operating Power Dissipation		300	mW	
T_A	Operating Temperature (Ambient Temperature under bias)	-20	85	°C	1
T_{STR}	Storage Temperature	-30	85	°C	1

NOTES: 1) Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

2) All voltages are with respect to ground (DGND) unless otherwise noted.

3) For D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, DCLK, DATA_INV, 2xCLK, LP, EIO1#, EIO300# and LD300_1 input pads.

4) **V_{DDA} must be greater than or equal to V_{DDD} for proper circuit operation**. For this reason, V_{DDA} should be powered on first (or at the same time as V_{DDD}). Also, V_{DDD} should be powered off first, or at same time as V_{DDA}.

5.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDD}	Digital Supply Voltage	2.3 3.0	2.5 3.3	2.7 3.6	Volts Volts	1 1
V_{DDA}	Analog Supply Voltage	4.5	5.0	5.5	Volts	1
T_A	Ambient Temperature	0	25	70	°C	
EV_8 - EV_0 OV_8 - OV_0	Analog Reference Voltage	0		V_{DDA}	Volts	1, 2
I_{REF}	Analog Reference Current			20	mA	

NOTES: 1) All voltages are with respect to ground (DGND) unless otherwise noted.
2) Case I: $V_{DDA} \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0$ for EV_n or OV_n
Case II: $V_{DDA} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8$ for EV_n or OV_n

5.3 DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5 V ± 0.5 V, T_A = 25° C, unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions	Note
V_S	Analog Output Voltage				VDDA-0.03	Volts		1
V_{ST}	Analog Output Transition Band				$\|E/OV_8-E/OV_0\|$	Volts		
V_{ERR}	Analog Output Error Voltage		-0.15		+0.15	LSB		2
V_{IH}	Logic Input high Voltage		$0.7V_{DDD}$			Volts		3
V_{IL}	Logic Input low Voltage				$0.3V_{DDD}$	Volts		3
V_{OH}	Logic Output high Voltage		V_{DDD} - 0.4			Volts	I_{OH} = - 0.4 mA	4
V_{OL}	Logic Output low Voltage				0.4	Volts	I_{OL} = 0.4 mA	4
I_{QR}	Reference Quiescent Current		0.53	0.9	1.27	mA		5
I_{DDA}	Analog Supply Current				400	µA	V_{DDA} = 5.0 V	6
I_{DDD}	Digital-Supply Current (active)			3.5	5.0	mA	V_{DDD} = 2.5 V	6
				5.0	7.0	mA	V_{DDD} = 3.3 V	6
I_{DDD}	Digital-Supply Current (Stand-by)			80	400	µA	V_{DDD} = 2.5 V	7
				100	400	µA	V_{DDD} = 3.3 V	7
I_{IN}	Input Leakage Current		-5		+5	µA	$0 < V_{IN} < V_{DDD}$	
C_{IN}	Input Capacitance				5	pF	4	
R_{String}	String Resistance	E/OV0-E/OV1	380	561	723	Ω		
		E/OV1-E/OV2	219	304	389			
		E/OV2-E/OV3	185	256	327			
		E/OV3-E/OV4	185	256	327			
		E/OV4-E/OV5	185	256	327			
		E/OV5-E/OV6	185	256	327			
		E/OV6-E/OV7	219	304	389			
		E/OV7-E/OV8	434	612	790			
R_{OUT}	Output Resistance							
	E/OV_0-E/OV_1 (at code 2)				23.8	kΩ		
	E/OV_1-E/OV_2 (at code 11)				14.4			
	E/OV_2-E/OV_3 (at code 19)				12.5			
	E/OV_3-E/OV_4 (at code 27)				12.5			
	E/OV_4-E/OV_5 (at code 35)				12.5			
	E/OV_5-E/OV_6 (at code 43)				12.5			
	E/OV_6-E/OV_7 (at code 51)				14.4			
	E/OV_7-E/OV_8 (at code 61)				25.9			

NOTES: 1) See Table 4-2 for digital code-Voltage relationship.

2) For all codes

3) DCLK, LP, DATA_INV, 2xCLK, D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, EIO1#, EIO300#, and LD300_1 inputs

4) EIO1# and EIO300# outputs
5) Quiescent current into E/OV_0 and out of E/OV_8 with $|E/OV_0-E/OV_8|$ = 2.5V and all other references floating.
6) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is loading,100% of data lines toggle each DCLK cycle
7) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is not loading,100% of data lines toggle each DCLK cycle

5.4 AC Characteristics (V_{DDD} = 3.3 V ± 0.3 V) – (Preliminary data – subject to change)

See Figures 5-1 to 5-4 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min 2xCLK/2xCLK	Max 2xCLK/2xCLK	Units	Note
f_{MAX}	Maximum DCLK frequency	65/32.5		MHz	
t_{CLK}	DCLK period	15.4/30.8		ns	
t_1	DCLK high pulse width	6/6		ns	
t_2	DCLK low pulse width	6/6		ns	
t_3	DCLK, LP rise time		6/6	ns	
t_4	DCLK, LP fall time		6/6	ns	
t_5	Data setup to DCLK	0/0		ns	
t_6	Data hold from DCLK	5/7		ns	
t_7	DATA_INV setup to DCLK	2/2		ns	
t_8	DATA_INV hold from DCLK	3/5		ns	
t_9	DCLK low to LP high	50/50		ns	
t_{10}	LP low to DCLK high	50/50		ns	
t_{11}	LP high pulse width	50/50		ns	1
t_{12}	Enable-In setup to DCLK	3/-2		ns	
t_{13}	DCLK to Enable-Out low		10/14	ns	2

NOTES: 1) LP width should not be wider than necessary since outputs don't drive to the next value until LP goes low.

2) C_{LOAD} = 15 pF (See Figure 5-5)

5.5 AC Characteristics (V_{DDD} = 2.5 V ± 0.2 V) – (Preliminary data – subject to change)

See Figures 5-1 to 5-4 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min 2xCLK/2xCLK	Max 2xCLK/2xCLK	Units	Note
f_{MAX}	Maximum DCLK frequency	45/22.5		MHz	
t_{CLK}	DCLK period	22.2/44.4		ns	
t_1	DCLK high pulse width	8/8		ns	
t_2	DCLK low pulse width	8/8		ns	
t_3	DCLK, LP rise time		6/6	ns	
t_4	DCLK, LP fall time		6/6	ns	
t_5	Data setup to DCLK	1/1		ns	
t_6	Data hold from DCLK	6/12		ns	
t_7	DATA_INV setup to DCLK	3/3		ns	
t_8	DATA_INV hold from DCLK	4/10		ns	
t_9	DCLK low to LP high	50/50		ns	
t_{10}	LP low to DCLK high	50/50		ns	
t_{11}	LP high pulse width	50/50		ns	1
t_{12}	Enable-In setup to DCLK	6/-2		ns	
t_{13}	DCLK to Enable-Out low		14/18	ns	2

NOTES: 1) LP width should not be wider than necessary since outputs don't drive to the next value until LP goes low.

2) C_{LOAD} = 15 pF (See Figure 5-5)

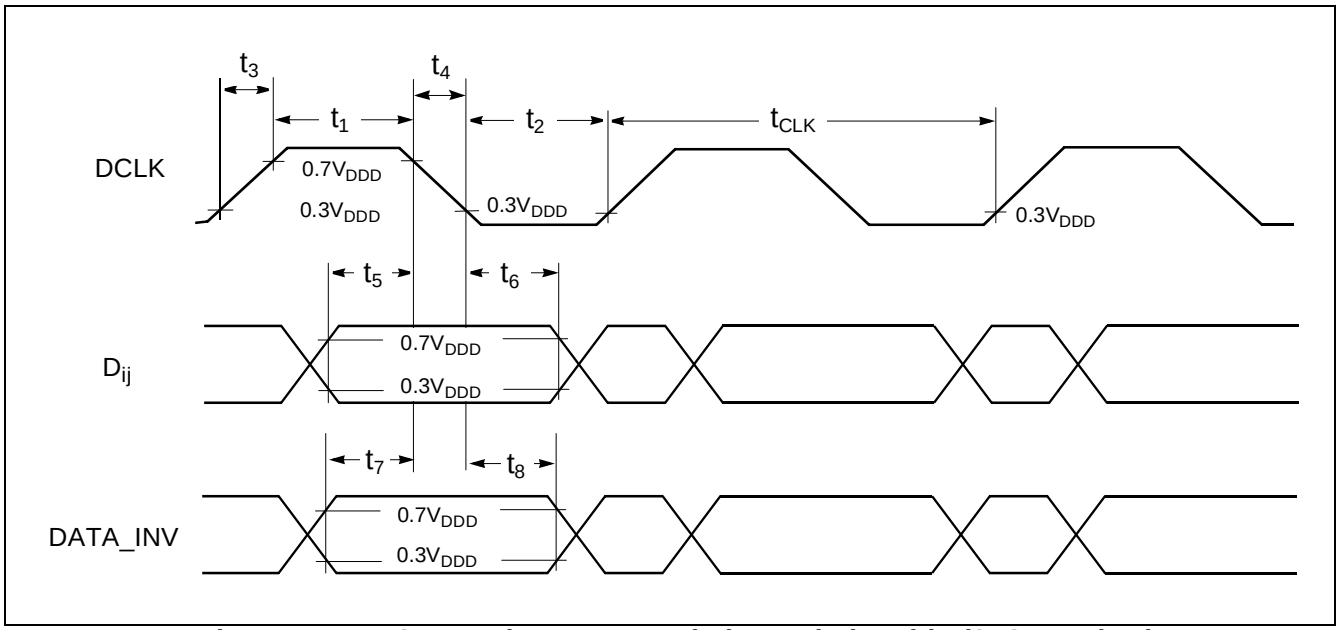


Figure 5-1: DCLK and Data Input Timing Relationship (2xCLK = low)

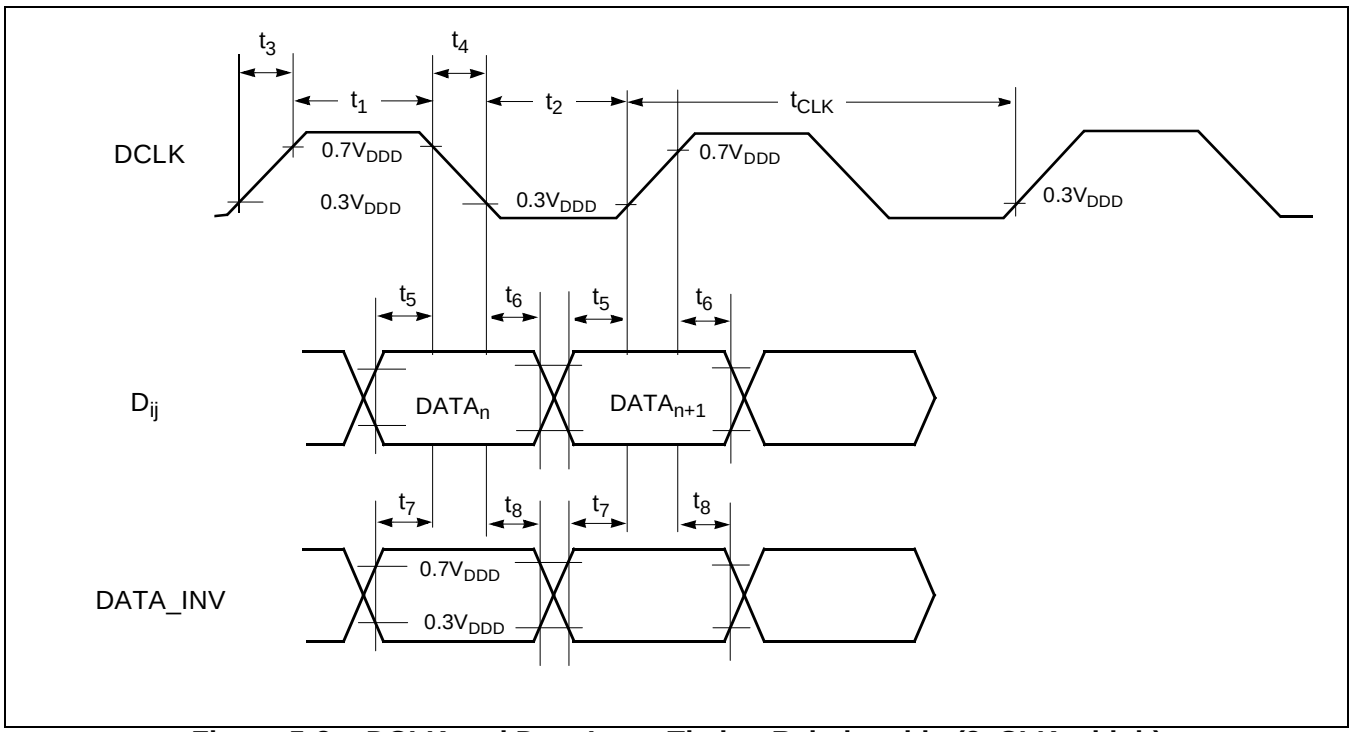


Figure 5-2: DCLK and Data Input Timing Relationship (2xCLK = high)

Note: When 2xCLK = high, the first rising edge of DCLK after LP falling edge clocks in the first display data word.

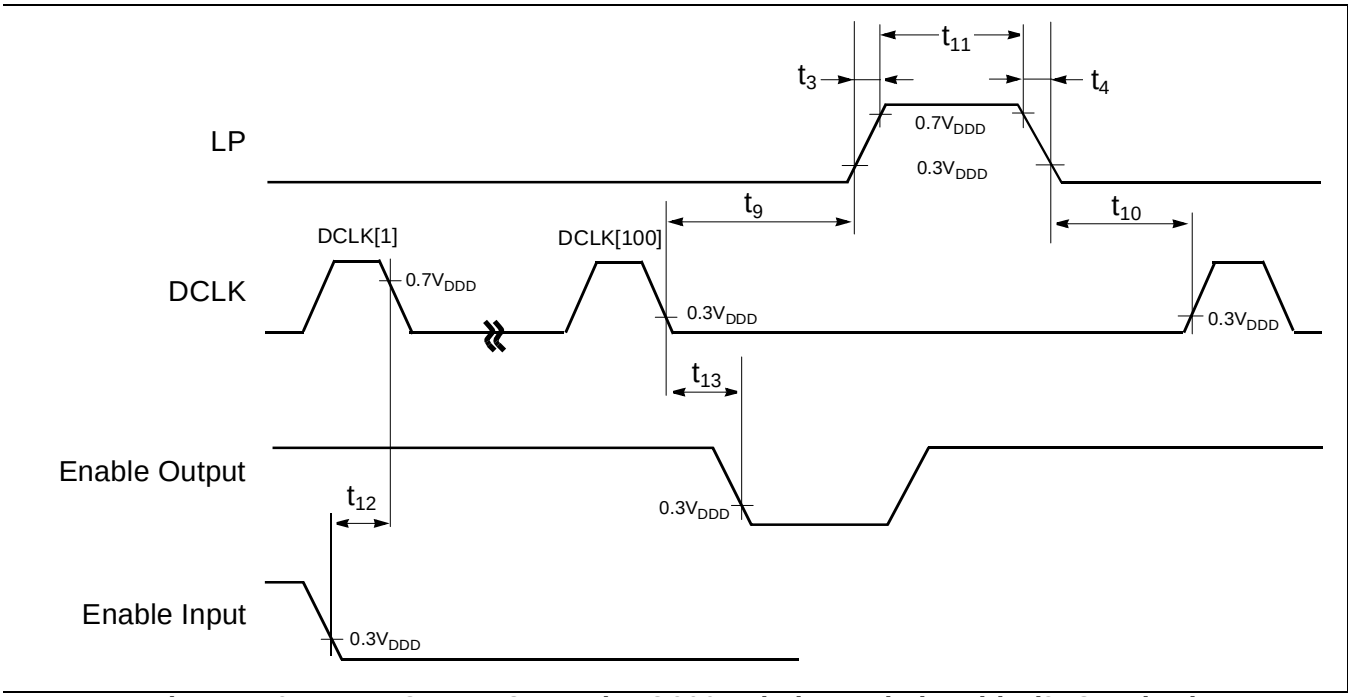


Figure 5-3: LP, DCLK, EIO1#and EIO300# Timing Relationship (2xCLK low)

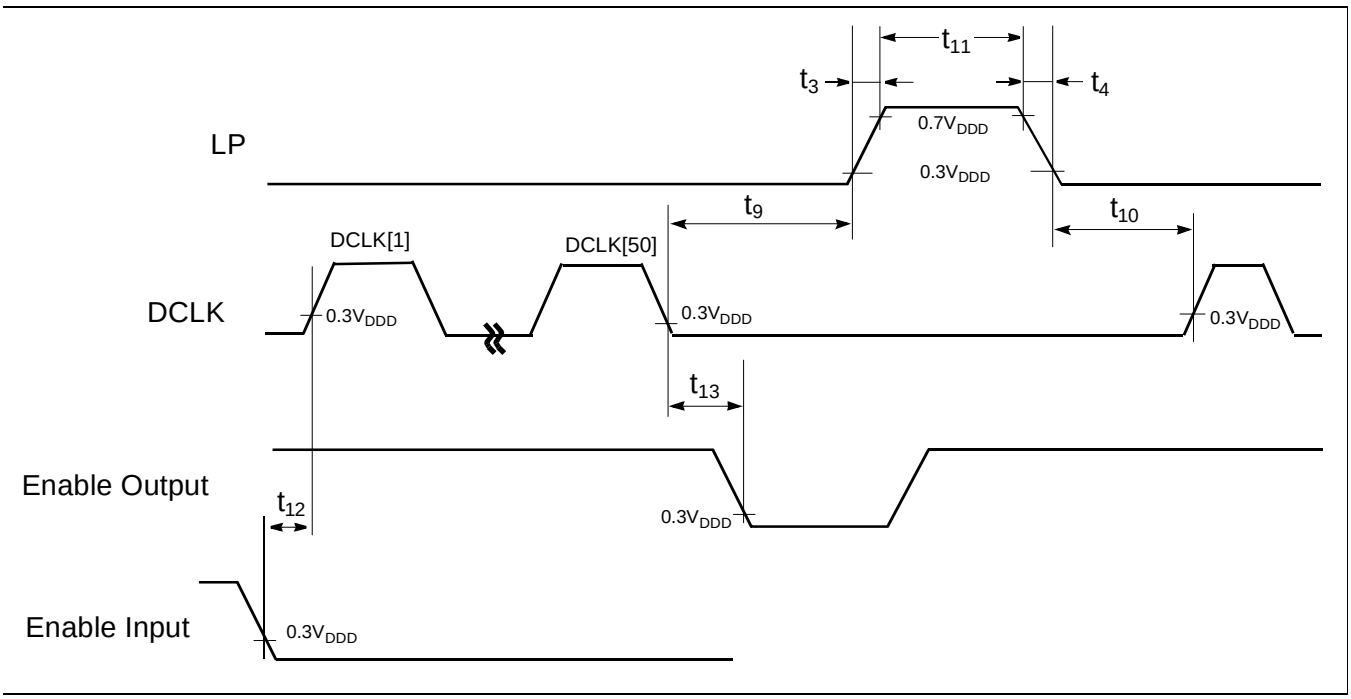


Figure 5-4: LP, DCLK, EIO1#and EIO300# Timing Relationship (2xCLK high)

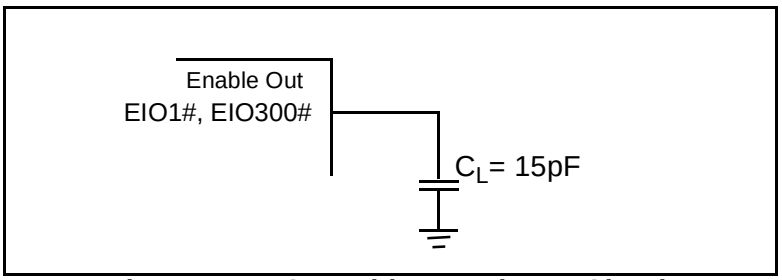


Figure 5-5: Capacitive Load Test Circuit

Changes from CL-FP6462 Version 0.02

Date of Issue	Page	Description
Timing specs t_1 to t_{13} change as follows:		
Feb. 14, 1997	19-22	Separate setup & hold times for Dij & DATA_INV inputs.
	19-22	Change definition & value of Enable-In setup to DCLK & DCLK to Enable-Out.
	19-22	Show dependence of timing specs on 2xCLK mode
	22-23	Eliminate old Figure 5-5; add new Figure 5-4 showing 2xCLK EIO timing.

Changes from CL-FP6462 Version 0.01

Date of Issue	Page	Description
September 26,1996	10,12,13	Add pad numbers to pad description table
	19,20	Change t_5,t_6,t_{12},t_{13}