Winbond Electronics Corp.

# ERMES PAGING DECODER

## GENERAL DESCRIPTION

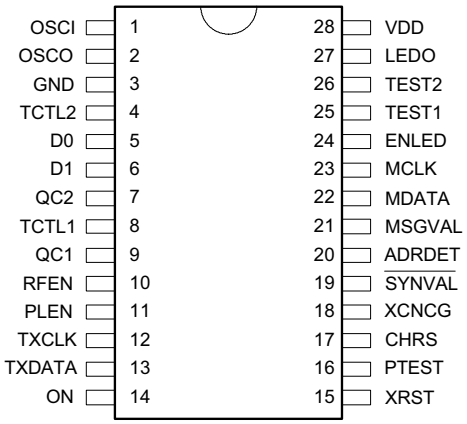
The W93910 is a low-power ERMES (Enhanced Radio MEssage System) paging protocol decoder using a single 100 kHz crystal. The W93910 supports individual call, group call, long message, changing character set and remote programming functions. To enhance the sensitivity of the pager system, a digital filter and DPLL are incorporated to remove noise and lock the signal. For convenient pager programming, the W93910 provides fully software-programmable options and also offers an independent LED frequency output.

With built-in flexible RF power saving control, frequency synthesizer enable control, quick charge controls, as well as automatic channel scan algorithm, the W93910 can combine with different RF receivers to construct a high performance, low power dissipation pager system.

## FEATURES

- 100 kHz crystal
- Built-in digital filter and digital phase lock loop
- Built-in two addresses concurrently
- One remote programming address
- International roaming capability
- Automatic channel scan algorithm
- Built in de-interleaving circuit
- 2-bit random error correction
- Individual call, long message, changing character set and remote programming
- CTAP group call
- Serial interface with μC
- 2-bit signal input from RF receiver
- RF and frequency synthesizer power saving control available
- Quick charge-discharge timing control
- Provides LED output
- 2.5 to 3.5 volts operating voltage range
- Packaged in 28-pin SSOP

## PIN CONFIGURATION



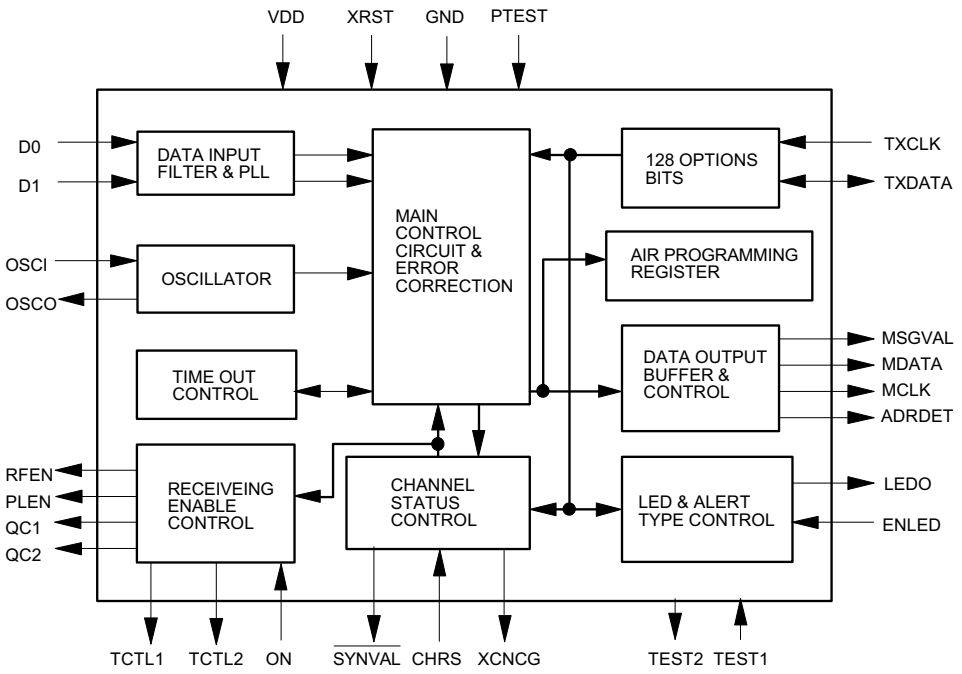

## PIN DESCRIPTION

| SYMBOL | PIN | I/O | PIN DESCRIPTION |
|---|---|---|---|
| OSCI | 1 | I | 100 kHz crystal input. |
| OSCO | 2 | O | 100 kHz crystal output. |
| GND | 3 | I | Ground power. |
| TCTL2 | 4 | O | RF control pin. Inversion output of QC2. |
| D0 | 5 | I | Demodulated data input bit0(LSB). |
| D1 | 6 | I | Demodulated data input bit1(MSB). |
| QC2 | 7 | O | Receiver quick charge 2 signal enable. Active high/low is dependent on QC2L option bit. |
| TCTL1 | 8 | O | RF control pin. |
| QC1 | 9 | O | Receiver quick charge 1 signal enable. Active high/low is dependent on QC1L option bit. |
| RFEN | 10 | O | Receiver power control. Active high/low is dependent on RFENL option bit. |
| PLEN | 11 | O | PLL frequency synthesizer power control. Active high/low depends on PLENL option bit. μC must program the freq. synthesizer counter while PLEN inactive. W93910 internal channel will be decided during PLEN active edge. |

Pin Description, continued

| SYMBOL | PIN | I/O | PIN DESCRIPTION |
|---|---|---|---|
| TXCLK | 12 | I | 192 option bits clock input from μC. TXDATA will be latched by W93910 during TXCLK rising edge. |
| TXDATA | 13 | I/O | 192 option bits serial data input from μC. Option bit address will be increased by one after each TXCLK period. After 192 option setting, the TXDATA pin will change to output pin for received OPID information access. |
| ON | 14 | I | Active high to enable W93910 chip operating. Oscillator starts oscillation after ON rising edge. OSCO will always stop while ON is low. |
| XRST | 15 | I | Internal pull low, Active high to reset decoder. |
| PTEST | 16 | I | Internal pull low, Test mode only. |
| CHRS | 17 | I | Force roaming control pin. Connect to GND for normal operation. Pull high is only for test purpose. |
| XCNCG | 18 | O | During PLEN pin high level, XCNCG (eXternal ChaNnel ChanGe) rising edge will inform μC to change channel according to channel scanning rule. |
| $\overline{\text{SYNVAL}}$ | 19 | O | Synchronization Indicator (out-of-range indicator output). Output low when synchronized with paging system. |
| ADRDET | 20 | O | Active high while the user IA detected in the address partition. (normally Low) |
| MSGVAL | 21 | O | MSGVAL will be active during MCLK, MDATA available period. Active high/low is dependent on MSGI option bit. |
| MDATA | 22 | O | Serial paging message output to μC. Rising/falling edge is dependent on MCKEG option bit. UDI1–0 used to select interval per bytes MDATA. |
| MCLK | 23 | O | Serial clock output to μC for available paging message. MCKI used to select initial state, and MCK1, MCK0 used to select clock rate. |
| ENLED | 24 | I | Internal pull low, Active high to enable LEDO output. |
| TEST1 | 25 | I | Test only. No connection for normal operation |
| TEST2 | 26 | O | Test only. No connection for normal operation |
| LEDO | 27 | O | 10/4 kHz or 40/16 kHz CMOS clock output. |
| $V_{DD}$ | 28 | I | 3 volts power supply. |

## BLOCK DIAGRAM



## ADDRESS & OPTION LIST

| BIT NO. | DATA | BIT NO. | DATA | BIT NO. | DATA | BIT NO. | DATA | BIT NO. | DATA | BIT NO. | DATA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ***b0*** | 0 | ***b32*** | FILT1 | ***b64*** | 1 | ***b96*** | SIEN | ***b128*** | 1 | ***b160*** | 1 |
| ***b1*** | IA17 | ***b33*** | GIA17 | ***b65*** | ZC2 | ***b97*** | QCON0 | ***b129*** | RPIA17 | ***b161*** | RPZC2 |
| ***b2*** | IA16 | ***b34*** | GIA16 | ***b66*** | ZC1 | ***b98*** | RFON | ***b130*** | RPIA16 | ***b162*** | RPZC1 |
| ***b3*** | IA15 | ***b35*** | GIA15 | ***b67*** | ZC0 | ***b99*** | PL1 | ***b131*** | RPIA15 | ***b163*** | RPZC0 |
| ***b4*** | IA14 | ***b36*** | GIA14 | ***b68*** | CC6 | ***b100*** | PL0 | ***b132*** | RPIA14 | ***b164*** | RPCC6 |
| ***b5*** | IA13 | ***b37*** | GIA13 | ***b69*** | CC5 | ***b101*** | GIAEN | ***b133*** | RPIA13 | ***b165*** | RPCC5 |
| ***b6*** | IA12 | ***b38*** | GIA12 | ***b70*** | CC4 | ***b102*** | PAEN | ***b134*** | RPIA12 | ***b166*** | RPCC4 |
| ***b7*** | IA11 | ***b39*** | GIA11 | ***b71*** | CC3 | ***b103*** | GPAEN | ***b135*** | RPIA11 | ***b167*** | RPCC3 |
| ***b8*** | IA10 | ***b40*** | GIA10 | ***b72*** | CC2 | ***b104*** | MCKI | ***b136*** | RPIA10 | ***b168*** | RPCC2 |
| ***b9*** | IA9 | ***b41*** | GIA9 | ***b73*** | CC1 | ***b105*** | MDAI | ***b137*** | RPIA9 | ***b169*** | RPCC1 |
| ***b10*** | IA8 | ***b42*** | GIA8 | ***b74*** | CC0 | ***b106*** | MCKEG | ***b138*** | RPIA8 | ***b170*** | RPCC0 |
| ***b11*** | IA7 | ***b43*** | GIA7 | ***b75*** | OP2 | ***b107*** | RFENL | ***b139*** | RPIA7 | ***b171*** | RPOP2 |
| ***b12*** | IA6 | ***b44*** | GIA6 | ***b76*** | OP1 | ***b108*** | PLENL | ***b140*** | RPIA6 | ***b172*** | RPOP1 |
| ***b13*** | IA5 | ***b45*** | GIA5 | ***b77*** | OP0 | ***b109*** | QC1L | ***b141*** | RPIA5 | ***b173*** | RPOP0 |
| ***b14*** | IA4 | ***b46*** | GIA4 | ***b78*** | FSN3 | ***b110*** | QC2L | ***b142*** | RPIA5 | ***b174*** | RSVD |
| ***b15*** | IA3 | ***b47*** | GIA3 | ***b79*** | FSN2 | ***b111*** | D0IV | ***b143*** | RPIA3 | ***b175*** | RSVD |
| ***b16*** | IA2 | ***b48*** | GIA2 | ***b80*** | FSN1 | ***b112*** | D1IV | ***b144*** | RPIA2 | ***b176*** | RSVD |
| ***b17*** | IA1 | ***b49*** | GIA1 | ***b81*** | FSN0 | ***b113*** | MCK1 | ***b145*** | RPIA1 | ***b177*** | RSVD |
| ***b18*** | IA0 | ***b50*** | GIA0 | ***b82*** | 0 | ***b114*** | MCK0 | ***b146*** | RPIA0 | ***b178*** | RSVD |
| ***b19*** | BN3 | ***b51*** | CH3 | ***b83*** | 1 | ***b115*** | LKR1 | ***b147*** | RPI | ***b179*** | RSVD |
| ***b20*** | BN2 | ***b52*** | CH2 | ***b84*** | 0 | ***b116*** | LKR0 | ***b148*** | RSVD | ***b180*** | RSVD |
| ***b21*** | BN1 | ***b53*** | CH1 | ***b85*** | 1 | ***b117*** | 0 | ***b149*** | RSVD | ***b181*** | RSVD |
| ***b22*** | BN0 | ***b54*** | CH0 | ***b86*** | 1 | ***b118*** | LEDF | ***b150*** | RSVD | ***b182*** | RSVD |
| ***b23*** | PA5 | ***b55*** | GPA5 | ***b87*** | 0 | ***b119*** | MSGI | ***b151*** | RPPA5 | ***b183*** | RSVD |
| ***b24*** | PA4 | ***b56*** | GPA4 | ***b88*** | 0 | ***b120*** | UDI1 | ***b152*** | RPPA4 | ***b184*** | RSVD |
| ***b25*** | PA3 | ***b57*** | GPA3 | ***b89*** | 0 | ***b121*** | UDI0 | ***b153*** | RPPA3 | ***b185*** | RSVD |
| ***b26*** | PA2 | ***b58*** | GPA2 | ***b90*** | 0 | ***b122*** | QC1WTH | ***b154*** | RPPA2 | ***b186*** | RSVD |
| ***b27*** | PA1 | ***b59*** | GPA1 | ***b91*** | 0 | ***b123*** | 0 | ***b155*** | RPPA1 | ***b187*** | RSVD |
| ***b28*** | PA0 | ***b60*** | GPA0 | ***b92*** | 0 | ***b124*** | 0 | ***b156*** | RPPA0 | ***b188*** | RSVD |
| ***b29*** | 0 | ***b61*** | LPWR | ***b93*** | 0 | ***b125*** | 0 | ***b157*** | RSVD | ***b189*** | RSVD |
| ***b30*** | 0 | ***b62*** | QCON1 | ***b94*** | 0 | ***b126*** | 0 | ***b158*** | RSVD | ***b190*** | RSVD |
| ***b31*** | 0 | ***b63*** | 0 | ***b95*** | 0 | ***b127*** | 0 | ***b159*** | 0 | ***b191*** | 0 |

Table 1

## 192 OPTION BITS

Detailed description given in Function Description section.

**RIC format**

IA17–IA0: Basic RIC initial address
BN3–BN0: Basic RIC batch number A(0000)–P(1111)
PA5–PA0: Basic RIC paging area code (000000–111111)
PAEN: Enable PA5–PA0 while PAEN active
GIA17–GIA0: Second RIC initial address
CH3–CH0: Home channel initial value from Channel 0 (0000)–Channel F (1111)
GPA5–GPA0: Second RIC paging area code (000000–111111)
GPAEN: Enable GPA5–GPA0 while GPAEN active
GIAEN: Enable GIA17–GIA0 initial address
ZC2–ZC0: Receiver zone code
CC6–CC0: Receiver country code
OP2–OP0: Receiver operator code
FSN3–FSN0: Frequency subset number (0000–1111)
RPIA17–RPIA0: Remote programming initial address
RPPA5–RPPA0: Remote programming paging area code (000000–111111)
RPZC2–RPZC0: Remote programming zone code
RPCC6–RPCC0: Remote programming country code
RPOP2–RPOP0: Remote programming operation code
RPI: Remote programming index

**RF Interface:**

RFENL: RFEN pin active level option bit
PLENL: PLEN pin active level option bit
QC1L: QC1 active level option bit
QC2L: QC2 active level option bit
D0IV: D0 input polarity option bit
D1IV: D1 input polarity option bit
PL1–0, RFON, QCON1–0, QC1WTH: RFEN, PLEN, QC1 and QC2 active timing control bits.

**uC Interface:**

MSGI, MCKI, MDA I: MSGVAL, MCLK, MDATA pin initial state option bit
MCKEG: MCLK active edge;
MCK1–MCK0: MCLK output clock option bits
UDI1–0: MCLK stop clock option
LEDF: LED freq. output selection(1:10/40 kHz; 0:4/16 kHz)

**Others:**

LKR1–LKR0: SYNC lost hold time option
SIEN: System information output enable option
LPWR: Power saving option
FILT1: Digital filter option

## FUNCTION DESCRIPTION

The W93910 ERMES paging decoder can be used to easily construct an ERMES pager with RF receiver and μC. To initialize the decoder, first, 192 option bits must be programmed through TXCLK, TXDATA pin by μC. After the oscillator has been turned on and is stable, the decoder can then receive and decode the 2 bit digital QFSK signal from the RF receiver. With built-in PLEN, RFEN, QC1 and QC2 controls, the decoder can warm up and shut down the frequency synthesizer and IF demodulator for optimum reception in different stages.

While starting, the pager will begin to search the home channel. If system synchronization can't occur in the current channel, the pager will change to the next channel according to the channel scan algorithm until synchronization occurs. Once synchronized with the channel, the pager will lock to its own batch, ready to receive paging message. If an address-matched message is received, the de-interleaved data will be transferred to μC through MDATA and MCLK pin. With the automatic channel scan algorithm, the decoder will inform μC by PLEN and XCNCG to change channel during channel scan and normal mode.

### RECEIVING OPERATION FLOW

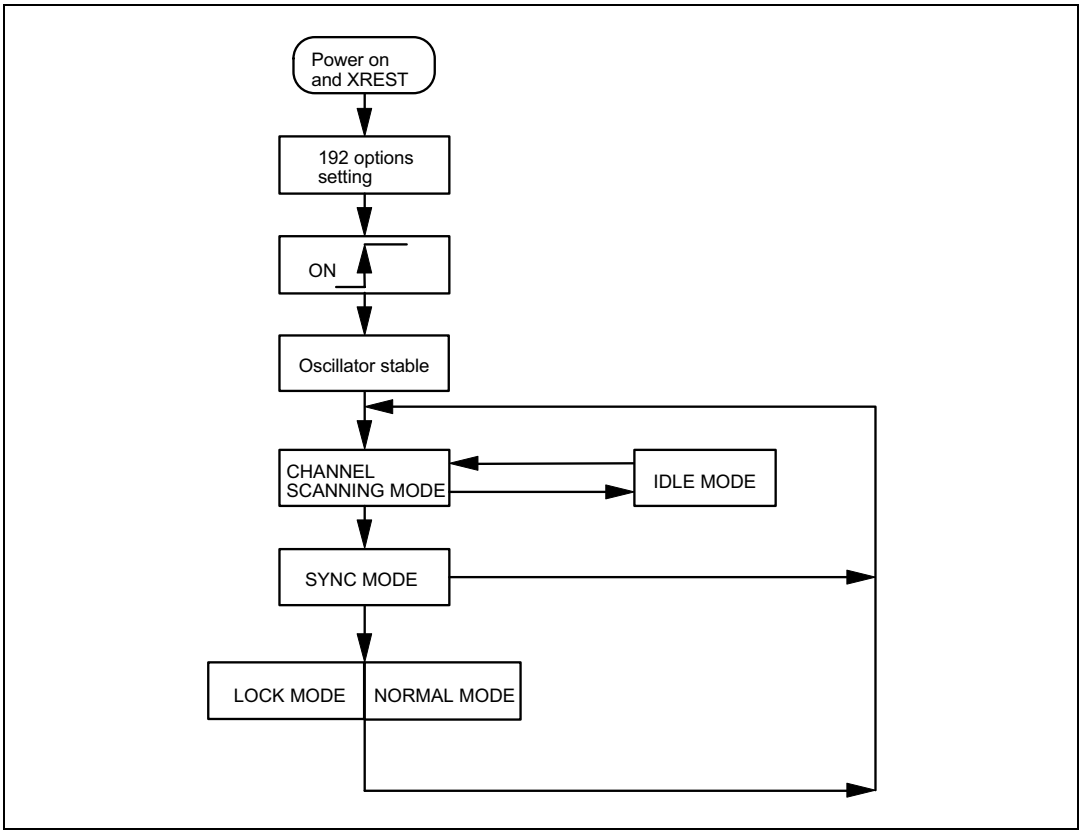



Figure 1. Operating Flow Chart

## 192 OPTION BITS PROGRAMMING

After power on and XRST pin active, the μC should send 192 clock inputs to TXCLK pin and 192 options to TXDATA pin. Figure 2 shows the TXCLK and TXDATA programming timing. The data values in TXDATA are latched at TXCLK rising edge. The clock rate of TXCLK should be smaller than 1 MHz.

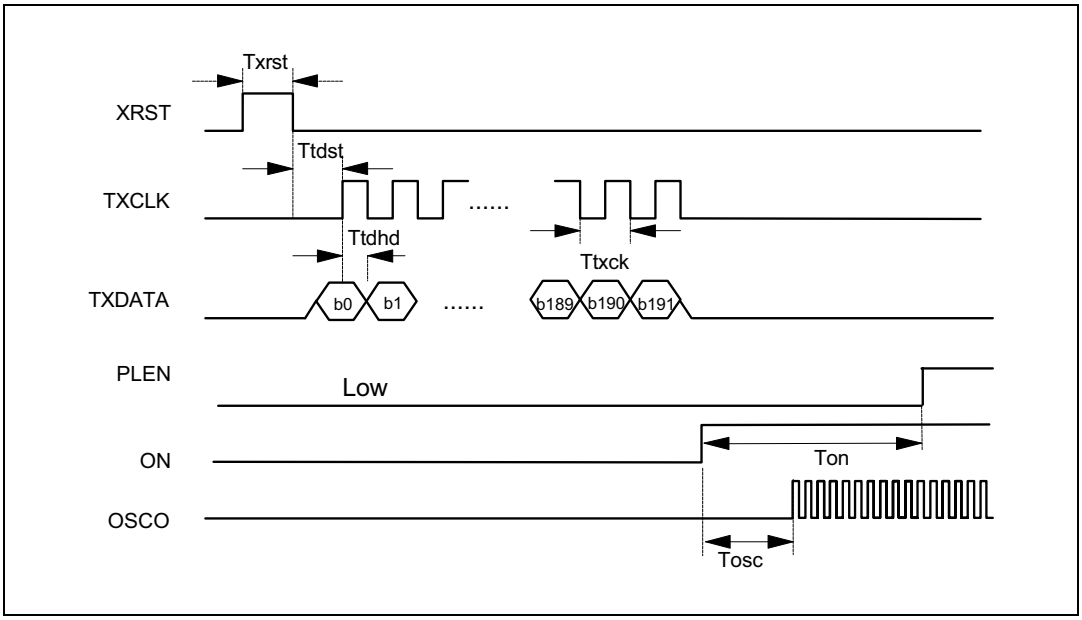



Figure 2. 192 option bits programming timing

## RECEIVING ENABLE CONTROL

After the W93910 has received the 192 options, it will start the operation if the ON pin is high, or in stand-by mode if ON pin is low. The On pin can be pulled high at any time to activate the oscillator. After oscillator is stable, the decoder will activate the PLEN. RFEN, QC1, QC2, TCTL1, and TCTL2 to control the frequency synthesizer and IF demodulator, based on the option setting as shown in Figure 3. The frequency synthesizer need to be programmed to the right channel (normally home channel) before PLEN active. The PLEN is used to control the frequency synthesizer power, and inform μC of the receiving status. The output levels of RFEN, PLEN, QC1 and QC2 are defined by the option bits RFENL, PLENL, QC1L and QC2L as shown in Table 2. TCTL2 is the inversion output of QC2. The TCTL1 active level is fixed. The TCTL1 and TCTL2 output will be activated only when the LEDF option bit is set to 1.

Option bit PL1–0, RFON, QCON1–0 and QC1WTH provides different set up time for PLEN, RFEN, QC1, QC2, TCTL1 and TCTL2, as shown in Table 3, to meet different RF receiver requirements.

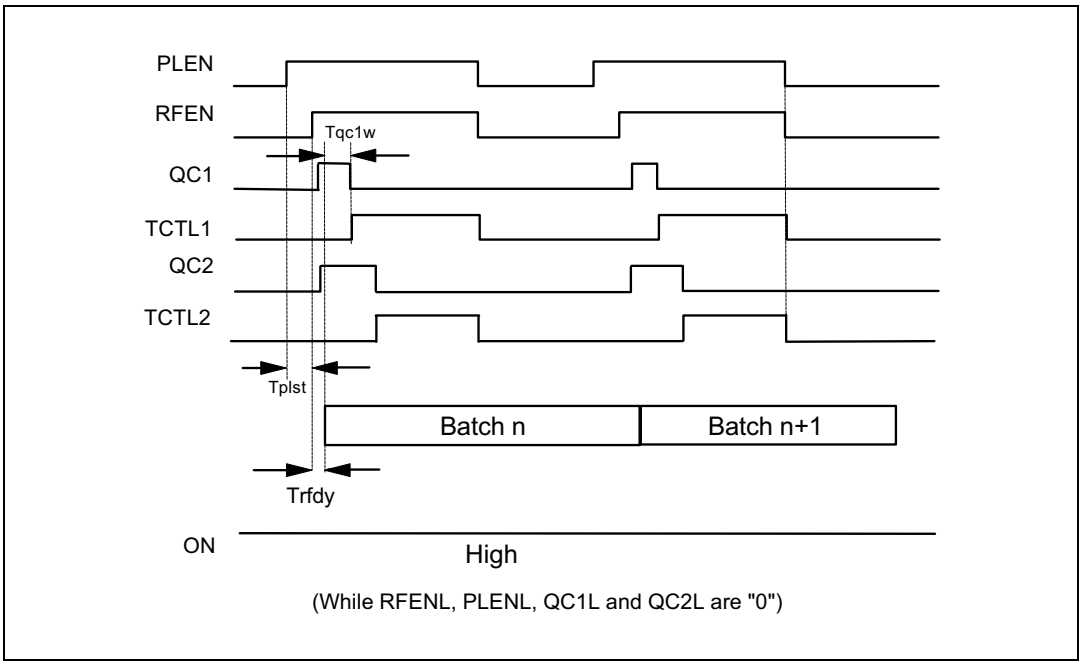



Figure 3. PLEN, RFEN, QC1, QC2, TCTL1 and TCTL2 timing

| OPTION BIT | FUNCTION |
|---|---|
| RFENL, PLEN, QC1L, QC2L | RFEN, PLEN, QC1, and QC2 pin voltage level |
| 0 | Active high |
| 1 | Active low |

Table 2. RF interface active option bits

| OPTION BIT | | FUNCTION |
|---|---|---|
| **PL1** | **PL0** | Tplst setting |
| 0 | 0 | 9.6 mS |
| 0 | 1 | 19.2 mS |
| 1 | 0 | 28.8 mS |
| 1 | 1 | Reserved |

Table 3. PLL enable timing

| OPTION BIT | FUNCTION |
|---|---|
| RFON | Trfdy |
| 0 | 4.8 mS |
| 1 | 9.6 mS |

Table 4. RF interface timing control option bit

| OPTION BIT | FUNCTION |
|---|---|
| QC1WTH | Tqc1w |
| 0 | 3.8 mS |
| 1 | 2.5 mS |

Table 5. Quick-charge duration option bit

| OPTION BIT | | FUNCTION | |
|---|---|---|---|
| QCON1 | QCON0 | QC1 duration | QC2 duration |
| 1 | 0 | Tplst + Trfdy + Tqc1w | Tplst + Trfdy + 9.6ms |
| 0 | 0 | Trfdy + Tqc1w | Trfdy + 9.6ms |
| 0 | 1 | Tqc1w | 9.6 ms |

Table 6. Quick-charge active timing control option bits

## CHANNEL SCAN MODE

In this mode, decoder will enable the receiver to search the available channel in different frequency channels based on the channel scan control algorithm.

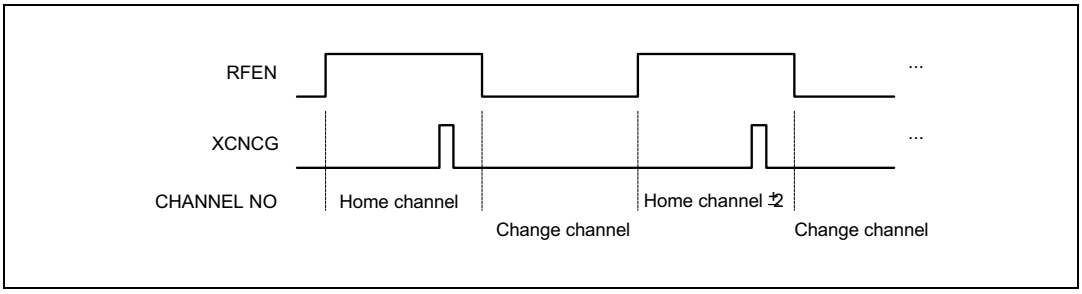



Figure 4. Channel Scan Mode

## CHANNEL SCAN CONTROL

The channel scanning and switching are controlled by the decoder. Table 7 shows the channel number and frequency. In channel scan mode, the decoder will first search the home channel, defined by the CH3–CH0. Therefore, the synthesizer should be programmed to home channel before the channel scan mode. If the pager can not detect a valid signal in the home channel, the pager will change to the next channel to search until the decoder lock to the signal. The scanning sequence is shown in Figure 5, and needs to be followed to avoid losing signal.

| OPTION BIT | FUNCTION | |
|---|---|---|
| CH3–CH0 | Home channel number | RF center frequency |
| 0000 | 0 | 169.425 MHz |
| 0010 | 2 | 169.475 MHz |
| 0100 | 4 | 169.525 MHz |
| 0110 | 6 | 169.575 MHz |
| 1000 | 8 | 169.625 MHz |
| 1010 | A | 169.675 MHz |
| 1100 | C | 169.725 MHz |
| 1110 | E | 169.775 MHz |
| 1111 | F | 169.800 MHz |
| 1101 | D | 169.750 MHz |
| 1011 | B | 169.700 MHz |
| 1001 | 9 | 169.650 MHz |
| 0111 | 7 | 169.600 MHz |
| 0101 | 5 | 169.550 MHz |
| 0011 | 3 | 169.500 MHz |
| 0001 | 1 | 169.450 MHz |

Table 7. Channel number and frequency

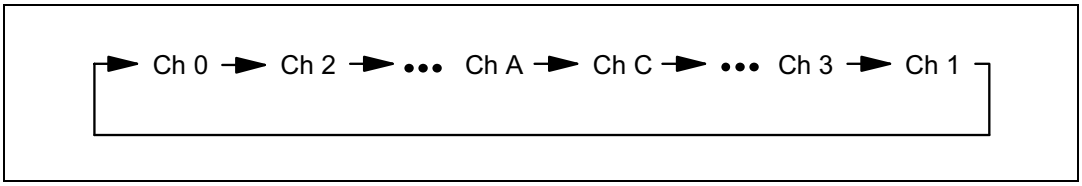



Figure 5. Channel scan sequence

The frequency channel adjustment is implemented by XCNCG, PLEN, and µC. XCNCG is used to output a high pulse to inform µC of the frequency channel increment request. µC needs to count the XCNCG high pulse during the PLEN active period. Each XCNCG pulse indicates one frequency channel increment. During the PLEN inactive period, the µC should program the synthesizer with suitable data based on the previous XCNCG counting result to ensure the receiver can catch the right channel. During the lock mode, the pager will fix at the same channel as shown in Figure 6 and 7. The normal mode operation is described in Figure 8 and 9. The batch number setting is shown in Table 8.

| OPTION BIT | FUNCTION |
|---|---|
| bn3–bn0 | Batch Number |
| 0000 | A |
| 0001 | B |
| 0010 | C |
| 0011 | D |
| 0100 | E |
| 0101 | F |
| 0110 | G |
| 0111 | H |
| 1000 | I |
| 1001 | J |
| 1010 | K |
| 1011 | L |
| 1100 | M |
| 1101 | N |
| 1110 | O |
| 1111 | P |

Table 8. bn3–bn0 batch number format

## IDLE MODE

If there is no meaningful signal after scanning the channel several times, the decoder will enter idle mode to save power, and will re-enter the channel scan mode after a period of time.

## SYNC MODE

While synchronizing with the paging system, the decoder enters sync mode and the $\overline{\text{SYNVAL}}$ pin outputs LOW The decoder will then change to lock mode or normal mode based on the receiving information.

## LOCK MODE

In lock mode, the decoder will stay at the same channel. If matching addresses appear, all the available paging messages will be received until messages are finished or time out occurs.

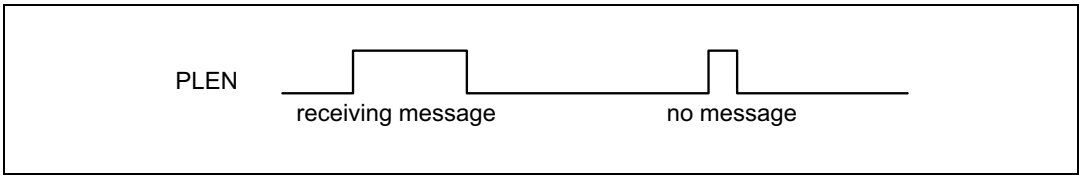



Figure 6. Lock Mode

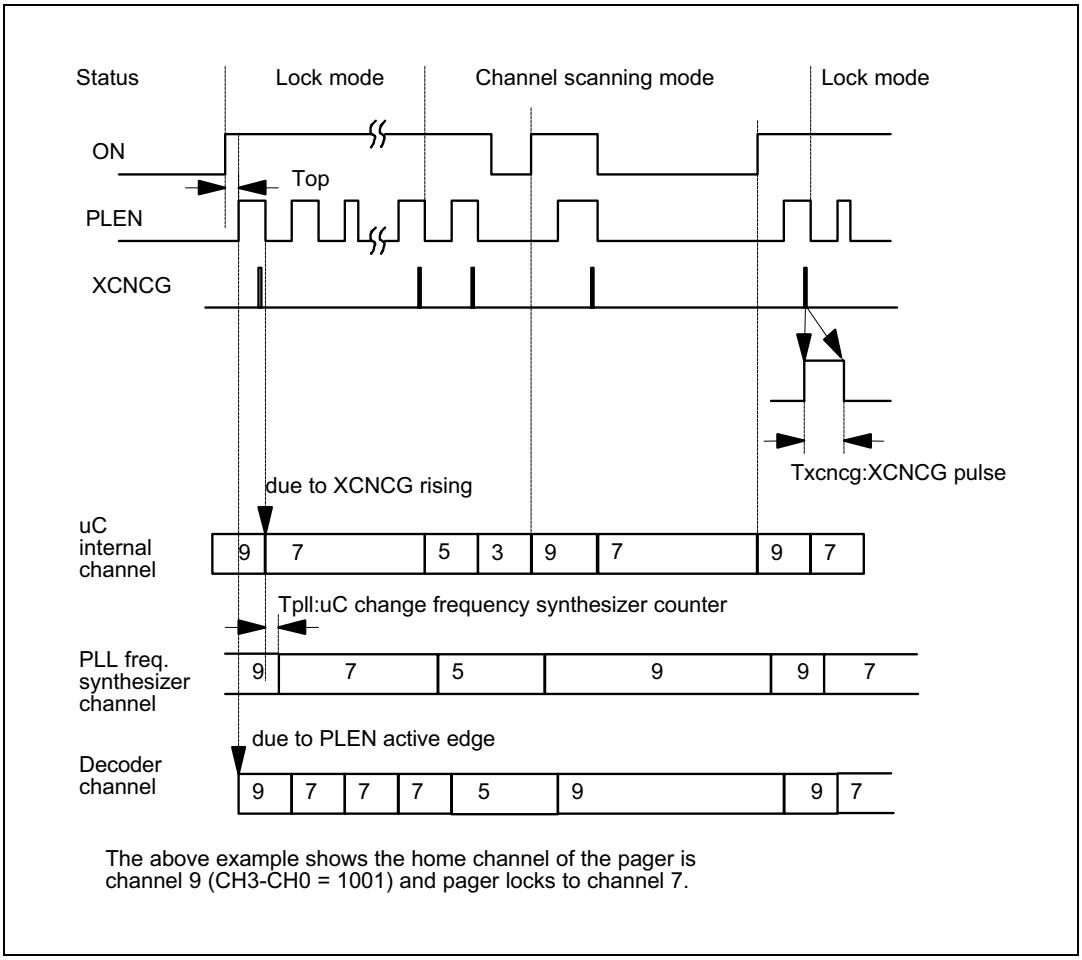



Figure 7. Channel Scan mode and lock mode

## NORMAL MODE (NONLOCK)

Decoder will enter normal mode while not in the home network or the border area indication condition. In this mode, the decoder will switch and listen to different frequency channel based on the channel scan control algorithm. The PLEN operating timing is shown in Figure 8.

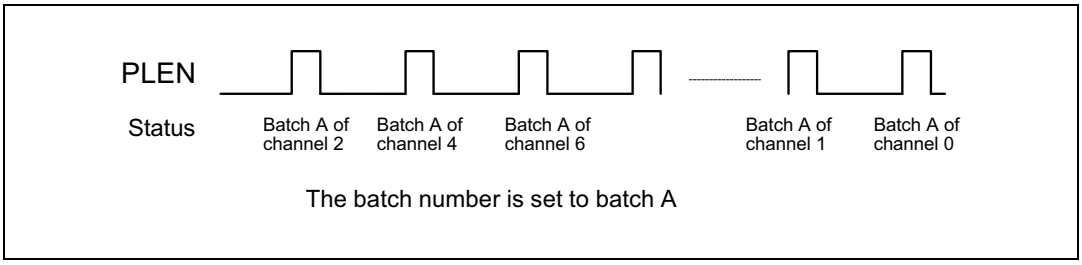



Figure 8. Normal Mode

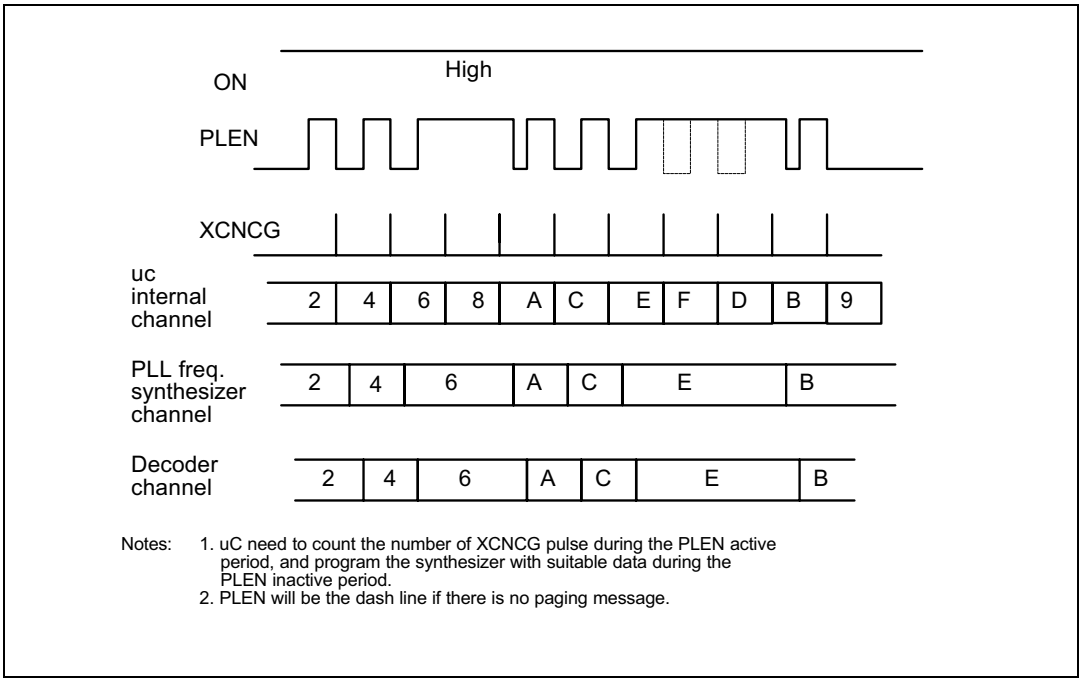



Figure 9. Channel scan in NORMAL MODE

## LOST SYNCHCONIZATION

If synchronization is lost for several minutes (pre-defined by option bit LKR1–LKR0 ), the pager will change to the channel scan mode. The $\overline{\text{SYNVAL}}$ pin will keep low during the lock mode and normal mode unless the synchronization lost duration exceeds the hold time condition, then the $\overline{\text{SYNVAL}}$ pin will change to high level and the decoder will go back to the channel scan mode.

| OPTION BIT | | FUNCTION |
|---|---|---|
| LKR1 | LKR0 | Synchronization lost hold time |
| 0 | 0 | 1 min. |
| 0 | 1 | 2 min. |
| 1 | 0 | 3 min. |
| 1 | 1 | 4 min. |

Table 9. Lock re-try option bits

## RIC (Radio Identify Code) FORMAT

For ERMES system, RIC has 35 bits and is defined by ZC2–ZC0, CC6–CC0, OP2–OP0, IA17–IA0, and BN3–BN0 option bits as shown in Table 10.

| Function | Radio Identify Code | | | | | |
|---|---|---|---|---|---|---|
| | OPID | | | LOCAL ADDRESS | | |
| | Zone Code | Country Code | Operator Code | Initial Address | Batch Number | Paging area |
| OPTION bit | ZC2–ZC0 | CC6–CC0 | OP2–OP0 | IA17–IA0 | BN3–BN0 | PA5–PA0 |
| | | | | GIA17–GIA0 | | GPA5–GPA0 |

Table 10. RIC format

The W93910 provides two initial addresses with corresponding paging area code, IA17–IA0 with PA5–PA0 and GIA17–GIA0 with GPA5–GPA0, for the same OPID. The first one is dedicated for the basic RIC. Each pager has one unique batch number, defined by BN3–BN0, and will only turn on and listen at that specific batch except where a message continues over one batch. If PAEN option bit is set to "1", the received message must match to the pre--defined paging area code, PA5–PA0. Other than in this situation, the received paging area code doesn't need to match the pre-defined PA5–PA0, but must be consistent throughout the whole message. The second IA, GIA17–GIA0, is enabled by setting the GIAEN option bit to 1. GPAEN has the same function as PAEN, but for GIA17–GIA0 address only.

| OPTION BIT | FUNCTION |
|---|---|
| GIAEN | Second user address (GPA+GIA) |
| 0 | Disable |
| 1 | Enable |

Table 11-1. Second initial address setting option bits

| OPTION | FUNCTION |
|---|---|
| PAEN, GPAEN | PA5–PA0, GPA5–GPA0 |
| 0 | Don't care |
| 1 | Enable |

Table 11-2. Paging area setting

## REMOTE PROGRAMMING

The W93910 provides remote programming addresses including initial address, paging area, zone code, and country code to support the remote programming function. These option bits are listed in Table 12. These temporary addresses can be programmed during the initial setting or modified by the air message. While receiving the remote programming address message, W93910 will automatic update the internal remote programming addresses and also pass the programming message to μC through MDATA pin. The data should be stored for re-initialization purpose. Please refer to Summary of Data Output Format. If the remote programming data is less than 18 bits, the dummy "0" is filled in the other low bits of rd17–rd0. For the first time initialization, all the option bits should be "0" including the RPI. The RPI is the remote programming index, which can be read out from MDW while receiving the remote programming message.

| OPTION BIT | FUNCTION |
|---|---|
| RPIA17–RPIA0 | Initial Address |
| RPPA5–RPPA0 | Paging Area |
| RPZC2–RPZC0 | Zone Code |
| RPCC6–RPCC0 | Country Code |
| RPOP2–RPOP0 | Operator Code |
| RPI | Remote Programming Index |

Table 12. Remote programming register

## SYSTEM INFORMATION

By setting the SIEN option bit to 1, the system information can also be read out from TXDATA pin. After 192 option bits setting, if the μC decides to read out the received system information, the μC needs to send 31 clocks to TXCLK pin. The first clock pulse will switch TXDATA pin from input to output, and the last clock pulse will disable this function. At the falling edge of the each clock pulse except the first and last clock one, the system information (batch no, country code, operator code, cycle no., hour) can be read out from the TXDATA pin. The best timing to read out the system information is right after PLEN falling edge. The format and timing are shown in Figure 10. This function is disabled if SIEN is set to 0.

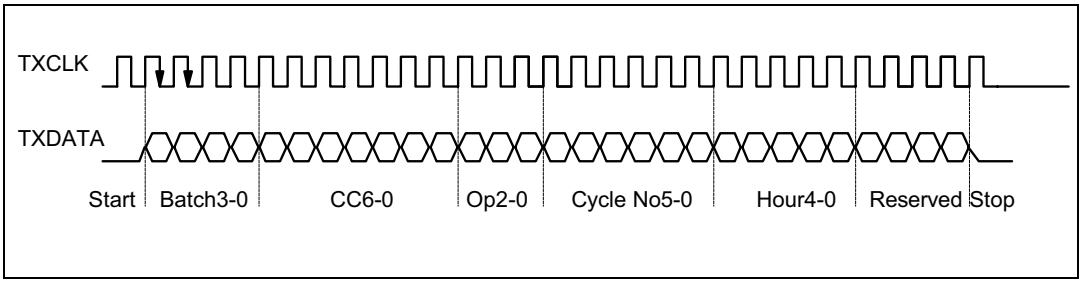



Figure 10. System information read out format

## DATA INPUT

The 4 level FSK signal is converted to 2 bit digital signal by IF demodulator, as shown in Figure 11, where fn is the carrier frequency from 169.425 MHz to 169.8 MHz. The 2 bit digital signal should be connected to the D1(MSB), D0(LSB) inputs of W93910. The D1 and D0 inputs could be inverted by setting the D1IV, and D0IV option bits to provide some flexibility.

| OPTION BIT | FUNCTION |
|---|---|
| D1IV, D0IV | D1 input, D0 input |
| 0 | Non-inversion |
| 1 | Inversion |

Table 13. D1, D0 relative option bits

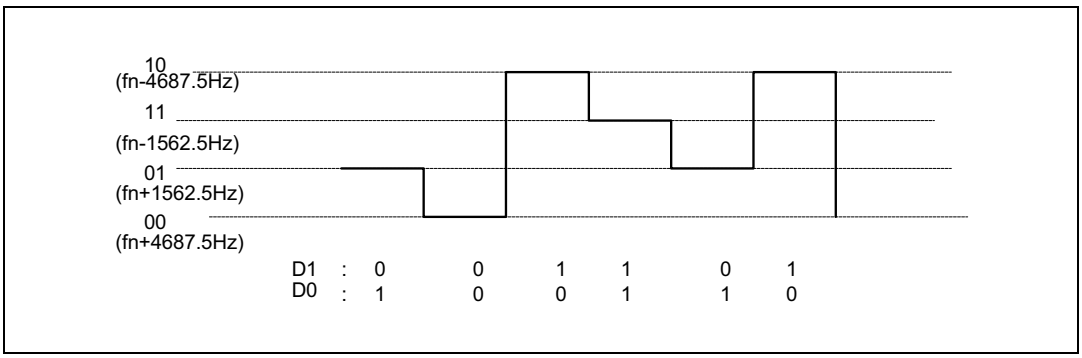



Figure 11. 4 PAM mapping to D1, D0(fn is the channel carrier frequency)

## DIGITAL FILTER & POWER SAVING

The W93910 provides different digital filter to remove the noise of the 4FSK signal. The enhanced filtering require higher power consumption. Table 14 shows different combinations of digital filtering and power saving.

| OPTION BIT | | FUNCTION |
|---|---|---|
| FILT1 | LPWR | Digital filter & power saving |
| 0 | 0 | Low power consumption, normal filtering |
| 1 | 1 | Enhanced filtering, high power consumption |

Table 14. Digital filter and power saving option

## DE-INTERLEAVER AND ERROR CORRECTION

The W93910 performs 2 bits random error correction for system information, address partition as well as message partition, and codeword de-interleaving for message partition.

## TIME OUT CONTROL

When the decoder recognizes a valid initial address it will start to search the associated paging message. Time out criteria will stop message searching at once. While the searching is stopped due to time out issue, the "epa" and "etm" in EDW format will be set to indicated the time out situation. At the mean time, the RF control signal will become inactive at once when ending message delimiter (MD) has been detected.

- **For Individual calls**

Two time out criteria shall apply. The earliest detected shall prevail:

1. If PA5–PA0 in paging message is not consistent throughout the receiving, then the epa flag will be set to "1".
2. If the paging message lasts more than 12 sec, then etm flag will be set to "1".

- **For group calls**

Individual member shall cease message search if:

1. If PA5–PA0 in paging message is not consistent throughout the receiving, then the epa flag will be set to "1".
2. If the paging message lasts more than 12 sec, then etm flag will be set to "1".

- **For long message calls**

The time out criteria for each sub-message is the same as for individual call. The time out of the whole long message should be proceeded by the software to meet the ERMES protocol.

## DATA OUTPUT CONTROL

When the chip detects the proper address, the chip will first activate ADRVAL pin to inform the µC and then send the de-interleaved paging message and related system information to the µC through MCLK and MDATA pin. The format and timing of the data output is shown in Figure 12. The data output is packed into a 3-byte word format. The function of each word is defined by the **Function Code,** the first 4 bits of byte3, as shown in Table 15. The format of the rest 20 bits will depend on the function code.

| HIGH NIBBLE OF BYTE 3 | FUNCTION CODE |
|---|---|
| 0000 | System Information Word (SIW) |
| 0010 | ComMand Word (CMW) |
| 010x | Addition Information Word (AIW) |
| 0110 | Message data Word (MDW) |
| 1110 | EnD message Word (EDW) |
| Others | RESERVED |

Table 15. Data Output Function Code

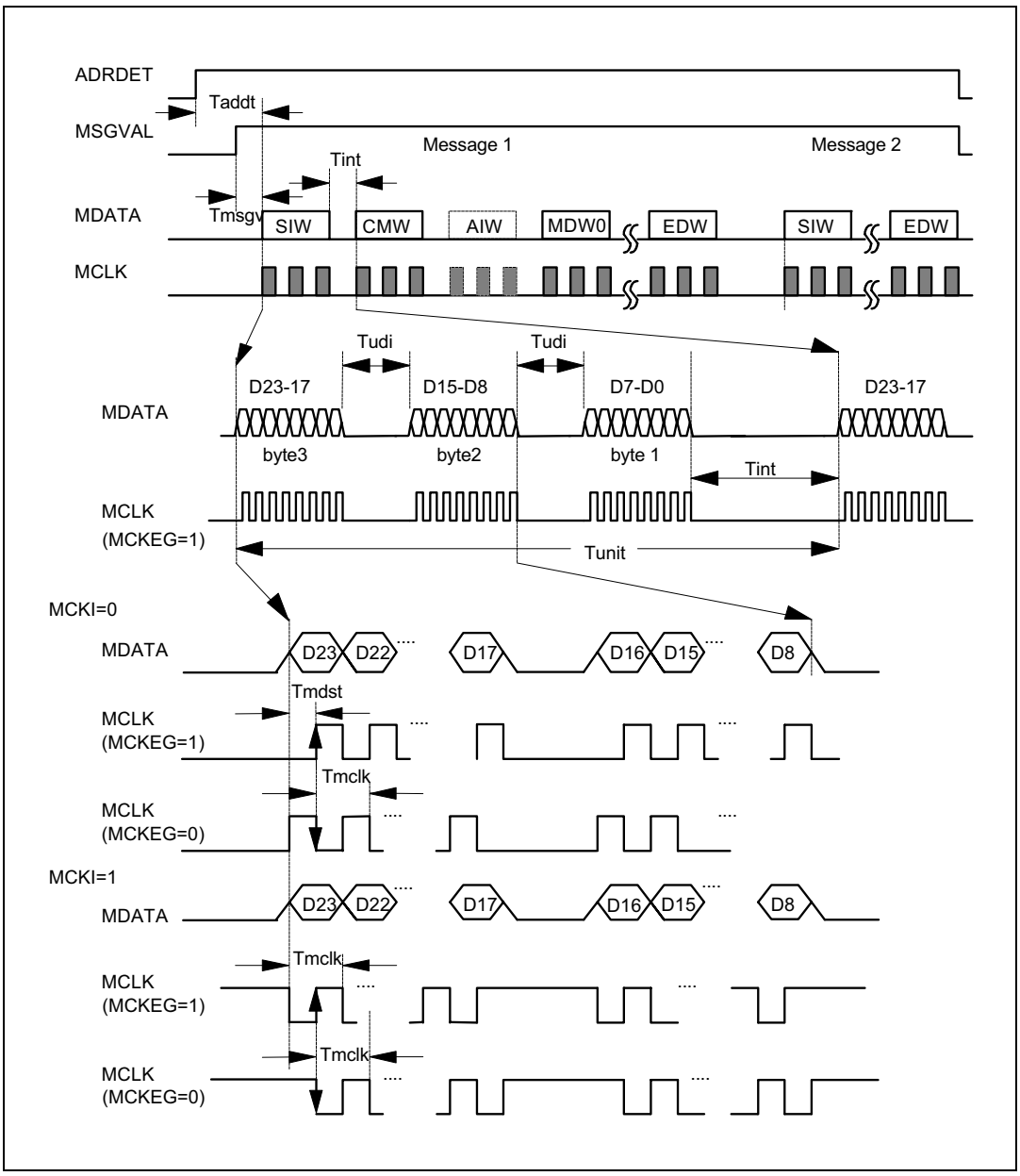



Figure 12. Data Output Timing

Table 16−Table 19 list the active level and timing option bit settings of the data output format. MCLK clock rate is defined by option bit MCK1−0. The duration between each word, Tint, and the duration between each byte, Tudi, are defined by option bit UDI1−UDI0. Option bit MCKEG defines MCLK active edge. MCKI, MSGI and MDAI option bits set MCLK, MSGVAL and MDATA pin initial and active state.

The output sequence of MDATA pin is SIW, CMW, MDW0, MDW1...MDWn, EDW for all the message types except long message. For long message, an extra AIW is added between CMW and MDW0. Please refer to **Summary of Data Output Format** for different paging message format.

| OPTION BIT | FUNCTION |
|---|---|
| MCKEG | MCLK active edge |
| 0 | Falling edge active |
| 1 | Rising edge active |

Table 16. Data output pin option

| OPTION BIT | FUNCTION |
|---|---|
| MSGI | MSGVAL active level |
| 0 | active low |
| 1 | active high |

Table 17. Data output pin option

| OPTION BIT | FUNCTION |
|---|---|
| MDAI, MCKI | MDATA, MCKI pin initial state |
| 0 | Initial low |
| 1 | Initial high |

Table 18. Data output pin option

| OPTION | | FUNCTION | |
|---|---|---|---|
| MCK1, MCK0 | UD1, UD0 | Tudi timing | Tint timing |
| 00<br>Tmclk = 80 µS | 00 | 0 | 2.08 mS |
| | 01 | 160 µS | 1.76 mS |
| | 10 | 320 µS | 1.44 mS |
| | 11 | 640 µS | 800 µS |
| 01<br>Tmclk = 40 µS | 00 | 0 | 3.04 mS |
| | 01 | 160 µS | 2.72 mS |
| | 10 | 640 µS | 1.76 mS |
| | 11 | 1 mS | 1.04 mS |
| 10<br>Tmclk = 20 µS | 00 | 0 | 3.52 mS |
| | 01 | 160 µS | 3.2 mS |
| | 10 | 640 µS | 2.24 mS |
| | 11 | 1.16 mS | 1.2 mS |
| 11<br>Tmclk = 5 µS | 00 | 0 | 3.88 mS |
| | 01 | 80 µS | 3.72 mS |
| | 10 | 640 µS | 2.66 mS |
| | 11 | 1.275 mS | 1.33 mS |

Table 19. Tudi and Tint timing option (where Tunit = 4 mS minimum)

### SIW Definition

When the W93910 receives a message, the MSGVAL pin will be activated first, and then SIW will be the first word to output from the MDATA pin. System information, such as year, month, date, hour, day and OPID, may resolve from SIW.

| SIW | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| byte3 | 0 | 0 | 0 | 0 | fsi | sn2 | sn1 | sn0 |
| byte2 | s13 | s12 | s11 | s10 | s9 | s8 | s7 | s6 |
| byte1 | s5 | s4 | s3 | s2 | s1 | s0 | X | X |

Table 20. SIW format

### SIW Description

| fsi | s13 | s12 | s11 | s10 | s9 | s8 | s7 | s6 | s5 | s4 | s3 | s2 | s1 | s0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | z2 | z1 | z0 | h4 | h3 | h2 | h1 | h0 | d4 | d3 | d2 | d1 | d0 | rv |
| 1 | w2 | w1 | w0 | mt3 | mt2 | mt1 | mt0 | yr6 | yr5 | yr4 | yr3 | yr2 | yr1 | yr0 |

Table 21. s13–s0 format

sn2–sn0 is the subsequence number 0(000) to 4(100) that existed in SI field.

fsi is the function bit of s13–s0 that provides all transmitter time base information.

1. fsi = 0 while SSIT is equal "0000" in SSI field

   z2–z0: RIC zone code from 000–111

   h4–h0: Local hour from 0(00000)–23(10111)

   d4–d0: Local date from 1(00001)–31(11111)

   rv: reserve bit for future

   (Note: minute will be shown as cy5–cy0 in EDW)

2. fsi = 1 while SSIT is equal "0001" in SSI field

   w2–w0: Local day of week from Monday(001)–Sunday(111)

   mt4–mt0: Month from January(0001)–December(1100)

   yr6–yr0: Year from 1990(0000000) –2117(1111111)

### CMW Definition

The second word is CMW, which indicates the message type, message number, paging category, and alert type of received paging message.

| CMW | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| byte3 | 0 | 0 | 1 | 0 | cm3 | cm2 | cm1 | cm0 |
| byte2 | eb | g1 | g0 | mn4 | mn3 | mn2 | mn1 | mn0 |
| byte1 | 0 | 0 | pc1 / f1 | pc0 / f0 | ain3 | ain2 | ain1 | ain0 |

Table 22. CMW format

**CMW Description:**

| cm3–cm0 | message type description |
|---|---|
| 0000 | individual call |
| 1000 | long message w/o C.S--First submessage. |
| 1001 | long message w/o C.S--Others submessage. |
| 1010 | remote programming |
| 1100 | retransmit latest message no# |
| 1101 | long message with C.S--Others submessage. |
| 1110 | long message with C.S--First submessage. |
| 1111 | Change Character Set (C.S.) |
| Others | Reserved |

Table 23. Message type description (cm3–cm0)

| eb | External flag |
|---|---|
| 0 | Home Receiver |
| 1 | External receiver |

Table 24. External receiver index

| g1 g0 | RIC address index of received message |
|---|---|
| 00 | IA17–IA0 available |
| 01 | Air Programming RIC |
| 10 | GIA17–GIA0 available |
| 11 | Group call by CTAP method |

Table 25. Received message address index

| mn4–mn0 | Message number |
|---|---|
| 00000 | For group calls the reserved dummy value 00000 shall be used. The reserved dummy value may also be used when the message numbering is deactivated, as with remote programming. |
| Others | For individual calls the initial value shall be 00001; then mn4–mn0 will be increased by 1 continuously for the following message. |

Table 26. Message number description (mn4–mn0)

| pc1 pc0 | Paging category |
|---|---|
| 00 | Tone only |
| 01 | Numeric |
| 10 | Alphanumeric |
| 11 | transparent data |

Table 27. Paging category index

The ain3–ain0 is used to indicated the alert type of the message, except in the remote programming situation.

| ain3–ain0 | Alert type description |
|---|---|
| 0000 | non-urgent alert type 0 |
| 0001 | non-urgent alert type 1 |
| 0010 | non-urgent alert type 2 |
| 0011 | non-urgent alert type 3 |
| 0100 | non-urgent alert type 4 |
| 0101 | non-urgent alert type 5 |
| 0110 | non-urgent alert type 6 |
| 0111 | non-urgent alert type 7 |
| 1000 | urgent alert type 0 |
| 1001 | urgent alert type 1 |
| 1010 | urgent alert type 2 |
| 1011 | urgent alert type 3 |
| 1100 | urgent alert type 4 |
| 1101 | urgent alert type 5 |
| 1110 | urgent alert type 6 |
| 1111 | urgent alert type 7 |

Table 28. Alert type index

## CMW for remote programming

When the pager receives the remote programming message, the W93910 will program the internal remote programming addresses automatically, and will also inform the μC by sending out the received message. For remote programming, the cm3–cm0 of CMW is equal to 1010, the f1–f0 and ain3–ain0 of CMD, and rd17–rd0 of MDW will send out the received programming message to μC as shown below.

| ain3–0 of CMW | rd17–rd0 definition in MDW | Programmable function |
|---|---|---|
| 0001 | RIA17–RIA0 | Initial Address |
| 0010 | RPA5–RPA0 + 12 dummy '"0" | Paging Area |
| 0100 | RZC3 + RCC7 + ROP3 + 5 dummy "0" | OPID |
| 1000 | SM5 + HNL3 + 12 dummy "0" | Home receiver battery saving |
| 0111 | SM5 + ENL3 + 12 dummy "0" | External receiver battery saving |

Table 29. Remote programming MDW format only

| f1–f0 | Function description |
|---|---|
| 00 | Add RIA, RPA, ROPID or replace SM |
| 01 | Remove RIA, RIA, ROPID |
| 10 | Restore SM, ENL, HNL to Table 1 |
| 11 | Reserve |

Table 30. Remote programming MDW format only

### AIW Definition

| AIW | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| byte3 | 0 | 1 | 0 | cs4 | cs3 | cs2 | cs1 | cs0 |
| byte2 | lc15 | lc14 | lc13 | lc12 | lc11 | lc10 | lc9 | lc8 |
| byte1 | lc7 | lc6 | lc5 | lc4 | lc3 | lc2 | lc1 | lc0 |

Table 31. AIW format

The AIW is only available for long message (cm3–cm0 = 1000,1001,1101,1110) or changing character set (cm3–cm0 = 1111), otherwise it's absent. The cs4–0 indicate character set and lc15–lc0 indicate link counter. The different formats of AIW for the four different types of long message and changing character set are listed in **Summary of Data Output Format**

Each long message is divided into many submessages. The first submessage (cm3–cm0 = 1000 or 1110) must be transmitted first, then other submessages follow in sequence. Each submessage has its own link counter lc15–lc0, which indicates how many message bits remain to be transmitted. The ter flag is defined to indicate the end of the long message as shown in Table 28. When ter flag is 1, it means the long message is completed. Otherwise, it means there are still some other submessages in the coming signal.

For a long message, the W93910 will store all the received submessages including the EOM and filler bits in MDW and then send to UC. The filler bits and EOM are the last message part of MDW group, MDW1, MDW2...MDWn, and need to be removed to construct the long message. The following equation shows how many message bits of the previous MDW group need to be truncated. The long message can then be reproduced by connecting all the submessages except the truncated parts.

No. of message bits needing to be truncated in previous MDW group

= Total message bits of previous MDW group - [ $(lc15–lc0)_{previous}$ - $(lc15–lc0)_{current}$ ]

| ter flag in EDW | Status |
|---|---|
| ter = 1 | long message is completed |
| ter = 0 | long message is not completed |

Table 32. ter flag of EDW for long message

### MDW Definition

The received paging message will be output as MDW1, MDW2 ....MDWn format (MDW group). md17–md0 are the actual paging message data resolved from the message partition, including terminator character EOM and any dummy bit such as a filler. For any submessage of a long message, µC needs to use AIW's lc15–lc0 to truncate terminator or dummy bit from md17–md0 according to AIW description. While remote programming, rd17–rd0 is used for remote programming data only. RPI is the remote programming index received from system. This bit should be loaded into b147 of option bit during the re-initialization stage if the remote address is programmed.

| MDW | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| byte3 | 0 | 1 | 1 | 0 | md17/ rd17 | md16/ rd16 | md15/ rd15 | md14/ rd14 |
| byte2 | md13/ rd13 | md12/ rd12 | md11/ rd11 | md10/ rd10 | md9/ rd9 | md8/ rd8 | md7/ rd7 | md6/ rd6 |
| byte1 | md5/rd5 | md4/rd4 | md3/rd3 | md2/rd2 | md1/rd1 | md0/rd0 | er1 | RPI |

Table 33. MDW format

### MDW Description

| BIT | FUNCTION |
|---|---|
| md17–md0 (normal message) | Available paging message |
| rd17–rd0 (remote programming) | Remote programming data only |
| er1 | set to 1 if the random error can't be corrected in this message word |
| rsv | don't care, reserved for future |

Table 34. MDW bit description

Any paging message such as 7 bit alphanumeric, 4 numeric or transparent data will be placed continuously in the 18 bit information field, md17–md0. After the last character (or bit) of message the following message termination procedures shall be used:

- Alphanumeric: an EOM character (0010001) shall be appended;
- Numeric: no terminating character required;
- Transparent data: a single bit set to one shall be appended;

Unused bit in message shall be set as the following default values:

- Alphanumeric: EOM character and partial EOM character (MSB used first) shall be repeated to fill the remaining bits;
- Numeric: space character and partial space character ( MSB used first ) shall be repeated to fill the remaining bits;
- Transparent data: binary zeros shall be used to fill the remaining bits;

The bit mapping in MDW unit for numeric and 7 bit alphanumeric are as follows.

For numeric format, bit17–14 of MDW0 construct the first numeric, bit13–10 are the second... bit1–0 of MDW0 and bit17–16 of MDW1 are the fifth numeric.... Therefore, two MDWs will construct 9 numeric.

For 7 bit alphanumeric format, bit17–11 of MDW0 construct the first character, bit10–4 of MDW0 are the second character, bit 3–0 of MDW0 and bit17–15 of MDW1 are the third character... The alphanumeric definition is depended on Character Set (C.S.). The default C.S. is 00000.

### EDW Definition

The EDW will follow the last MDW while the paging message is completed. Normally, the ter flag is "0" except in a long message completion situation. For any submessage of a long message except the last one, the ter flag of EDW is "0". Only when the long message is completed will the ter flag of EDW be "1". There is some other system information in byte2 of EDW such as eti flag, bai flag and current cycle number, cy5–cy0. The ch3–0 of byte3 indicate which frequency channel the current paging message is caught from and the bn3–bn0 of byte3 indicate which batch the message is completed in.

| EDW | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| byte3 | 1 | 1 | 1 | 0 | 0 | ter | epa | etm |
| byte2 | eti | bai | cy5 | cy4 | cy3 | cy2 | cy1 | cy0 |
| byte1 | bn3 | bn2 | bn1 | bn0 | ch3 | ch2 | ch1 | ch0 |

Table 35. EDW format

### EDW description:

| BIT | FUNCTION |
|---|---|
| ter | set to "1" while current long message is completed, otherwise ter flag is "0" for any individual call or submessage. |
| epa | set to "1" if paging message searching is stopped due to PA inconsistency |
| etm | set to "1" if paging message searching is stopped due to 12 sec time out |
| cy5–cy0 | cycle number from 0(000000) –59(111011) as minute index. |
| eti | External Traffic indicator in SI field |
| bai | Border Area Indicator flag in SI field |

Table 36. EDW description

## Summary of Data Output Format

| message type (cm3–0) | byte | SIW (D23–D0) | CMW (D23–D0) | AIW (D23–D0) | MDW (D23–D0) | EDW (D23–D0) |
|---|---|---|---|---|---|---|
| **Individual** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | X | 0110 md17–md14 | 1110 0 ter epa etm |
| 0000 | 2 | s13–s6 | eb g1 g0 mn4–mn0 | X | md13–md6 | eti bai cy5–cy0 |
| | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | X | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |
| 0XXX(Reserved) | | | | | | |
| **Long w/o C.S.** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | 010 xxxxx | 0110 md17–md14 | 1110 0 ter epa etm |
| **(First submessage)** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | lc15–lc8 | md13–md6 | eti bai cy5–cy0 |
| 1000 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | lc7–lc0 | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |
| **Long w/o C.S.** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | 010 xxxxx | 0110 md17–md14 | 1110 0 ter epa etm |
| **(Other submessages)** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | lc15–lc8 | md13–md6 | eti bai cy5–cy0 |
| 1001 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | lc7–lc0 | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |
| **Remote** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | X | 0110 md17–md14 | 1110 0 ter epa etm |
| **Programming** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | X | **rd13–rd6** | eti bai cy5–cy0 |
| 1010 | 1 | s5–s0 0 0 | 0 0 **f1–f0 ain3–ain0** | X | **rd5–rd0** er1 rsv | bn3–bn0 ch3–ch0 |
| 1011(reserved) | | | | | | |
| **Retransmit** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | X | 0110 md17–md14 | 1110 0 ter epa etm |
| **Latest msg no** | 2 | s13–s6 | eb g1 g0 mn4~mn0 | X | md13–md6 | eti bai cy5–cy0 |
| 1100 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | X | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |
| **Long with C.S.** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | 010 cs5–cs0 | 0110 md17–md14 | 1110 0 ter epa etm |
| **(First submessage)** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | lc15–lc8 | md13–md6 | eti bai cy5–cy0 |
| 1101 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | lc7~lc0 | md5~md0 er1 rsv | bn3–bn0 ch3–ch0 |
| **Long with C.S.** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | 010 cs5–cs0 | 0110 md17–md14 | 1110 0 ter epa etm |
| **(Other submessages)** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | lc15–lc8 | md13–md6 | eti bai cy5–cy0 |
| 1110 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | lc7–lc0 | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |
| **Change** | 3 | 0000 fsi sn2–sn0 | 0010 **cm3–cm0** | 010 cs5–cs0 | 0110 md17–md14 | 1110 0 ter epa etm |
| **Character Set** | 2 | s13–s6 | eb g1 g0 mn4–mn0 | xxxx xxxx | md13–md6 | eti bai cy5–cy0 |
| 1111 | 1 | s5–s0 0 0 | 0 0 pc1–pc0 ain3–ain0 | xxxx xxxx | md5–md0 er1 rsv | bn3–bn0 ch3–ch0 |

Table 37. MDATA output summary

Note: where "x" means don't care

## LED CONTROL

LEDO will output a frequency while ENLED is in high level. The LEDO output frequency is selected by option bit LEDF and PLEN condition as described in table 38. When the LEDF is set to 1, the TCTL1 and TCTL2 control pin will also be activated to output the control signal. The TCTL1 and TCTL2 timing is shown in figure 3.

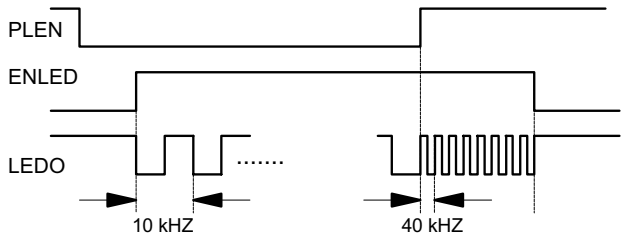



Figure 13. LEDO Timing

| OPTION BIT AND PLEN PIN | | FUNCTION |
|---|---|---|
| LEDF | PLEN Status | LEDO output frequency |
| 0 | inactive | 4 kHz |
| 0 | active | 16 kHz |
| 1 | inactive | 10 kHZ |
| 1 | active | 40 kHZ |

Table 38. LED option bit

## RESET CONDITION

The W93910 has two reset conditions.

### Power on & XRST active

- Reset all 192 option bits and all remote programming registers
- RFEN, PLEN, QC1, QC2, LOCK, MSGVAL, MCLK, MDATA in non-active state

### ON pin rising edge is occurred

- Oscillator start oscillation
- Reset channel number to CH3–CH0 of the 192 option bits
- The values of remote programming registers is not changed

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply Voltage to Ground Potential | -0.3 to +7.0 | V |
| Applied Input/Output Voltage | -0.3 to +7.0 | V |
| Power Dissipation | 120 | mW |
| Ambient Operating Temperature | -20 to +70 | °C |
| Storage temperature | -55 to +155 | °C |

Note: The device should be operated under the above conditions. Operation beyond these conditions may result in permanent damage to the device.

## DC/AC ELECTRONIC CHARACTERISTICS

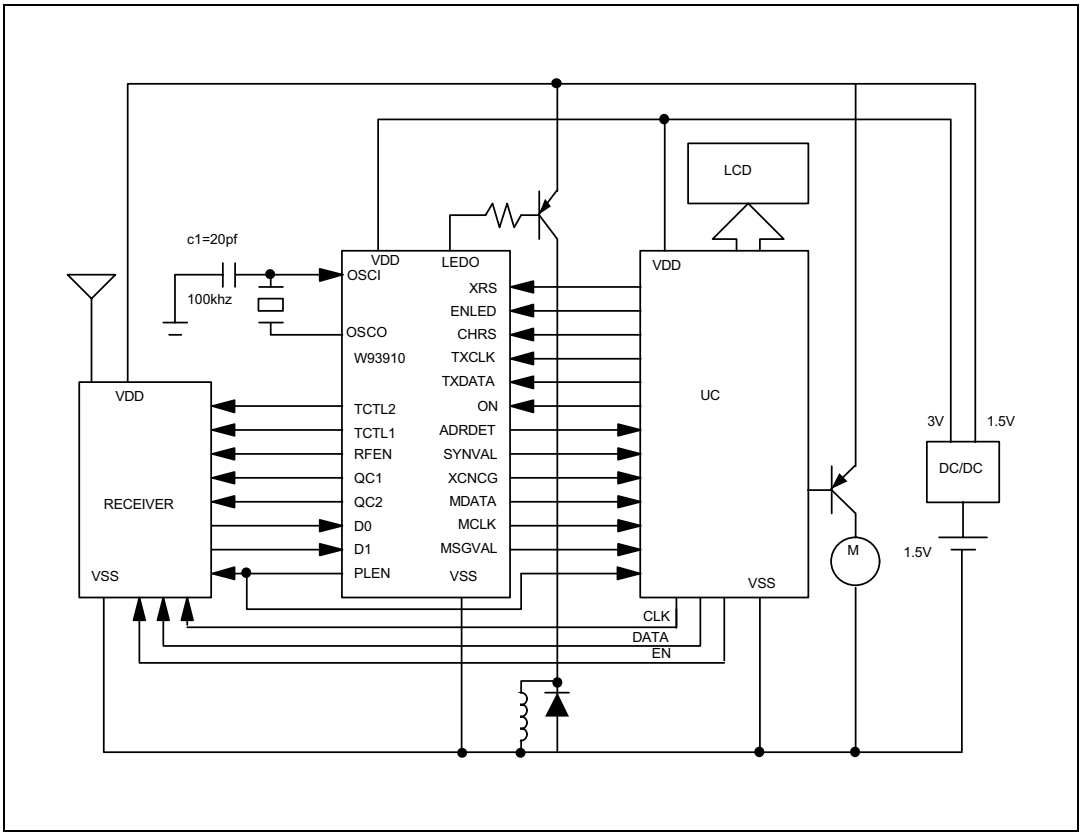
($V_{DD}$ = 3 volt, Fosc = 100 kHz, Ta = 25° C )

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| VDD | Operating Voltage | | 2.5 | 3 | 3.5 | V | |
| IOP | Operating Current | $V_{DD}$ = 3 volt | | 25 | 100 | µA | |
| ISB | Stand By current | ON = 0 volt | | 1 | 2 | µA | |
| VOH | Output high voltage | | 2.4 | | | V | |
| VOL | Output Low voltage | | | | 0.4 | V | |
| VIH | Input high voltage | | 2 | | | V | |
| VIL | Input low voltage | | | | 0.8 | V | |
| IOH | Output High Current | VO = 2.1 volt | 500 | | | µA | |
| IOL | Output Low Current | VO = 0.4 volt | 500 | | | µA | |
| TCHRS | CHRS Active Width | | 1 | | | µS | |
| TXCNCG | XCNCG Active Width | | 4 | | 4.5 | mS | |
| TTXCK | TXCLK Period | | 1 | | | µS | |
| TTDST | TXDATA Setup Time | | 20 | | | nS | |
| TTDHD | TXDATA Hold Time | | 20 | | | nS | |
| TOSC | OSCO Stable Time | | | | 1 | S | |
| TXRST | XRST Active Width | | 10 | | | µS | |
| TPG | Programming setup | | 1 | | | µS | |
| TON | TXCLK to ON delay | | 3 | | | Txclk | |

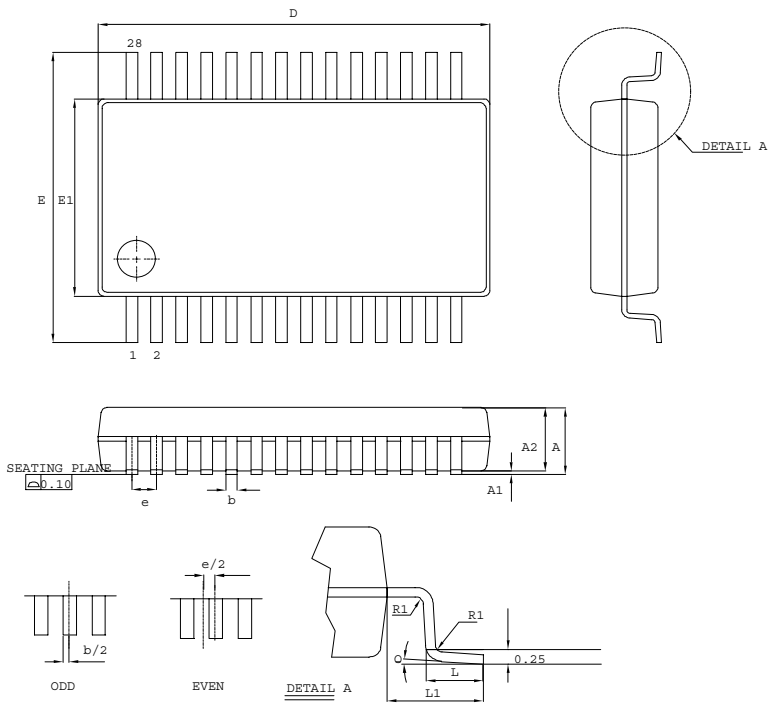
DC/AC Electronic Charac, continued

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| TOP | ON active to PLEN active delay | | | 4 | | S | |
| TADDT | ADRDET active to MCLK active | | 45 | | | mS | |
| TMSGV | MSGAVL active to MCLK active | | | 700 | | µS | |
| TMCLK | MCLK Period | MCK1–0 = 00 | | 80 | | µS | |
| | | MCK1–0 = 01 | | 40 | | µS | |
| | | MCK1–0 = 10 | | 20 | | µS | |
| | | MCK1–0 = 11 | | 5 | | µS | |
| TMDST | MDATA Setup Time | MCLK active edge | 1/4 | | | Tmclk | |
| TMDHD | MDATA Hold Time | MCLK active edge | 1/4 | | | Tmclk | |
| TPLST | PLEN Pre-Active Time | PL1–0 = 00 | | 9.6 | | mS | |
| | | PL1–0 = 01 | | 19.2 | | mS | |
| | | PL1–0 = 10 | | 28.8 | | mS | |
| | | PL1–0 = 11 | | 38 | | mS | |
| TRFDY | RFEN Delay to Preamble | RFON = 0 | | 4.8 | | mS | |
| | | RFON = 1 | | 9.6 | | mS | |
| TQC1W | QC1 Active Width | QC1WTH = 0 | 2.5 | | | mS | |
| | | QC1WTH = 1 | 3.8 | | | mS | |
| TUNIT | MDATA D23 to Next unit D23 | | 4 | | | mS | |
| TUDI | MCLK Stop Clock per byte | MCK1–0 = 11<br>UDI1–0 = 11 | 1.2 | | 1.3 | mS | |
| TINT | MDATA D0 Delay to Next D23 | MCK1–0 = 00<br>UDI1–0 = 00 | 2 | | 2.1 | mS | |

## TYPICAL APPLICATION CIRCUIT



## Package Information




| Symbol | Common Dimension (Millimeters) | | | Common Dimension (Inches) | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | | | 2.0 | | | 0.079 |
| A1 | 0.05 | | | 0.002 | | |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | | 0.38 | 0.009 | | 0.015 |
| D | 9.9 | 10.2 | 10.5 | 0.390 | 0.401 | 0.413 |
| E | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| E1 | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| e | | 0.65 | | | 0.0256 | |
| L | 0.55 | 0.75 | 0.95 | 0.021 | 0.030 | 0.037 |
| L1 | | 1.25 | | | 0.050 | |
| R1 | 0.09 | | | 0.004 | | |
| O | 0 | 4 | 8 | 0 | 4 | 8 |

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