CALLING LINE FSK INDENTIFIER

Table of Contens-

GENERAL DESCRIPTION

The Winbond Caller Identification device W91040 is a low power CMOS integrated circuit used to receive physical layer signals transmitted according to Bellcore specifications. The W91040 device provides the features and functions of the Caller Identification specification in on-hook calling with caller ID message includes FSK demodulation and ring detection. The FSK demodulation function can demodulate FSK signal of the Bell 202 and CCITT V.23 Frequency Shift Key-in (FSK) with 1200 baud rate. The ring signal for Bellcore can be detected by ring detector.

The operation mode of the W91040 is DL-mode and UP-mode. The DL-mode is used to interface with the dialer and LCD controller W91C570 device. It can be used on the feature phones for extracting and displaying date/time and telephone number during Bellcore on-hook caller ID data receive. The UP-mode is micro controller based, fully caller ID message can be extracted and interpreted by micro controller. Micro controller should not take care of the caller ID timing sequence of Bellcore on-hook.

The W91040 can be waked up itself by the detection of ring automatically and can be power down itself if the caller ID message has been extracted or the data format is incorrect or even if no FSK signal arriveral. If external bandpass filter is used to detect alerting signal, the W91040 can be waked up by micro controller to detect and demodulate the FSK signal and then extract the caller ID message.

FEATURES AND APPLICATIONS

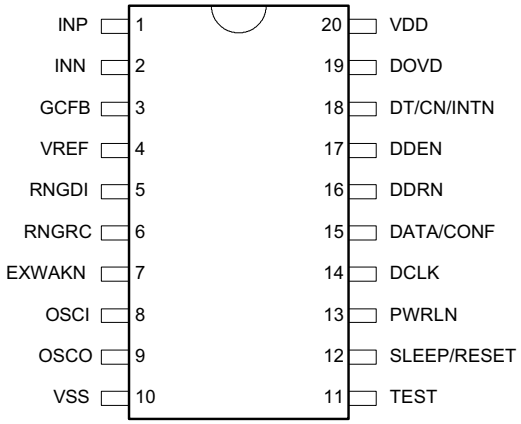
Features

- Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476, U.K. Cable Communications Association (CCA) specification
- Ring and line reversal detection
- BELL 202 and CCITT V.23 FSK demodulation with 1200 baud rate
- Use 3.579545 MHz crystal or ceramic resonator
- Low power CMOS technology with sleep mode
- Automatical power up and power down control
- External power up and power down feature provided
- Power low detection circuit provided
- High input sensitivity
- Input gain adjustable amplifier
- DL-mode (dialer interface mode) or UP-mode (micro controller interface mode) of operation modes
- Automatical process Bellcore on-hook caller ID timing sequence
- Extract valid caller ID message automatically in UP-mode
- Converted data of date/time and calling/called number output in DL-mode
- Internal check sum and error check operation
- External power supplier input for digital data and status output with level shifting
- All of packaged are 20-pin 300 mil either DIP or SOP

Applications

- Bellcore Calling Identity Delivery (CID) and CCA CLIP systems
- Feature phones with or without micro controller
- Phone set adjunct boxes
- FAX and answering machines
- Data base telephone system and Computer Telephony Integration (CTI) systems

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	INP	I	Non-inverting Input of the gain control op-amp.
2	INN	I	Inverting Input of the gain control op-amp.
3	GCFB	O	Op-amp Feed-back Gain Control signal. Set the input gain by connecting this pin and INN pin with feed-back resistor. It is recommended that the op-amp be set to unity gain.
4	VREF	O	Reference Voltage. Nominally $V_{DD}/2$ is used to bias the input of the gain control op-amp.

Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
5	RNGDI	I	Ring Detect Input (Schmitt trigger input). Used for ring detection and line reversal detection. The device will update the status of power low detection and will not wake up during line reversal. Must maintain a voltage between VDD and VSS.
6	RNGRC	O	Ring RC (Open drain output and schmitt trigger input). Used to set the time interval from the end of RNGDI pin to the start of the internal wake up trigger, the operation mode also configured during this pin is low. An external resistor must connected to VDD and capacitor connected to VSS, the time interval is the RC time constant.
7	EXWAKN	I	External Wake Up (Schmitt trigger input). Used to wake up the device from sleeping mode. This pin must hold low for at least 5 μS and the device will be waked up at the end of the low pulse, please refer to Figure 7-2.
8 9	OSCI, OSCO	I, O	Oscillator Input and Output. A 3.579545 MHz crystal or ceramic resonator should be connected between these two pins. OSCI pin may be driven by an external clock source, OSCO pin should left open or drive another device of the OSCI pin.
10	VSS	I	Power Supply Ground.
11	TEST	I	Test pin. Must be connected to VSS for normal operation.
12	SLEEP/ RESET	I	Sleep or Reset input (Schmitt input). Resets the device or puts the device into a sleep condition. When high, the device will enter a low power state by disabling the gain control op-amp, the oscillator and other internal circuit. The function of RNGDI and RNGRC pins are not affected when the device is in a sleep condition. This pin is also used to reset the internal circuit and must be set low for normal operation.
13	PWRLN	O	Power low detection inverted output. The power low detection circuit detects VDD pin and reflects the status at the end of line reversal, ring or external wake up pulse.
14	DCLK	O	Data Clock for the output interface. Used to latch the valid data at the rising edge.
15	DATA/ CONF	I,O	Data signal output (tri-state output) or Configure input. Uesd to configure the operation mode during ring detection. The device is configured as UP-mode if DATA/CONF = high, configured as DL-mode if DATA/CONF = low. It is driven out when DDEN pin is low. In DL-mode, serial data output according to the date, time or calling/called number. Each character data has 4 bits only and low bit outputs first. In UP-mode, serial data output according to the FSK input demudulated. Each byte data has 8 bits and low bit outputs first.
16	DDRN	O	Data Ready, is an inverted output pin. This pin identifies the 4-bit character data boundary in DL-mode or 8-bit data boundary in UP-mode.

Pin Descriptions, continued

PIN	NAME	TYPE*	DESCRIPTION
17	DDEN	O	Data Enable signal (open-drain output in DL-mode or inverted output in UP-mode). When low, it indicates the presence of valid caller ID call is progressing and the DATA pin will be driven out. In DL-mode, this pin is an open-drain output and must pulled high by external resistor or component.
18	DT/CN /INTN	O	Date/Time and Calling/called Number or Interrupt (interrupt is an open drain output). In DL-mode, 8 characters of date and time is transmitting when this pin is high, calling or called number is transmitting when it is low. If check status is outputing, this pin will be low and refer to Figure 7-8. In UP-mode, this pin is used to interrupt the micro controller.
19	DOVD	I	Power supply of digital output pins. This is the power source of the PWRLN, DCLK, DATA, DDRN, DDEN and DT/CN pins.
20	V_{DD}	I	+5V Power Supply input.

SYSTEM DIAGRAM

DL-mode:

When DATA/CONF pin = low, the W91040 is in dialer mode (DL-mode), these pins of DDEN, DDRN, DATA, DCLK and DT/CN are used to interface with the W91C570 device. This system can be used on the feature phones for extracting and displaying date/time and telephone number during Bellcore on-hook. Figure 5-1 shows the system diagram of W91040 in DL-mode and the W91040 extracted and converted the date/time and calling/called number to the W91C570 device, the system can be easily to implement in Bellcore on-hook state.

UP-mode:

When DATA/CONF pin = high, the W91040 in UP-mode is for micro controller based, fully caller ID message can be extracted and interpreted by the micro controller. If another alert detector is used, the device can be waked up by the alert tone through micro controller. The micro controller based caller ID system illustrates in Figure 5-2.

System Diagram, continued

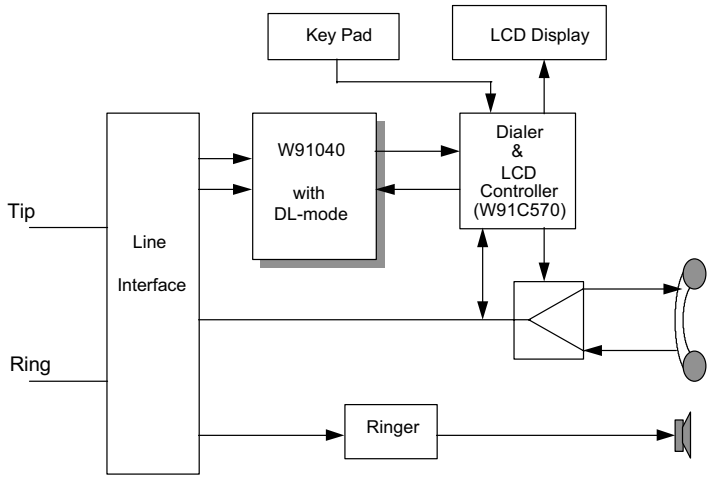


Figure 5-1. System Diagram of W91040 with Dialer IC Interface

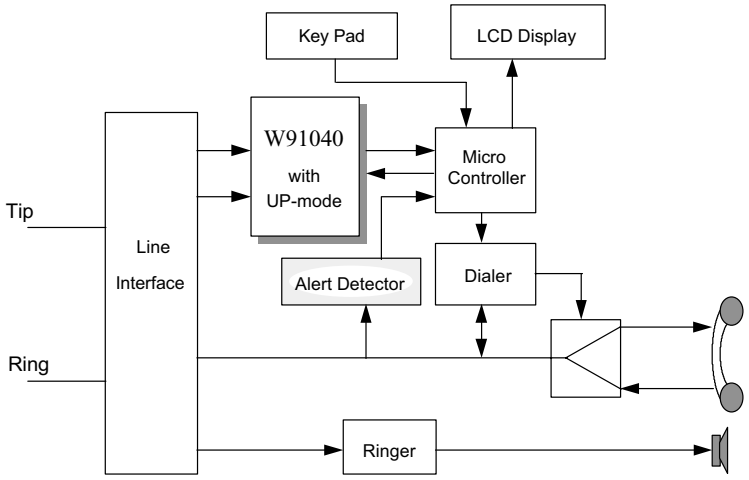


Figure 5-2. System Diagram of W91040 with Micro Controller Interface

BLOCK DIAGRAM

Figure 6-1 illustrates the functional blocks of the W91040 device.

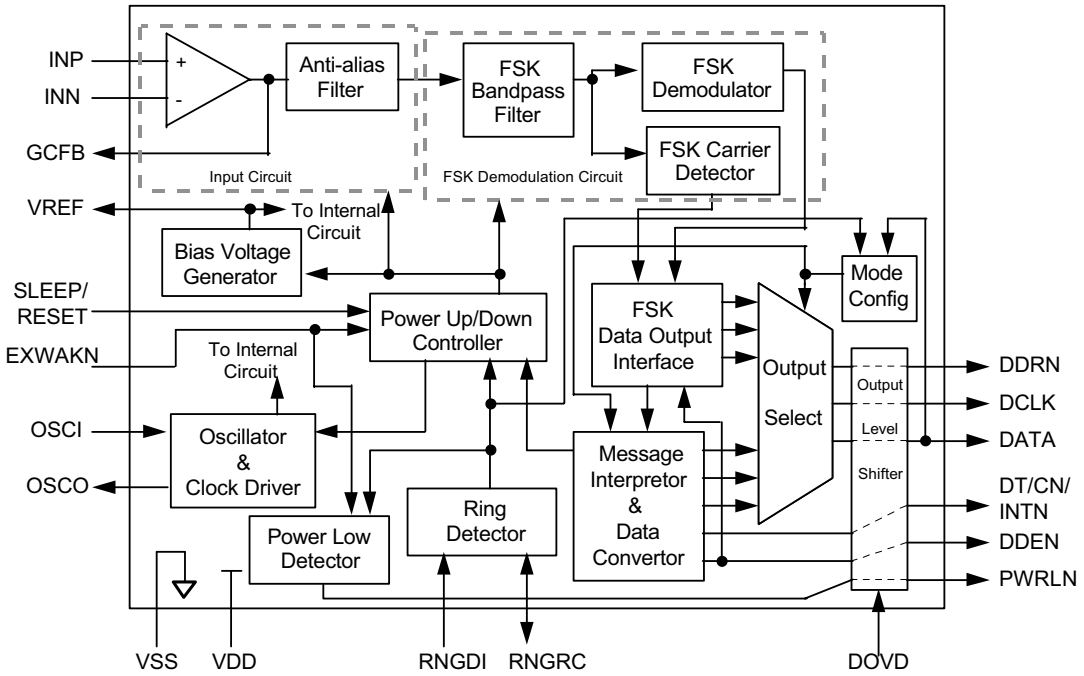


Figure 6. The Block Diagram of W91040 Device

FUNCTIONAL DESCRIPTIONS

Wake Up and Power Control

The device will be waked up itself after the ring had been detected. It will be sleep again when the DDEN pin becomes inactive or the FSK signal doesn't detected any message within 1.5 second. If the SLEEP pin sets to high, the device never wake up even if the the ring had been detected. Figure 7-1 illustrates the related timing waveform of ring, wake up and calling message received for Bellcore on-hook data transmission, the DDEN will held for 40 mS when in DL-mode and the data has been extracted if no error occurs. Another wake up command comes from EXWAKN pin, a low pulse on the EXWAKN pin will force the device to wake up at the end of the pulse, and the device will sleep again when the DDEN pin becomes inactive or the FSK signal does not detected for 1.5 second. The timing shows on the Figure 7-2.

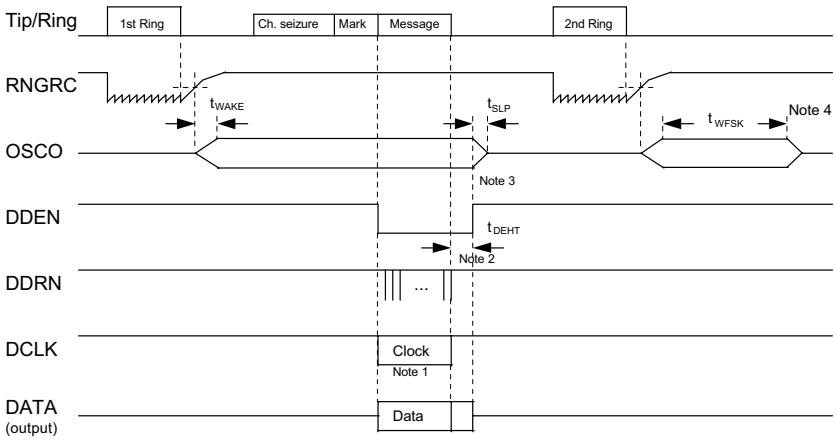


Figure 7-1. Input and Output Timing for Bellcore On-hook Data Transmission.

Notes:

1. The output waveform of DDRN, DCLK and DATA according to the operation mode of W91040.
2. The t_{DEHT} is about 40 mS if the device is in DL-mode and the data has been extracted with no error.
3. The device will be sleep when the DDEN pin becomes inactive.
4. The device also will be sleep when a ring with no FSK data transmission. The t_{WFSK} is about 1.5 sec.

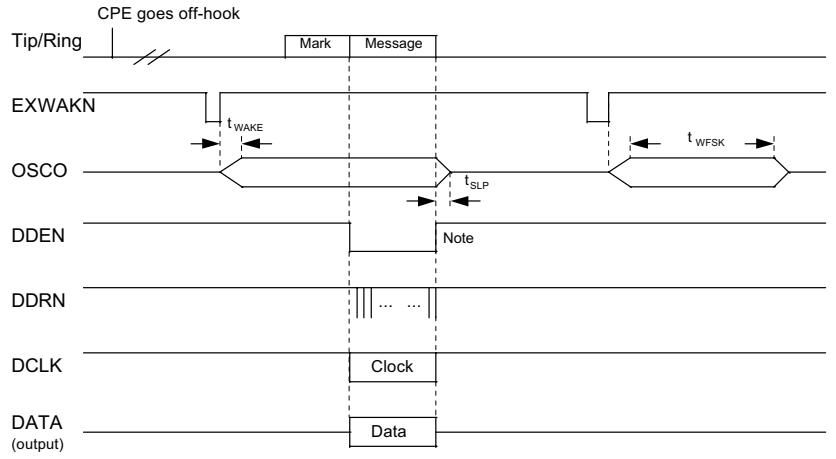


Figure 7-2. Input and Output Timing of external Wake Up Command

Note: The DDEN will be inactived as soon as the last DDRN pulse is disable if the device is in UP-mode or the data is extracted with error.

Ring Detection

The application circuit in Figure 7-3 illustrates the relationship between the RNGDI and RNGRC signals. The two pins combination is used to detect an increase of RNGDI voltage from ground to above the Schmitt trigger high going threshold voltage VT+.

The Schmitt trigger buffered input from RNGDI and RNGRC pins are uesd to detect line reversal and ring, the device will update the status of the power low detection and will not waked up if line reversal has been detected.

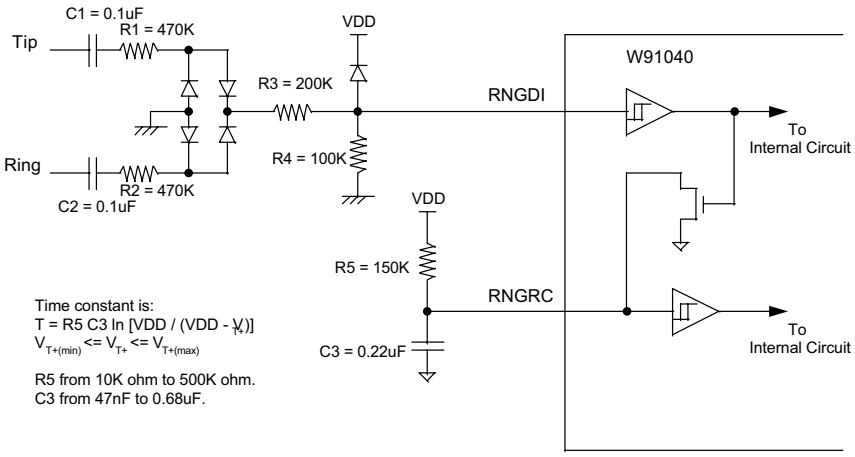


Figure 7-3. Application Circuit of Ring Detector

The RC time constant of RNGRC pin is used to delayed the internal signal pulse for a low going edge on the RNGDI pin. The RNGDI low going edge goes from above the VT+ voltage to the Schmitt trigger low going threshold voltage VT-. The RC time constant is the time constant of capacitor charge from V_{SS} through the VT+ voltage to V_{DD}, it must greater than the maximum period of the ring signal, to ensure a minimum low interval and to filter the ring signal to get an envelope output.

The diode bridge shown in Figure 7-3 is used to balance ringing for both ended of tip and ring line. The R1 and R2 are used to set the maximum loading and must be of equal value to achive balance loading at both tip and ring line. R1, R3 and R4 form a resistor divider to supply a reduced voltage to the RNGDI input. The attenuate value is determined by the detecting of minimal ring voltage and maximum noise tolerance between tip/ring and ground.

FSK Analog Input

The input signal is processed by input circuit to added the bias voltage and to adjust the input amplitude and to filter out the unwanted frequency. The gain control op-amp is used to bias the input voltage with the VREF signal voltage, VREF is $V_{DD}/2$ typically. It also used to select the input gain by connecting a feed-back resistor between this pin and the INN pin. Figure 7-4 shows the necessary connections with tip/ring line inputs. In a single-ended configuration, the gain control op-amp is connected as shown in Figure 7-5.

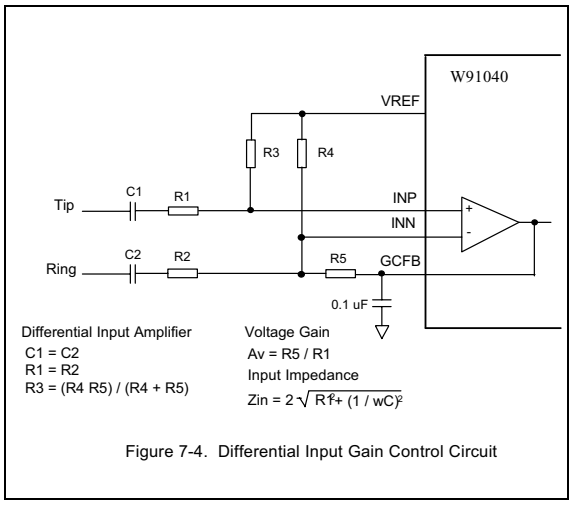


Figure 7-4. Differential Input Gain Control Circuit

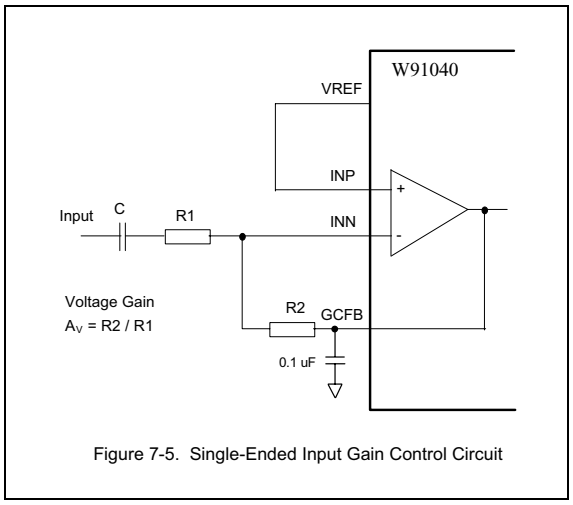


Figure 7-5. Single-Ended Input Gain Control Circuit

Message Interprete

The Bellcore on-hook data transmission format on the FSK signal is shown in the Figure 7-6. The channel seizure is 01010101..., mark and space alternates on the FSK signal, and will be omitted by the W91040 device. The mark signal continues for at least 45 mS. The data follows mark signal is the data package, may be Single Data Message Format (SDMF) or Multiple Data Message Format (MDMF). The first byte of the data package is called message type of the caller ID message and the current valid message type is 80H, 82H, 04H and 06H. 80H is Multiple Data Message Format, 82H is message waiting of Multiple Data Message Format, 04H is Single Data Message Format and 06H is message waiting of Single Data Message Format. The data type of message body or parameter body is represented the same as ASCII code.

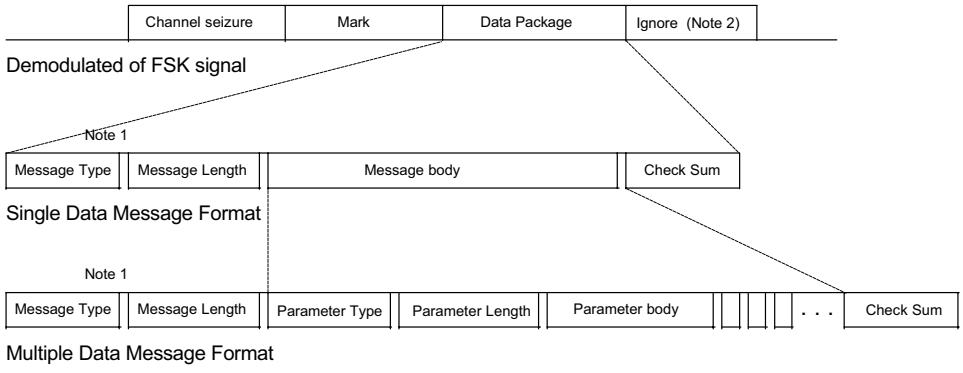


Figure 7-6. Data Transmission of FSK Signal

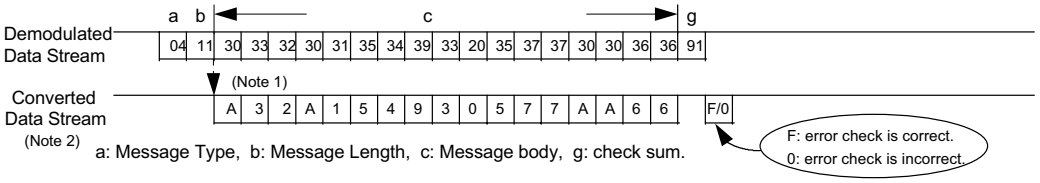
Notes:

1. Bellcore specified that up to 20 bits of mark may be inserted between message (parameter) type and message (parameter) length or message (parameter) length and message (parameter) body or message (parameter) body and check sum.
2. May be exist or not depends on the central office or the quality of the telephone channel.

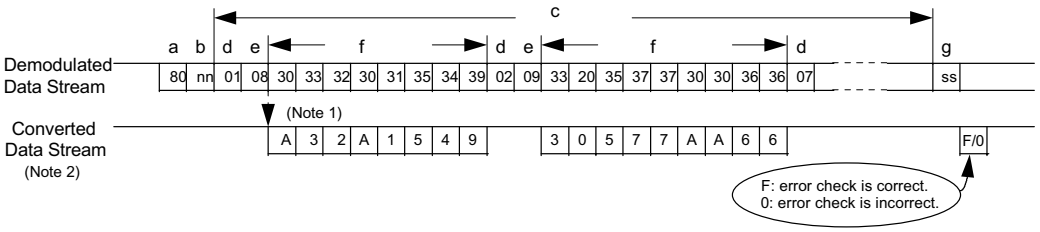
The W91040 will be waked up itself after the ring had been detected. If the FSK signal has been detected and if the message interpreter is enabled, the message interpreter is waiting for at least 40 mS of the mark signal and then read and check the first byte (message type) of the data. If the data of the message type is 1000xxxxB (8XH) or 0000xxxxB (0XH), DDEN pin will be low and DCLK, DATA and DDRN will be activated according to the operation mode of the W91040 functions until the end of FSK data package and the devices will be power down itself. If otherwise of the message type, the W91040 will be power down itself.

Data Extract and Convert (DL-mode only)

The date/time parameter and calling/called number can be extracted by W91040 device if the device is configured as DL-mode by setting DATA/CONF pin to low during ring input. In Single Data Message Format, the accepted data of message type is 00000100B only, the message body contains 8 bytes of date/time parameter and specific bytes of calling number or called number number. In Multiple Data Message Format, the accepted data of message type is 10000000B only, the parameter body contains 8 bytes of date/time parameter if the parameter type is 00000001B and the parameter body contains specific bytes of calling number or called number if the parameter type is 00000010B or 00000011B. The example of data extract and convert for Single Data Message Format and Multiple Data Message Format are shown in Figure 7-7.



Single Data Message Format , (a = 04H, Date: 03/20, Time: 15:49, Tel: 3 5770066)



a: Message Type, b: Message Length, c: Message body, d: Parameter Type, e: Parameter Length, f: Parameter body, g: check sum.

Multiple Data Message Format , (a = 80H, Date: 03/20, Time: 15:49, Tel: 3 5770066)

Figure 7-7. Data Extract and Convert Example of Caller ID Data Package

Notes:

1. The timing delay from demodulated data stream to converted data stream output is not shown.
2. The data conversion refer to the character coding table and as listed below.

The 4-bit data in each character will be transmitted to the dialer IC W91C570. The character coding table is listed as follows:

ORIGINAL DATA	CONVERTED DATA		
BITS 7 6 5 4 3 2 1 0	BITS 3 2 1 0	CHARACTERS	NOTES
x 0 1 1 0 0 0 1	0 0 0 1	1	1, 2
x 0 1 1 0 0 1 0	0 0 1 0	2	1, 2
x 0 1 1 0 0 1 1	0 0 1 1	3	1, 2
x 0 1 1 0 1 0 0	0 1 0 0	4	1, 2
x 0 1 1 0 1 0 1	0 1 0 1	5	1, 2
x 0 1 1 0 1 1 0	0 1 1 0	6	1, 2
x 0 1 1 0 1 1 1	0 1 1 1	7	1, 2
x 0 1 1 1 0 0 0	1 0 0 0	8	1, 2
x 0 1 1 1 0 0 1	1 0 0 1	9	1, 2
x 0 1 1 0 0 0 0	1 0 1 0	0	1
x 1 0 0 1 1 1 1	1 1 0 0	O	1
x 1 0 1 0 0 0 0	1 1 1 0	P	1
x 0 1 0 0 0 0 0	1 1 0 1	"Space"	1
x 0 1 0 1 1 0 1	1 0 1 1	-	1
others	0 0 0 0		3

Notes:

1. Bit 7 of original code is ignore.
2. Ignored the higher 4-bit only.
3. The other codes convert to the "0000" code, the same code as error code of check status.

Date and Time Parameter

There are "Month" field then "Day" field then "Hours" field and then "Minutes" field.

The "Month" field is encoded as two characters, 01 for January, 02 for February and so on until 12 for December.

The "Day" field is encoded as two characters, 01 to 31.

The "Hours" field is encoded in 24-hour time as two characters, 00 to 23.

The "Minutes" field is encoded as two characters, 00 to 59.

Calling Number or Called Number Parameter

The maximum length of calling number or called number is 18 characters. The "P", "O", "space" and "-" codes also included.

Data Output

The W91040 skipps the arrived data of channel seizure, receives and processes the FSK signal and finally appends a check status after the check sum data has been received and checked. The W91040 in DL-mode also extracts and converts the date time and calling/called number according to the character coding table. Figure 7-8 is the timing relation of FSK input signal and output signal of the W91040 in DL-mode and Figure 7-9 is the timing relation of FSK input signal and output signal of the W91040 in UP-mode.

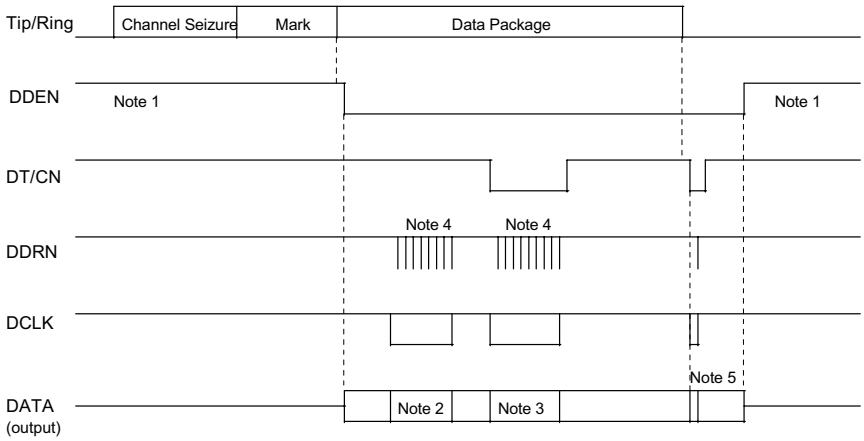


Figure 7-8. Timing Relation of FSK Input Signal and Output Signal of W91040 in DL-mode

Notes:

1. DDEN is pulled high by external resistor or component.
2. The data of this area is the character of date and time parameter.
3. The data of this area is the calling number or called number parameter.
4. If no date/time and or calling/called number present, DDRN signal will not activated at these time interval.
5. Check status appended.

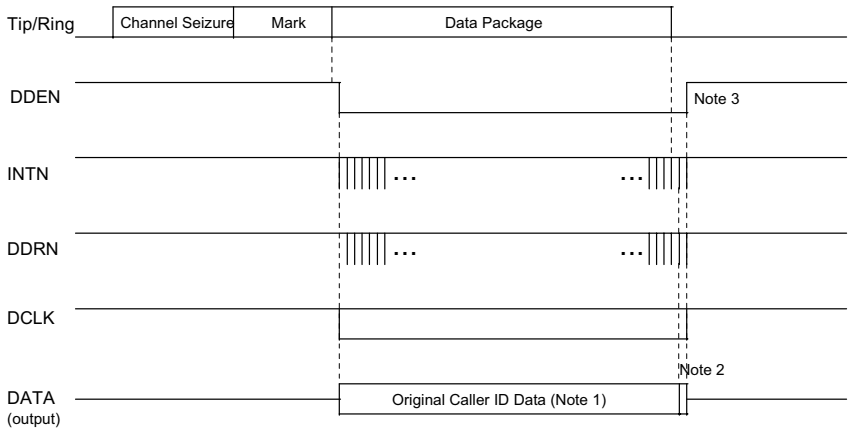


Figure 7-9. Timing Relation of FSK Input Signal and Output Signal of W91040 in UP-mode

Notes:

1. The original caller ID data includes check sum data.
2. Check status appended.
3. The DDEN will be inactived as soon as the last DDRN pulse is disable.

The data is buffered one byte from the demodulated FSK data stream to DATA output for message interpreting and character code converting. Figure 7-10 shows the serial data interface timing from the analog FSK signal to the character data output in DL-mode. Figure 7-11 is the serial data interface timing from the analog FSK signal to the data output in UP-mode.

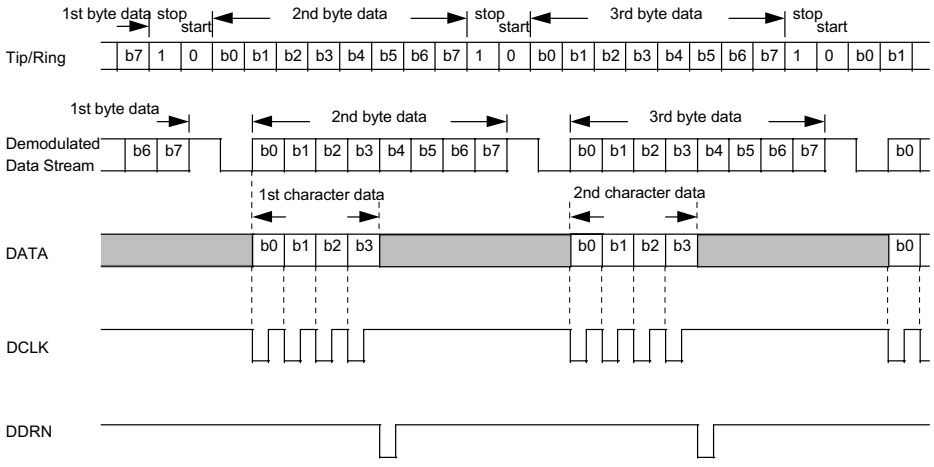


Figure 7-10. Serial Data Interface Timing of Character Data Output in DL-mode

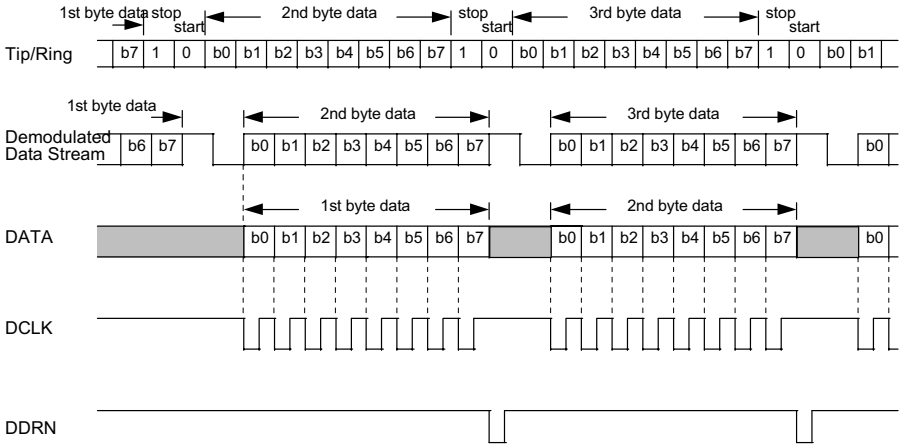


Figure 7-11 Serial Data Interface Timing of Data Output in UP-mode.

Error Check

The error check will proceeded when valid message type has been decoded with DDEN low. The check result will appended on the last byte (in UP-mode) or last 4-bit (in DL-mode) of the series DATA output. The data of check status is 11111111B (or 1111B) if the error check is correct, the data is 00000000B (or 0000B) if the error check is incorrect. The DDEN will be inactive and DATA is set to tri-state as soon as check error occurs. There are four conditions that will introduce check error:

1. Check sum error. If the data of the check sum register is not 0 when the check sum data has been received.
2. Data interruption for at least 40 mS. This condition occurs if the internal FSK demodulated data holds high (mark) or low (space) for at least 40 mS before check sum arrival, the data of input FSK signal after data interruption will be dropped out.
3. Data package is incorrect in Multiple Data Message Format. In Multiple Data Message Format, if the last parameter body does not fit to the message body in Figure 7-7 when check sum data is arrival.

Power Low Detector

The power low detector is used to detect the power voltage on VDD pin. It is enabled during line reversal or ring is detected or external wake up trigger input. The detected status is latched on the PWRLN pin at the end of line reversal, ring or external wake up trigger input and then the detector circuit is disabled. To ensure the detect circuit is enabled, the low pulse of EXWAKN pin must above 5 uS.

Others

Interrupt (UP-mode only)

The INTN pin is used to interrupt the micro controller that a valid caller ID's call is going or the 8-bit data boundary is on the serial data output stream. The micro controller must read the DDRN pin to identify that a new caller ID's call will going if DDRN pin is high or the 8-bit data boundary on the serial data output stream if DDRN pin is low during interrupt occurs. The message type of the valid caller ID's call is 1000xxxxB (8XH) or 0000xxxxB (0XH). The interrupt pulse width is the same as DDRN pulse width. If the INTN is activated with DDRN low, the DDRN will be high before INTN goes to high. Figure 7-12 shows the timing of interrupt, the interrupt pulse width is the same as DDRN pulse width.

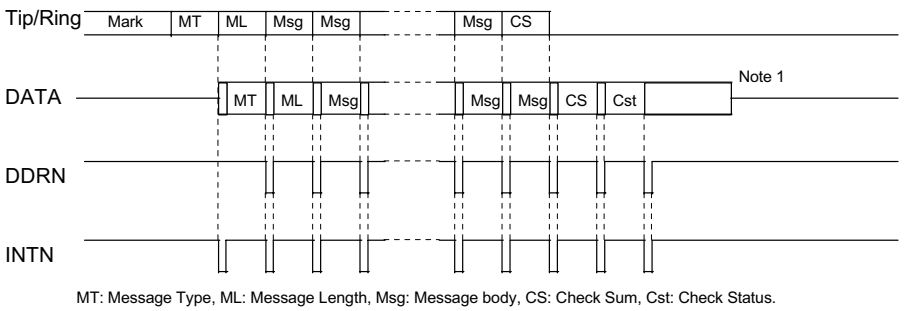


Figure 7-12 Timing of Interrupt Signal During Valid Caller ID Call

Note: The DATA will be tri-state when DDEN is inactive and the waveform of DDEN is not shown.

Crystal Oscillator

The operation frequency of the W91040 is 3.579545 MHz. The crystal osscillator, ceramic resonator or other clock source can be used. The crystal oscillator and ceramic resonator can be connected to the OSCI and OSCO pins without external components. If other clock source is used, the OSCI pin is driven by clock source input and the OSCO pin can be used to drive other external colcked devices or left open.

The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	+/- 0.1 % (-40 °C to +85 °C)
Resonance Mode:	Parallel
Load Capacitance:	18 pF
Maximum Series Resistance:	150 Ω
Maximum Drive Level (mV):	2 mV

Bias Voltage Generator

The bias voltage generator generates low impedance voltage source equal to $V_{DD}/2$ and is used to bias the gain control op-amp. The voltage source is also used for internal circuits. A 0.1 μF capacitor should be connected between VREF pin and V_{SS} to reduce noise.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

(Voltage referenced to V_{SS} pin)

PARAMETER	SYMBOL	RATING	UNITS
Supply Voltage with Respect to V_{SS} (at V_{DD} pin)	V_{DD}	-0.3 to 6	V
Supply Voltage with Respect to V_{SS} (at DOVD pin)	V_{DOVD}	-0.3 to 6	V
Voltage on Any Pin Other Than Supplies (Note 1)		-0.7 to V_{DD} + 0.7	V
Voltage on Any Pin Other Than Supplies (Note 2)		-0.7 to V_{DOVD} + 0.7	V
Current at Any Pin Other Than Supplies		0 to 10	mA
Storage Temperature	T_{ST}	-65 to 150	°C

* Exceeding these values may cause permanent damage.

Notes:

1. V_{DD} +0.7 should not excess maximum rating of supply voltage at V_{DD} pin. PWRLN, DCLK, DATA/CONF, DDRN, DDEN and DT/CN/INTN pins are exclusive.
2. V_{DOVD} +0.7 should not excess maximum rating of supply voltage at DOVD pin, only on the PWRLN, DCLK, DATA/CONF, DDRN, DDEN and DT/CN/INTN pins.

Recommended Operating Conditions

(Voltage referenced to V_{SS} pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supplies	V_{DD}	2.7 to 5.5	V
Power Supplies (digital output interface)	V_{DOVD}	2.0 to 5.5	V
Clock Frequency	f_{OSC}	3.579545	MHz
Tolerance on Clock Frequency	Δf_C	-0.1 to +0.1	%
Operation Temperature	T_{OP}	0 to 75	°C

DC Electrical Characteristics

(Voltage reference to V_{SS} pin and DC electrical characteristics are over recommended operating conditions unless otherwise stated.)

PARAMETER	CONDITION	SYM.	MIN.	TYP*	MAX.	UNITS	TEST/ NOTES
Operating Supply Voltage	Power Supply			2.7	5.0	V	
Standby Supply Current		I_{DDQ}			1	µA	Test 1
Operating Supply Current	V_{DD} = 2.7V	I_{DD1}		1.0	1.5	mA	Test 2
	V_{DD} = 5.0V			2.2	3.0		
Schmitt Input High Threshold	RNGDI, RNGRC	VT+	0.48 V_{DD}		0.68 V_{DD}	V	
Schmitt Input Low Threshold	SLEEP, CONF	VT-	0.28 V_{DD}		0.48 V_{DD}	V	

DC Electrical Characteristics, continued

PARAMETER	CONDITION	SYM.	MIN.	TYP*	MAX.	UNITS	TEST/ NOTES
Schmitt Hysteresis		V_{HYS}	0.2			V	
Output High Sourcing Current	DCLK, DATA, DDRN, DDEN, DT/CN	I_{OH}	0.5			mA	Note 1
Output Low Sinking Current	DCLK, DATA, DDRN, DDEN, DT/CN, RNGRC	I_{OL}	0.5			mA	Note 2
Input Current 1	INP, INN	I_{IN1}			1	µA	Note 3, 5
Input Current 2	RNGDI, SLEEP, CONF	I_{IN2}			10	µA	Note 3, 5
Output High-Z Current	RNGRC	Ioz1			1	µA	Note 4, 5
Output High-Z Current	INTN	Ioz2			10	µA	
Reference Output Voltage	VREF	VRef	0.5 V_{DD} - 4%		0.5 V_{DD} +4%	V	Note 6
Reference Output Resistance	VREF	RRef			2	KΩ	
Power Low Detect Voltage	PWRLN	V_{DET}	2.5	2.6	2.7	V	

Tests:

1. All input pins are V_{DD} or V_{SS} except for oscillator pins. No analog input, output without loading and SLEEP = V_{DD}.
2. All input pins are V_{DD} or V_{SS} except for oscillator pins. No analog input, output without loading, SLEEP = V_{SS}.

Notes:

1. V_{OH} = 0.9 V_{DD}
2. V_{OL} = 0.1 V_{DD}
3. V_{IN} = V_{DD} to V_{SS}.
4. V_{OUT} = V_{DD} to V_{SS}.
5. Magnitude measurement, ignore signs.
6. Output no load.

*: Typical figure are at V_{DD} = 3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

Electrical Characteristics - Gain Control OP-Amplifier

(Electrical characteristics are over recommended operating conditions unless otherwise stated.)

PARAMETER	SYM.	MIN.	TYP*	MAX.	UNITS	TEST CONDITIONS
Input Offset Voltage	V_{OS}			25	mV	
Power Supply Rejection Ratio	PSRR	40			dB	1 KHz 0.1 V_{PP} ripple on V_{DD}
Maximum Capacitive Load (GCFB)	C_L			100	pF	
Maximum Resistive Load (GCFB)	R_L	50			KΩ	

*: Typical figure are at V_{DD} = 3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

AC Electrical Characteristics

(AC electrical characteristics are over recommended operating conditions, unless otherwise stated.)

FSK Detection

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Frequency Detection					Hz	
Bell 202 Mark (logic 1)	fMark	1188	1200	1212		+/- 1 %
Bell 202 Space (logic 0)	fSpace	2178	2200	2222		+/- 1 %
CCITT V.23 Mark (logic 1)	fMark	1280.5	1300	1319.5		+/- 1.5 %
CCITT V.23 Space (logic 0)	fSpace	2068.5	2100	2131.5		+/- 1.5 %
Maximum Input Signal Level				-5.78	dBm[a]	1,3
Input Sensitivity			-45		dBm	1, 3
Transmission Rate		1188	1200	1212	baud	
Input Noise Tolerance	SNRFSK	20			dB	1, 2

a. dBm = decibels with a reference power of 1 mW into 600 ohms, 0 dBm = 0.7746 Vrms.

Notes:

1. Both mark and space have the same amplitude. Both mark and space are at the nominal frequencies.
2. Band limited random noise 300–3400 Hz. Present only when FSK signal is present.
3. These characteristics are at V_{DD} = 3V and temperature = 25 °C

AC Timing Characteristics

(AC timing characteristics are over recommended operating conditions, unless otherwise stated.)

System

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Wake-up Time	SLEEP	t_{WAKE}			50	mS	1, 2
Sleep-down Time	OSCO	t_{SLP}			5	mS	1, 2

Notes 1: May be internal or external SLEEP command signal.

2: Parameter is design guaranteed and not subject to production testing.

Message Interprete

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNITS
Mark Hold Off Time Before Message Type Detected		t_{MRK}	40			mS

Note: Parameter is design guaranteed and not subject to production testing.

Data Output Interface

PARAMETER	CONDITION	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
DDEN Setup Time	DDEN, DCLK	t_{DEST}	0			µS	4
DDEN Hold Time	DDEN, DDRN	t_{DEHT}	40			mS	4, 5
Low Time	DDRN, INTN	t_{RL}	415	416	417	µS	2
Rate	DATA		1188	1200	1212	bpS	1
Input FSK to Internal Data Delay		t_{IDD}		1	5	mS	3, 4
DATA to DCLK Delay	DCLK	t_{DCD}	415	416	417	µS	1, 2
DCLK to Data Delay	DATA	t_{CDD}	415	416	417	µS	1, 2
Frequency	DCLK	f_{DCLK}	1201.6	1202.8	1204	Hz	2
High Time		t_{CH}	415	416	417	µS	2
Low Time		t_{CL}	415	416	417	µS	2
DCLK to FDRN Delay	DCLK, DDRN	t_{CRD}	415	416	417	µS	2

Notes:

1. FSK input data rate at 1200 +/- 12 baud.
2. OSCI frequency at 3.579545 MHz +/- 0.1%.
3. Function of FSK input signal condition.
4. Parameter is design guaranteed and not subject to production testing.
5. This condition presents only if the device is in DL-mode and the data is extracted with no error.

*: Typical figure are at V_{DD} = 3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

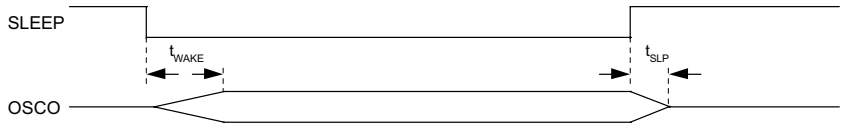


Figure 8-1. Wake up and Sleep Down Timing

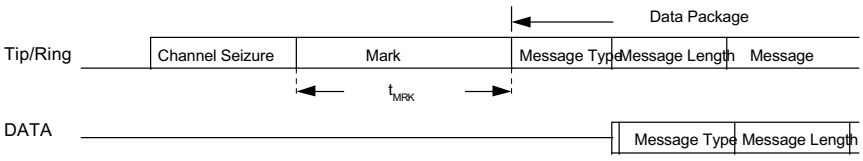


Figure 8-2. Mark Hold of Time Before Message Type

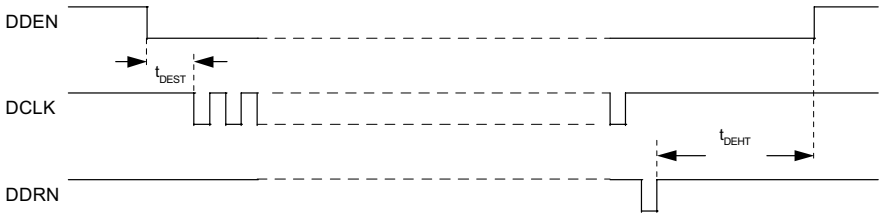


Figure 8-3. Setup Time and Hold Time of DDEN

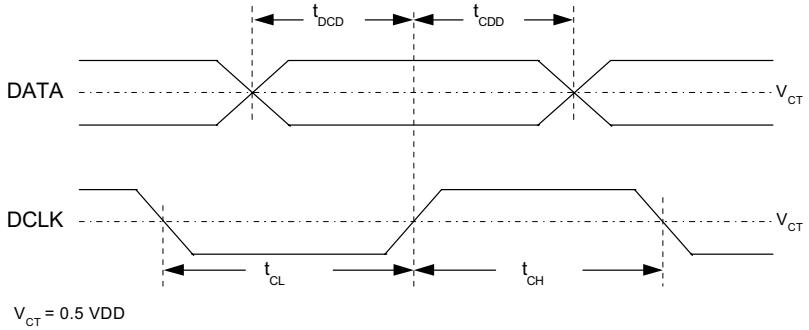


Figure 8-4. DATA and DCLK Output Timing

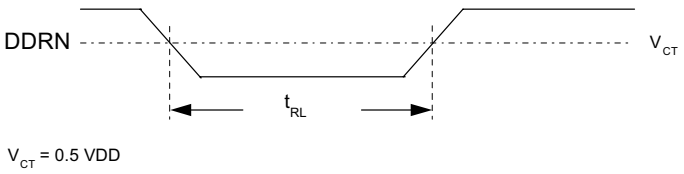


Figure 8-5. DDRN Output Timing

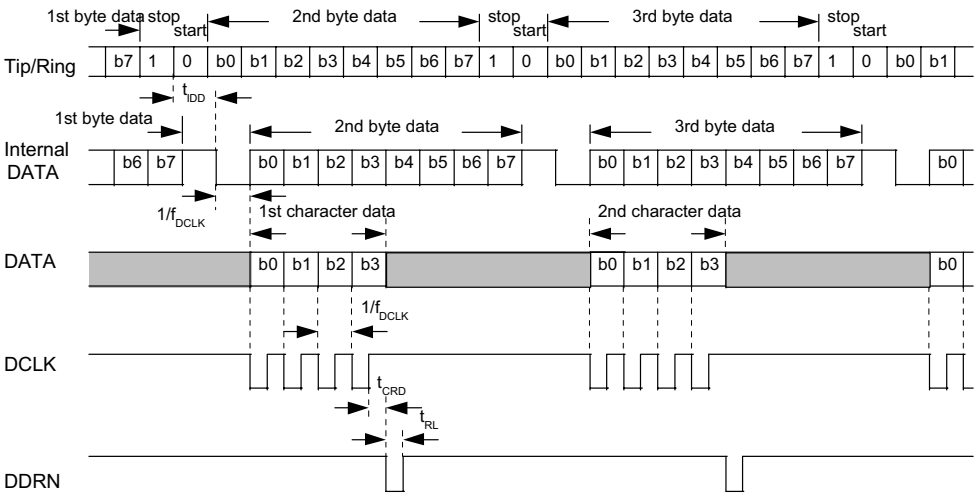
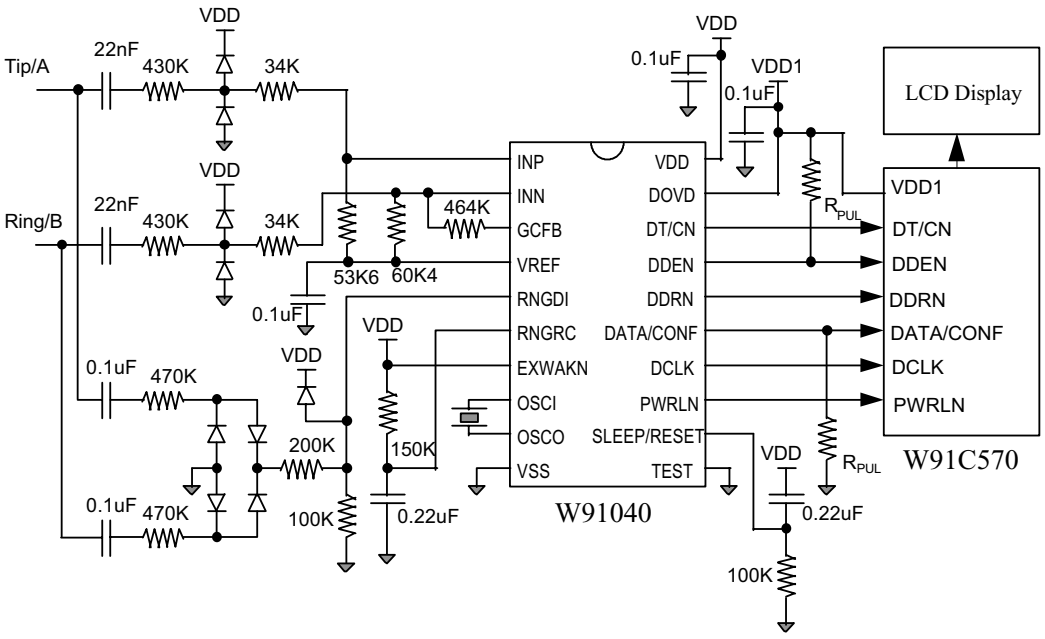


Figure 8-6. Serial Data Interface Timing of Character Data Output

APPLICATION INFORMATION

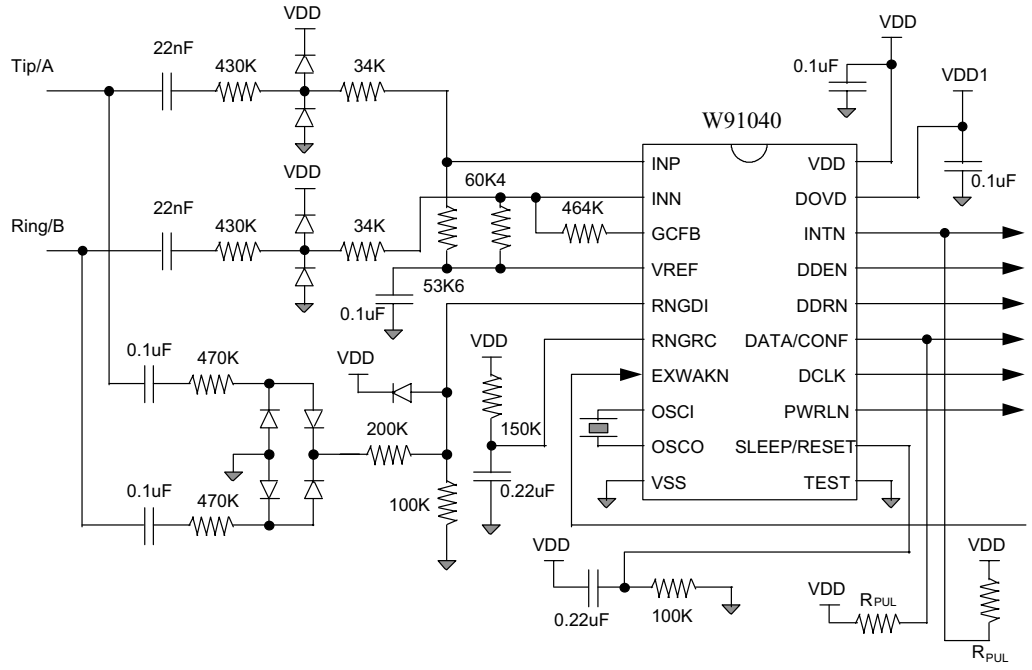
The application circuit of the W91040 is shown in Figure 9-1 and Figure 9-2. The circuit shown in Figure 9-1 illustrates the use of the caller ID device in a typical CPE system with dialer and LCD controller W91C570. It only shows the circuit between the caller ID device and line interface. The gain controller of gain control op-amp is set to unit gain, and the electrical characteristics can be met in this application circuit. The SLEEP pin of the caller ID device in Figure 9-1 is no use and must connected with a capacitor to VDD and a resistor to VSS to get a reset pulse. It should be noted that if glitch with sufficient amplitude on the tip and ring interface, the circuit will detect as line reversal input. Figure 9-2 shows another application circuit of the W91040, the caller ID device is interfaced with micro controller.



R_{PUL} may be 100K to 200K ohm.
Crystal is 3.579545MHz with 0.1% frequency tolerance.

VDD1 may be the same as VDD or not depend on the signal level of data output interface.

Figure 9-1. Application Circuit of W91040 in DL-Mode



R_{PUL} may be 100K to 200K ohm.
Crystal is 3.579545MHz with 0.1% frequency tolerance.

VDD1 may be the same as VDD or not depend on the signal level of data output interface.

Figure 9-2. Another Application Circuit of W91040 in UP-Mode

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