

W81281

**USB Keyboard/
Device Controller**

W81281 Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		09/01/1997	0.50		First published.
2	All	12/16/1997 7/12/1999	0.51 0.6		Update Features Update registers description
3					
4					
5					
6					
7					
8					
9					
10					
11					

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Preliminary

TABLE OF CONTENT

<u>1.</u>	<u>GENERAL DESCRIPTION</u>	1
<u>2.</u>	<u>FEATURES</u>	2
<u>3.</u>	<u>BLOCK DIAGRAM</u>	3
<u>4.</u>	<u>PIN CONFIGURATION</u>	4
<u>5.</u>	<u>PIN DESCRIPTION</u>	6
<u>5.1</u>	<u>40 PIN DIP</u>	6
<u>5.2</u>	<u>28-PIN SOP</u>	8
<u>5.3</u>	<u>48-PIN LQFP</u>	9
<u>6</u>	<u>FUNCTIONAL DESCRIPTION</u>	11
<u>6.1</u>	<u>FIRST IN FIRST OUT STORAGE (FIFO'S) ORGANIZATION</u>	11
<u>6.1.1</u>	<u>INTERFACE TO THE MICROCONTROLLER:</u>	11
<u>6.2</u>	<u>REGISTER DESCRIPTION</u>	12
<u>6.2.1</u>	<u>Status Registers</u>	12
<u>6.2.2</u>	<u>Control Registers</u>	13
<u>6.3</u>	<u>RESET</u>	15
<u>6.3.1</u>	<u>External Reset (Hardware Reset)</u>	16
<u>6.3.2</u>	<u>Warm Reset (Software Reset)</u>	16
<u>6.4</u>	<u>USB SUSPEND</u>	16
<u>6.5</u>	<u>USB RESUME</u>	16
<u>7.</u>	<u>PROGRAMMING NOTES:</u>	17
<u>7.1</u>	<u>CONTROL REGISTERS ACCESS:</u>	17
<u>7.2</u>	<u>STATUS REGISTERS ACCESS:</u>	17
<u>7.3</u>	<u>FIFOS ACCESS:</u>	17
<u>7.4</u>	<u>SET STALL FOR ENDPOINT 0 - 4:</u>	17
<u>7.5</u>	<u>SET NULL DATA FOR IN TRANSACTION OF EP 0:</u>	18
<u>8.</u>	<u>ELECTRICAL CHARACTERISTICS & CAPACITANCE</u>	19
<u>9.</u>	<u>USB KEYBOARD SAMPLE APPLICATION</u>	22
<u>10.</u>	<u>PACKAGE DIMENSIONS</u>	24
	<u>APPENDIX A: WINBOND(W81281-004) DEFAULT MATRIX CODE</u>	28



USB Keyboard/ Device Controller

1. GENERAL DESCRIPTION

W81281 is a low cost, high integration single-chip microcontroller with Universal Serial Bus (USB) interface for keyboard application, it includes the core of Winbond 8-bit microprocessor W78C52 which works on 6MHz. It implements a standard PC keyboard and enables connection to host system through low-speed (1.5Mhz) USB connection . It complies with USB Specification Revision 1.0 and HID Class Definition Revision 1.0.

For Keyboard application, W81281 supports an 18 X 8 keyboard scan matrix, which allows suspend wake up, and also provides a port for PS/2 mouse. It consists of an 8051 compatible CPU core, a 6K-byte ROM, a 256-byte SRAM, and three 16-bit programmable timers.

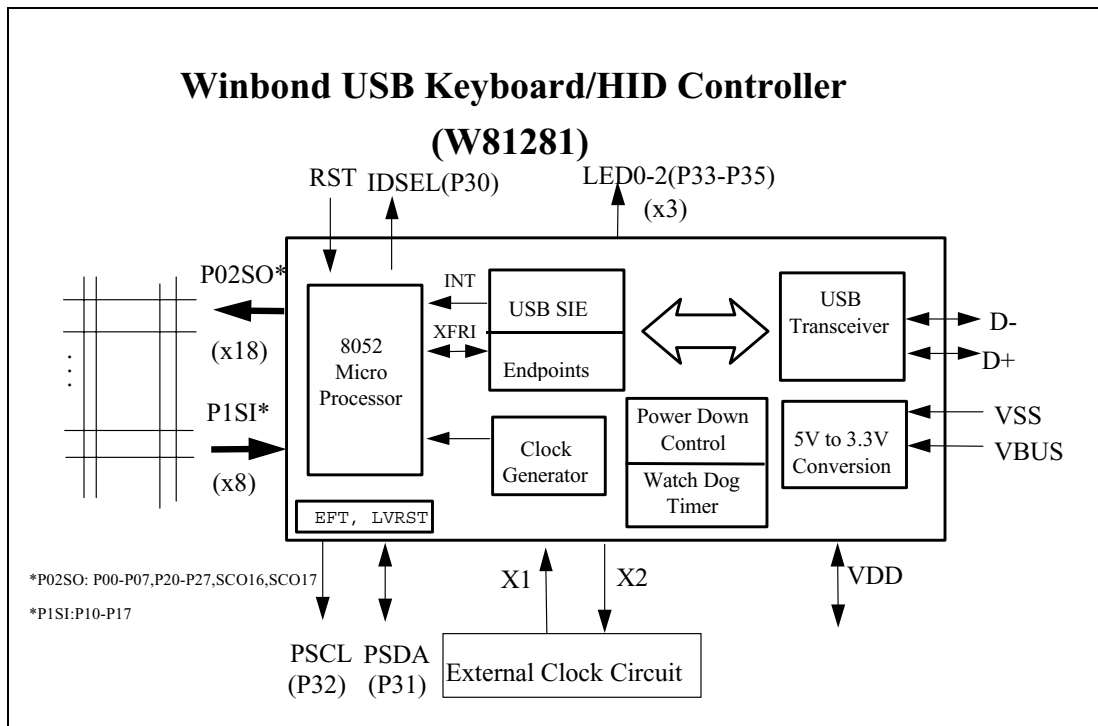
W81281 supports one device address and five endpoints, one bi-directional endpoint for Control transfer and four unidirectional endpoints for Interrupt IN transfer. Through modification of firmware of W78C52, it can be used for multifunction device design, such as USB-IR receiver and any Slow-Speed (1.5Mhz) USB peripheral device controller.

2. FEATURES

- Fully compliant with USB spec. Rev.1.0 and HID Class Rev. 1.0
- Supporting one device address and five endpoints (one Control transfer, four Interrupt transfer)
- Implementing USB keyboard with PS/2 mouse connection
- Microsoft Intellimouse(3D mouse) Supported
- Supporting 8-bit sense (row) input with wake up interrupt on falling edge, internal pull-ups
- Supporting 18-bit drive (column) output, open drain with pull-ups
- 8-bit 8051 compatible CPU core
- 6K-byte ROM
- 256-byte SRAM
- 3 direct drive LED outputs with internal series resistors
- Supporting warm reset
- Built-in low voltage reset and EFT/ESD protection circuit
- Built-in Watch-Dog Timer for device recovery
- Support Win98 system control function
- Support suspend/wake-up function, suspend current under 500 μ A
- Internal 3.3V regulator supported
- 40-pin DIP, 28-pin SOP and 48-pin LQFP packages
- 5V CMOS Device

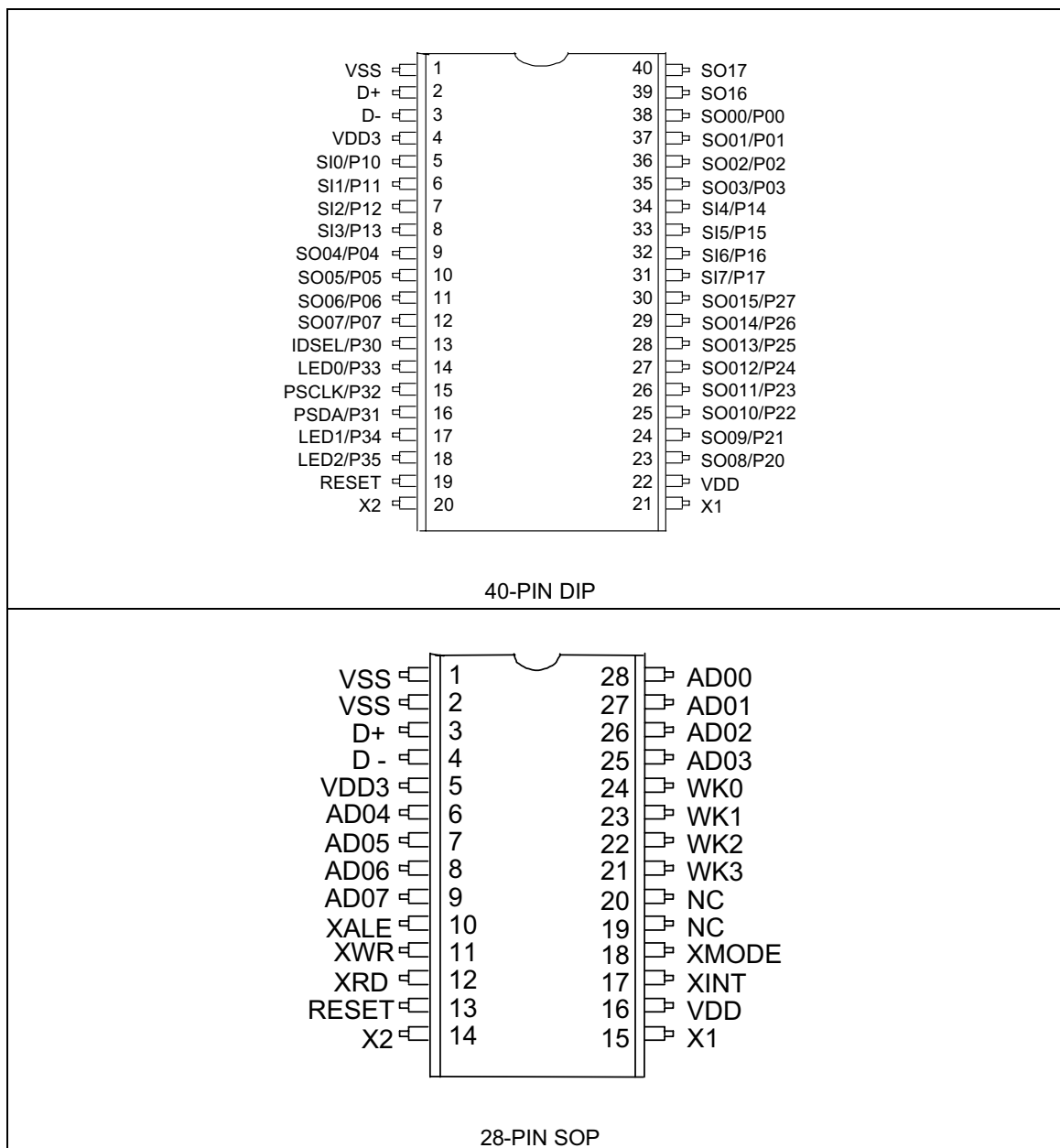
3

Winbond USB Keyboard/HID Controller

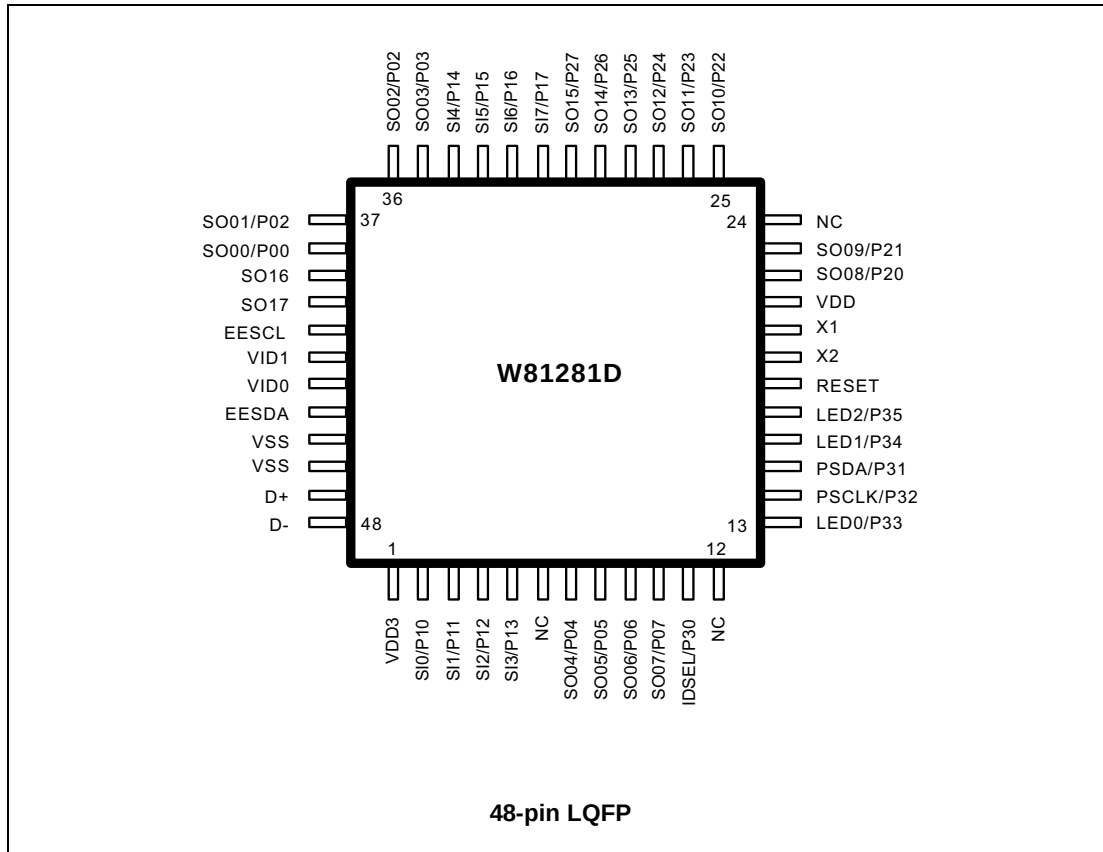


Preliminary

4. PIN CONFIGURATION



Preliminary



Preliminary

5. PIN DESCRIPTION

5.1 40 PIN DIP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VSS	POWER	Ground
2	D+	I/O	USB signal (+)
3	D-	I/O	USB signal (-)
4	VDD3	POWER	DC power 3.3V output
5	SI0/P10	I/O	Keyboard scan Input 0 / Internal μ C IO port 1.0
6	SI1/P11	I/O	Keyboard scan Input 1 / Internal μ C IO port 1.1
7	SI2/P12	I/O	Keyboard scan Input 2 / Internal μ C IO port 1.2
8	SI3/P13	I/O	Keyboard scan Input 3 / Internal μ C IO port 1.3
9	SO04/P04	I/O	Keyboard scan Output 04 / Internal μ C IO port 0.4
10	SO05/P05	I/O	Keyboard scan Output 05 / Internal μ C IO port 0.5
11	SO06/P06	I/O	Keyboard scan Output 06 / Internal μ C IO port 0.6
12	SO07/P07	I/O	Keyboard scan Output 07 / Internal μ C IO port 0.7
13	IDSEL/P30	I/O	Vendor ID selection / Internal μ C IO port 3.0
14	LED0/P33	I/O	Num. Lock LED / Internal μ C IO port 3.3
15	PSCLK/P32	I/O	PS/2 mouse clock pin / Internal μ C IO port 3.2
16	PSDA/P31	I/O	PS/2 mouse data pin / Internal μ C IO port 3.1
17	LED1/P34	I/O	Caps Lock LED / Internal μ C IO port 3.4
18	LED2/P35	I/O	Scroll Lock LED / Internal μ C IO port 3.5
19	RESET	INPUT	Chip reset pin
20	X2	OUTPUT	Clock output
21	X1	INPUT	Clock input
22	VDD	POWER	VDD power
23	SO08/P20	I/O	Keyboard scan Output 08 / Internal μ C IO port 2.0
24	SO09/P21	I/O	Keyboard scan Output 09 / Internal μ C IO port 2.1
25	SO10/P22	I/O	Keyboard scan Output 10 / Internal μ C IO port 2.2
26	SO11/P23	I/O	Keyboard scan Output 11 / Internal μ C IO port 2.3
27	SO12/P24	I/O	Keyboard scan Output 12 / Internal μ C IO port 2.4
28	SO13/P25	I/O	Keyboard scan Output 13 / Internal μ C IO port 2.5

Preliminary

5.1 40-PIN DIP, continued

PIN NO.	NAME	TYPE	DESCRIPTION
29	SO14/P26	I/O	Keyboard scan Output 14 / Internal μ C IO port 2.6
30	SO15/P27	I/O	Keyboard scan Output 15 / Internal μ C IO port 2.7
31	SI7/P17	I/O	Keyboard scan Input 7 / Internal μ C IO port 1.7
32	SI6/P16	I/O	Keyboard scan Input 6 / Internal μ C IO port 1.6
33	SI5/P15	I/O	Keyboard scan Input 5 / Internal μ C IO port 1.5
34	SI4/P14	I/O	Keyboard scan Input 4 / Internal μ C IO port 1.4
35	SO03/P03	I/O	Keyboard scan Output 03 / Internal μ C IO port 0.3
36	SO02/P02	I/O	Keyboard scan Output 02 / Internal μ C IO port 0.2
37	SO01/P01	I/O	Keyboard scan Output 01 / Internal μ C IO port 0.1
38	SO00/P00	I/O	Keyboard scan Output 00 / Internal μ C IO port 0.0
39	SO16	OUTPUT	Keyboard scan Output 16
40	SO17	OUTPUT	Keyboard scan Output 17

Preliminary

5.2 28-PIN SOP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VSS	POWER	Ground
2	VSS	POWER	Ground
3	D+	I/O	USB signal (+)
4	D-	I/O	USB signal (-)
5	VDD3	POWER	DC power 3.3V output
6	AD04	I/O	μC Interface AD04 (Address/Data 04)
7	AD05	I/O	μC Interface AD05 (Address/Data 05)
8	AD06	I/O	μC Interface AD06 (Address/Data 06)
9	AD07	I/O	μC Interface AD07 (Address/Data 07)
10	XALE	I/O	μC Interface ALE (Address Latch Enable)
11	XWR	I/O	μC Interface WR (Data Write)
12	XRD	I/O	μC Interface RD (Data Read)
13	RESET	INPUT	Chip reset pin
14	X2	OUTPUT	Clock output
15	X1	INPUT	Clock input
16	VDD	POWER	VDD power
17	XINT	I/O	μC Interface INT (Interrupt)
18	XMODE	I/O	Controller mode setting, it should be kept high
19	NC	I/O	Not Used
20	NC	I/O	Not Used
21	WK3	INPUT	Wakeup pin, Active low and keep more than 100ns
22	WK2	INPUT	Wakeup pin, Active low and keep more than 100ns
23	WK1	INPUT	Wakeup pin, Active low and keep more than 100ns
24	WK0	INPUT	Wakeup pin, Active low and keep more than 100ns
25	AD03	I/O	μC Interface AD03 (Address/Data 03)
26	AD02	I/O	μC Interface AD02 (Address/Data 02)
27	AD01	I/O	μC Interface AD01 (Address/Data 01)
28	AD00	I/O	μC Interface AD00 (Address/Data 00)

Preliminary

5.3 48-PIN LQFP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VDD3	POWER	DC power 3.3V output
2	SI0/P10	I/O	Keyboard scan Input 0 / Internal μ C IO port 1.0
3	SI1/P11	I/O	Keyboard scan Input 1 / Internal μ C IO port 1.1
4	SI2/P12	I/O	Keyboard scan Input 2 / Internal μ C IO port 1.2
5	SI3/P13	I/O	Keyboard scan Input 3 / Internal μ C IO port 1.3
6	NC	none	Not Used
7	SO04/P04	I/O	Keyboard scan Output 04 / Internal μ C IO port 0.4
8	SO05/P05	I/O	Keyboard scan Output 05 / Internal μ C IO port 0.5
9	SO06/P06	I/O	Keyboard scan Output 06 / Internal μ C IO port 0.6
10	SO07/P07	I/O	Keyboard scan Output 07 / Internal μ C IO port 0.7
11	IDSEL/P30	I/O	Vendor ID selection / Internal μ C IO port 3.0
12	NC	none	Not Used
13	LED0/P33	I/O	Num. Lock LED / Internal μ C IO port 3.3
14	PSCLK/P32	I/O	PS/2 mouse clock pin / Internal μ C IO port 3.2
15	PSDA/P31	I/O	PS/2 mouse data pin / Internal μ C IO port 3.1
16	LED1/P34	I/O	Caps Lock LED / Internal μ C IO port 3.4
17	LED2/P35	I/O	Scroll Lock LED / Internal μ C IO port 3.5
18	RESET	INPUT	Chip reset pin
19	X2	OUTPUT	Clock output
20	X1	INPUT	Clock input
21	VDD	POWER	VDD power
22	SO08/P20	I/O	Keyboard scan Output 08 / Internal μ C IO port 2.0
23	SO09/P21	I/O	Keyboard scan Output 09 / Internal μ C IO port 2.1
24	NC	none	Not Used
25	SO10/P22	I/O	Keyboard scan Output 10 / Internal μ C IO port 2.2
26	SO11/P23	I/O	Keyboard scan Output 11 / Internal μ C IO port 2.3
27	SO12/P24	I/O	Keyboard scan Output 12 / Internal μ C IO port 2.4
28	SO13/P25	I/O	Keyboard scan Output 13 / Internal μ C IO port 2.5
29	SO14/P26	I/O	Keyboard scan Output 14 / Internal μ C IO port 2.6
30	SO15/P27	I/O	Keyboard scan Output 15 / Internal μ C IO port 2.7

Preliminary

5.3 48-PIN LQFP, continued

PIN NO.	NAME	TYPE	DESCRIPTION
31	SI7/P17	I/O	Keyboard scan Input 7 / Internal μ C IO port 1.7
32	SI6/P16	I/O	Keyboard scan Input 6 / Internal μ C IO port 1.6
33	SI5/P15	I/O	Keyboard scan Input 5 / Internal μ C IO port 1.5
34	SI4/P14	I/O	Keyboard scan Input 4 / Internal μ C IO port 1.4
35	SO03/P03	I/O	Keyboard scan Output 03 / Internal μ C IO port 0.3
36	SO02/P02	I/O	Keyboard scan Output 02 / Internal μ C IO port 0.2
37	SO01/P01	I/O	Keyboard scan Output 01 / Internal μ C IO port 0.1
38	SO00/P00	I/O	Keyboard scan Output 00 / Internal μ C IO port 0.0
39	SO16	OUTPUT	Keyboard scan Output 16
40	SO17	OUTPUT	Keyboard scan Output 17
41	EESCL	OUTPUT	Clock pin of External serial EEPROM
42	VID1	INPUT	Vendor ID selection 1
43	VID0	INPUT	Vendor ID selection 0
44	EESDA	I/O	Data pin of External serial EEPROM
45	VSS	POWER	Ground
46	VSS	POWER	Ground
47	D+	I/O	USB signal (+)
48	D-	I/O	USB signal (-)

6 FUNCTIONAL DESCRIPTION

6.1 First In First Out Storage (FIFO'S) Organization

The W81281 has six FIFO's, one for receiving and five for transmitting.

FIFO or SRAM	SIZE (Byte)	NOTES
Endpt 0 Receiving	8	Data received on upstream port which contains the correct address and pids will be stored here for the CPU core to read.
Endpt 0 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 2 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 3 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 4 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.

6.1.1 INTERFACE TO THE MICROCONTROLLER:

The FIFOs communicate with the CPU core by address 06H Of External DATA Memory Access of CPU during IP.6 = "1". The FIFO access steps are firstly set IP.6 = "1" in CPU core. Secondly, CPU core selects FIFO to access by setting the followed bits in control register 2 :

EP0_RD_EN : read "IN" FIFO of Endpoint 0 (EP0).

EP0_WR_EN : write "OUT" FIFO of Endpoint 0 (EP0).

EP1_WR_EN : write "OUT" FIFO of Endpoint 1 (EP1).

EP2_WR_EN : write "OUT" FIFO of Endpoint 2 (EP2).

EP3_WR_EN : write "OUT" FIFO of Endpoint 3 (EP3).

EP4_WR_EN : write "OUT" FIFO of Endpoint 4 (EP4).

Then access FIFO by address 06H of External DATA Memory Access of CPU. For detailed programming steps, refer to section 7.3 Programming Note.

6.2 Register Description

The CPU core accesses registers by External DATA Memory Access during IP.6 = "1"1'

6.2.1 Status Registers

CPU core can set "High" at USB_EventINT_EN bit of control register 4 to enable interrupt of USB events to INT0. When interrupt comes, CPU reads status register 0 and 1 to check which event occurs. (refer to section 7.2 for accessing Status Registers)

Status Register 0: Address = 00H (Interrupt Event Flags)

BIT	SYMBOL	DESCRIPTION
7	NAK_EP0_IN	NAK occurs from EP0 for IN Transaction. (only valid during NakEP0In_INT_EN = 1 in Control Register 3)
6	ACK_EP0_SETUP	ACK occurs from EP0 for SETUP Transaction
5	ACK_EP0_OUT	ACK occurs from EP0 for OUT Transaction
4	ACK_EP0_IN	ACK occurs from EP0 for IN Transaction
3	ACK_EP1_IN	ACK occurs from EP1 for IN Transaction
2	ACK_EP2_IN	ACK occurs from EP2 for IN Transaction
1	ACK_EP3_IN	ACK occurs from EP3 for IN Transaction
0	ACK_EP4_IN	ACK occurs from EP4 for IN Transaction

Status Register 1: Address = 01H (Interrupt Event Flags)

BIT	SYMBOL	DESCRIPTION
7-6	VID[1:0]	Keyboard Scan Matrix Selection.
5	Reserved	must ignore this value.
4	EP0OutNullData	receiving Null Data at EP0 during OUT Transaction
3	Suspend_In	Suspend Mode active (no traffic on USB Bus > 3 mS)
2	USB_Reset	receiving Reset command from USB Bus
1	Resume_In	receiving Resume command from USB Bus
0	Reserved	must ignore this value

Preliminary

Status Register 2: Address = 07H (Data Byte Count of EP0 IN FIFO)

BIT	SYMBOL	DESCRIPTION
7-4	Reserved	must ignore those values
3-0	DataLength_CNT[3:0]	Number of Data byte for EP0 FIFO (receiving Data from USB Bus)

6.2.2 Control Registers

(All registers are set to 00h at power up.)(refer to section 7.1 for accessing Control Registers)

Control Register 0: Address = 02H (Endpoint Enable Control)

BIT	SYMBOL	DESCRIPTION
7-5	Reserved	must keep bits = "0"
4	USB_Speed	set "High" for Full Speed; set "Low" for Low Speed
3	EP1_EN	set "High" to enable Endpoint 1
2	EP2_EN	set "High" to enable Endpoint 2
1	EP3_EN	set "High" to enable Endpoint 3
0	EP4_EN	set "High" to enable Endpoint 4

Control Register 1: Address = 03H (Device Address Setting)

BIT	SYMBOL	DESCRIPTION
7	Bus_Connection	connect up stream port on USB Bus after chip initialization done
6-0	Device_Address[6:0]	Setup Device Address

Control Register 2: Address = 04H (FIFO Access Control)

BIT	SYMBOL	DESCRIPTION
7	Reserved	must keep bit = "0".
6	Set_Stall	Set Stall for EP 0 -4 (refer to section 7.4 for programming)

Preliminary

5	EP0_RD_EN	Set "High" before reading IN FIFO of EP0 (receiving Data from USB Bus)
4	EP0_WR_EN	Set "High" before writting OUT FIFO of EP0 (transmitting Data to USB Bus)
3	EP1_WR_EN	Set "High" before writting OUT FIFO of EP1 (transmitting Data to USB Bus)
2	EP2_WR_EN	Set "High" before writting OUT FIFO of EP2 (transmitting Data to USB Bus)
1	EP3_WR_EN	Set "High" before writting OUT FIFO of EP3 (transmitting Data to USB Bus)
0	EP4_WR_EN	Set "High" before writting OUT FIFO of EP4 (transmitting Data to USB Bus)

Control Register 3: Address = 05H (USB Event Control)

BIT	SYMBOL	DESCRIPTION
7	Reserved	must keep bit = "0"
6	NakEP0In_INT_EN	Enable interrupt event when NAK comes from EP0 for IN Transaction
5	Set_EP0NullData	set Null Data for IN Transaction of EP 0 (refer to section 7.5 for programming)
4	Warm_Reset	Active Warm Reset
3	Resume_Out	Send Resume command (K-state) to USB Bus (Set_Suspend should be "1")
2	Set_Suspend	Set suspend mode active
1	Read_Event	Set "High" during reading Status Registers (refer to section 7.2 for programming)
0	Set_EP0_Nak	Set "High" for responding Nak when IN/OUT Transaction of EP0 come

Preliminary

Control Register 4: Address = 08H (Interrupt Enable Control)

BIT	SYMBOL	DESCRIPTION
7-4	Reserved	must keep bits = "0"
3	Remote_Wakeup_EN	for Remote Wakeup Enable from Keystroke or Mouse moving
2	USB_EventINT_EN	for USB event interrupt enable
1	SCANOUT[17]	output port value of port SO17
0	SCANOUT[16]	output port value of port SO16

Control Register 5: Address = 09H (CPU Reset Control)

BIT	SYMBOL	DESCRIPTION
7-2	Reserved	must keep bit = "0"
1	UC_WarmReset_EN	set "High" for resetting CPU when Warm_Reset = "1"
0	DisconUSB_Bus_Disable	set "High" keeping device connecting with USB Bus during software or hardware reset set low" disconnecting with USB Bus during software or hardware reset

Control Register 6: Address = 0EH (Watch Dog Timer Reset)

BIT	SYMBOL	DESCRIPTION
7-0	Reset_WDT	Clear WDT = 00H when set Reset_WDT = AAH

6.3 Reset

The W81281 supports three types of reset. During a reset, all registers of the CPU core and USB return to their default status, and USB device address is set to zero.

Preliminary

6.3.1 External Reset (Hardware Reset)

As in 8051 series controller, the external RESET signal is sampled at S5P2. To take effect, it must be held high at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON(with exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6.3.2 Warm Reset (Software Reset)

W81281 provides a warm reset by setting "High" at Warm_Reset bit of control register 3.

The W81281 handles the USB reset function independently from the CPU core. If a Single Ended Zero (SE0) is detected on the upstream port for greater than 2.5us, then the interrupt is enabled. The CPU core read flag from USB_Reset bit of status register 1 then CPU

- to reset the device address to 0, and enter the default state. No any reset timing occurs.

or

- to set "High" at Warm_Reset bit of control register

6.3.3 WDT Reset (Hardware Reset)

There is a Watch Dog Timer installed in W81C281. CPU should periodically clear WDT to 00H by setting Reset_WDT=AAH before WDT time out. If CPU hangs WDT will time-out and cause hardware reset.

6.4 USB Suspend

If there is no upstream activity for 3 msec then the Suspend_In flag is set and the interrupt enabled. When Suspend_In flag is read, CPU core activates power down mode for W81281 go into suspend

6.5 USB RESUME:

The suspend state can be exit by a 'resume'. The resume can occur by three methods.

- The host can send a resume to all ports by placing a 0 (K state) on the bus. The W81281 sees the resume, , and enables the interrupt. In this case, the CPU core does not have to perform any functions.
- The host can reset the bus.
- When any falling edge is detected on CPU port1(keystrokes). The CPU core will exit from power down mode and initiate a resume by setting Resume_Out in the Control Register 3 which will cause a K state to be sent. To un-resume, the CPU core must clear the Resume_Out bit in the Control Register 3.

Preliminary

7. PROGRAMMING NOTES:

The W81281 uses reserved bit of the Interrupt Priority Register IP.6 as a pre-decoding bit to implement a alternative register and FIFO by External Data Memory Access of CPU core. Programming functions described as below:

7.1 Control Registers Access:

- Step 1: set IP.6 = 1
- Step 2: access Control Register (by MOVX Instruction)
- Step 3: set IP.6 = 0

7.2 Status Registers Access:

- Step 1: set IP.6 = 1
- Step 2 : set Read_Event = 1 in Control Register 3 (by MOVX Instruction)
- step 3 : access Status Registers (by MOVX Instruction)
- step 4 : set IP.6 = 0

7.3 FIFOs Access :

- step 1 : set IP.6 = 1
- step 2 : set EP0_RD_EN/EPX_WR_EN = 1 (X : 0 - 4) (by MOVX Instruction)
- step 3 : access FIFO by address 06H of MOVX Instruction
- step 4 : set EP0_RD_EN/EPX_WR_EN = 0 (X : 0 - 4) (by MOVX Instruction)
- step 5 : set IP.6 = 0

7.4 Set Stall for Endpoint 0 - 4 :

- step 1 : set IP.6 = 1
- step 2 : set Set_Stall = 1 (by MOVX Instruction)
- step 3 : set EP0_RD_EN/EPX_WR_EN = 1 (X : 0 - 4) (by MOVX Instruction)
- step 4 : set EP0_RD_EN/EPX_WR_EN = 0 (X : 0 - 4) (by MOVX Instruction)
- step 5 : set Set_Stall = 0 (by MOVX Instruction)
- step 6 : set IP.6 = 0

Note : 1. EP0_RD_EN = 1 for OUT Transaction of EP0.

2. EP0_WR_EN = 1 for IN Transaction of EP0.

7.5 Set Null Data for IN Transaction of EP 0 :

step 1 : set IP.6 = 1

step 2 : set Set_EP0NullData = 1 (by MOVX Instruction)

step 3 : set EP0_WR_EN = 1 (by MOVX Instruction)

step 4 : set EP0_WR_EN = 0 (by MOVX Instruction)

step 5 : set Set_EP0NullData = 0 (by MOVX Instruction)

step 6 : set IP.6 = 0

Preliminary

8. ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0°C to +70°C, VDD = +5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
VDD	Power Supply	4.0	5.0	5.5	V	
VIL	Input Low Voltage (except RESET)			0.8	V	
VIL1	Input Low Voltage (RESET)			0.6	V	
VIH1	Input High Voltage (except RESET)	2.0			V	
VIH2	Input High Voltage (RESET)	3.5			V	
VOH	Output High Voltage (except D+/D-)			2.4	V	IOH=-4mA
VOL	Output Low Voltage (except D+/D-)	0.4			V	IOL= 4mA
IOFL	Output Leakage Current (High-Z state)	-10		10	uA	
IIH	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VDD
IIL	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VSS

Preliminary

	Symbol	Conditions	Min	Max	Unit
D+/D- Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V < VIN < 3.3V	-10	+10	μA
D+/D- Input Levels:					
Differential Input Sensitivity	VDI	(D+) - (D-)	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Endge Receiver Threshold	VSE		0.8	2.0	V
D+/D- Output Levels:					
Static Output Low	VOL	RL of 1.5kΩ to 3.6V		0.3	V
Static Output High	VOH	RL of 1.5kΩ to GND	2.8	3.6	V
D+/D- Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
D+/D- Driver Characteristics:					
Transition Time:					
Rise Time	TR	CL=50pF/350pF	75	300	ns
Fall Time	TF	CL=50pF/350pF	75	300	ns
Rise / Fall Time Matching	TRFM	(TR / TF)	80	125	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
D+/D- Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave.Bit Rate (1.5Mb/s ±1.5%)	1.4775	1.5225	Mbs
Source Differential Driver Jitter					
To Next Transition	TDJ1		-95	95	ns
For Paired Transitions	TDJ2		-150	150	ns
Source EOP Width	TEOPT		1.25	1.50	μs
Differential to EOP Transition Skew	TDEOP		-40	100	ns
D+/D- Data Receiver Timings:					
Receiver Data Jitter Tolerance					
To Next Transition	TDJR1		-75	75	ns
For Paired Transitions	TDJR2		-45	45	ns
Receiver SE0 Tolerance during Differential Transition	TLST			210	ns

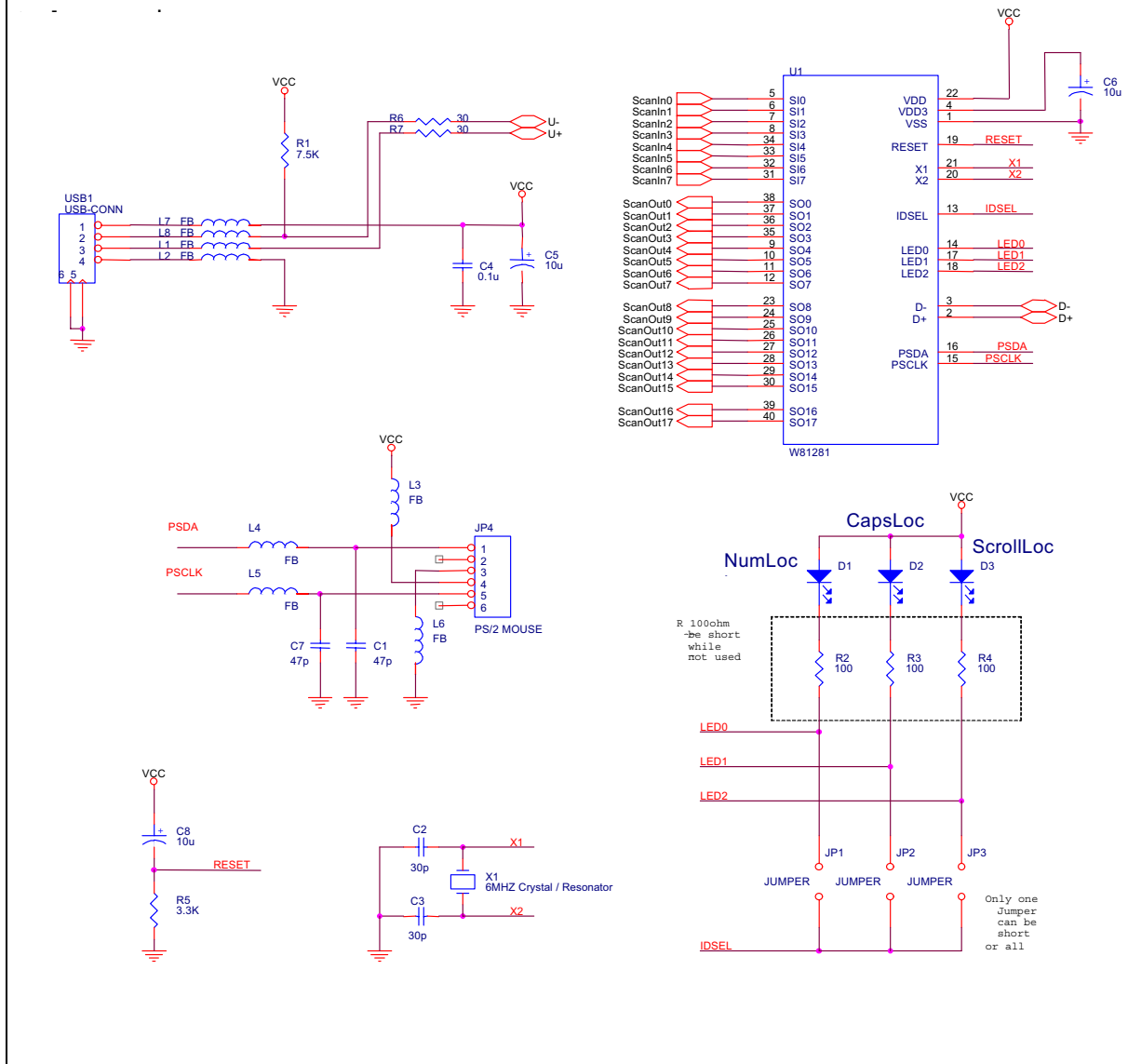
Preliminary

EOP Width at receiver					
Must reject as EOP	TEORP1		330		ns
Must accept as EOP	TEOPR2		675		ns

9. USB KEYBOARD SAMPLE APPLICATION

1. For 40 pin DIP package

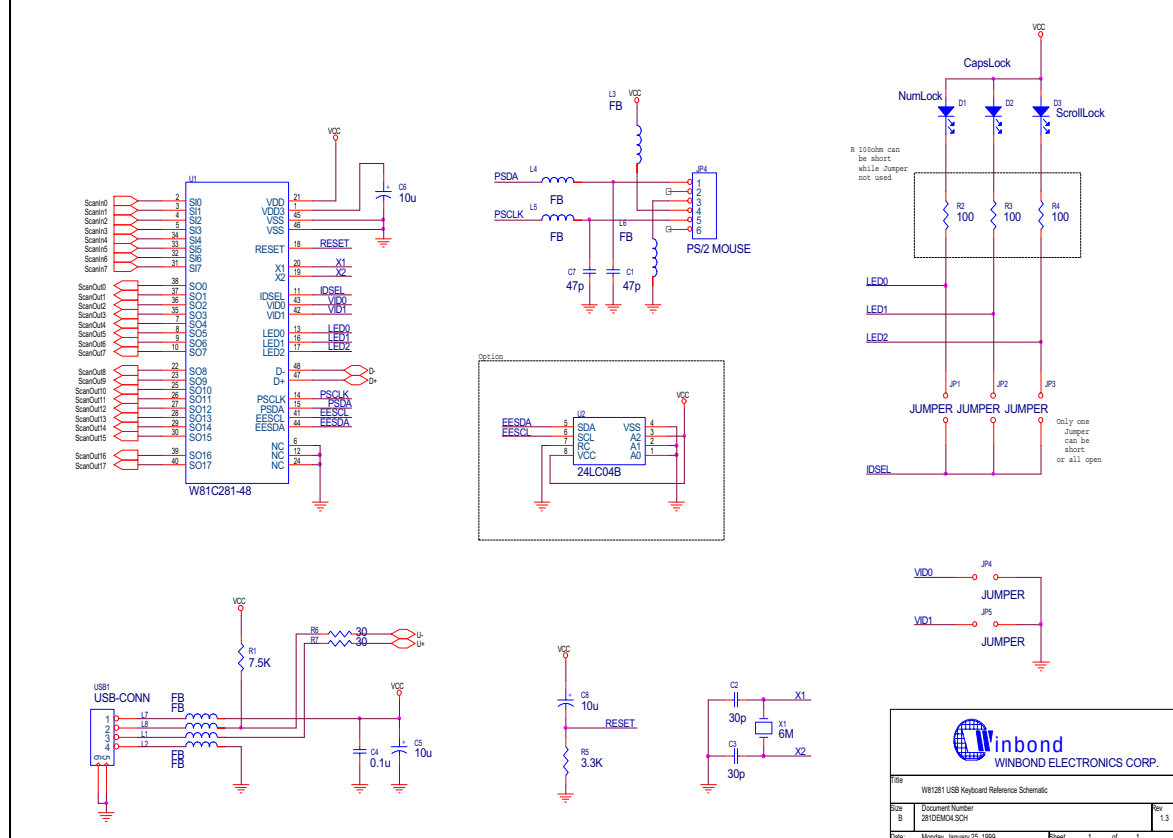
W81281 USB Keyboard Reference



Preliminary

For 48 pin LQFP package reference circuit

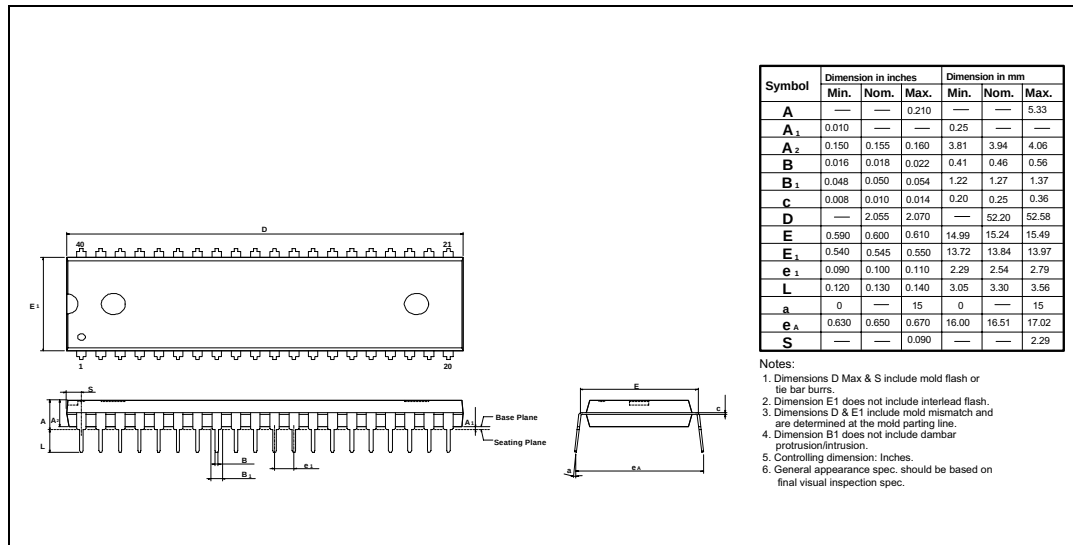
W81281 (48pin LQFP) USB Keyboard Reference Schematic



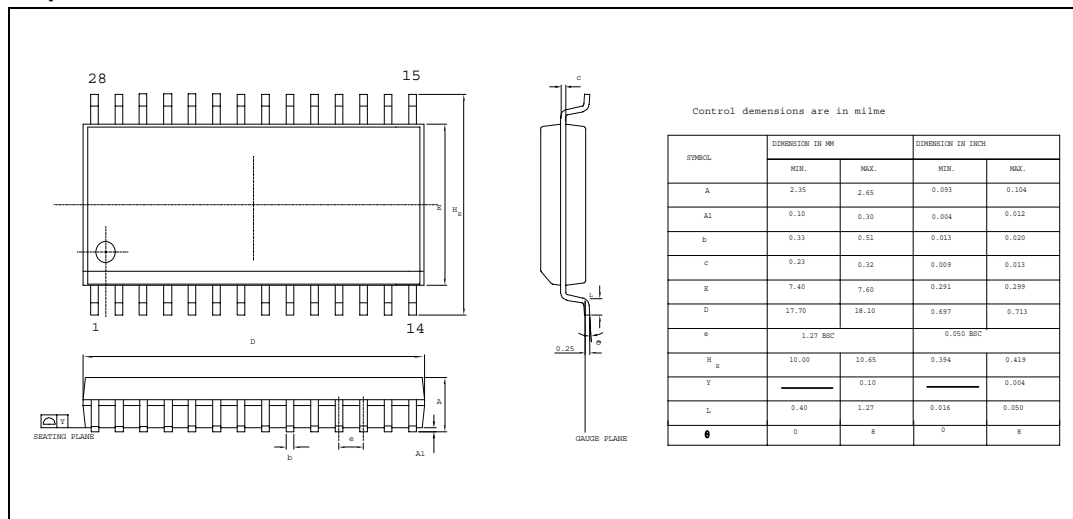
Preliminary

10. PACKAGE DIMENSIONS

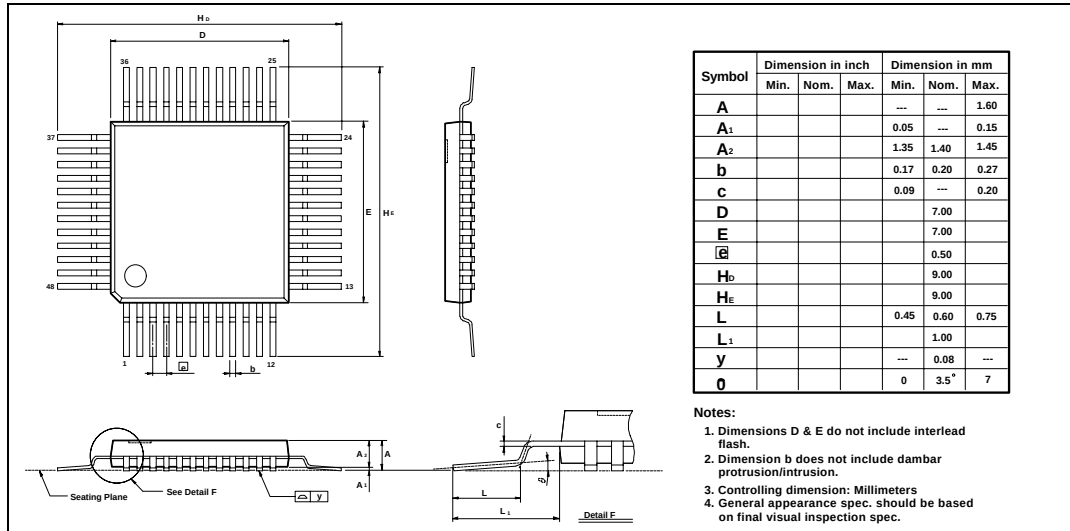
40-pin DIP



28-pin SOP



Preliminary

48-pin LQFP


Headquarters
 No. 4, Creation Rd. III
 Science-Based Industrial Park
 Hsinchu, Taiwan
 TEL: 886-35-770066
 FAX: 886-35-789467
 www: <http://www.winbond.com.tw/>

Taipei Office
 11F, No. 115, Sec. 3, Min-Sheng East Rd.
 Taipei, Taiwan
 TEL: 886-2-7190505
 FAX: 886-2-7197502
 TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
 Rm. 803, World Trade Square, Tower II
 123 Hoi Bun Rd., Kwun Tong
 Kowloon, Hong Kong
 TEL: 852-27516023-7
 FAX: 852-27552064

**Winbond Electronics
 (North America) Corp.**
 2730 Orchard Parkway
 San Jose, CA 95134 U.S.A.
 TEL: 1-408-9436666
 FAX: 1-408-9436668

Preliminary

**Industrial Technology Research Institute***Electronics Research & Service Organization*
Bldg. 17, 195-4 Sec. 4, Chung Hsing Rd., Chutung, Hsinchu, 310
Taiwan, Republic Of China
TEL : 886-3-5915717 FAX : 886-3-5825720

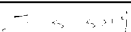
Report No. : 500-8801-018

Page 1 of 12

ELECTROMAGNETIC SUSCEPTIBILITY TEST REPORT

Company : Winbond Electronics Corp.
Address : No.4, Creation Rd. III, Science-Based Industrial Park
Hsinchu, Taiwan, R.O.C.
Sample Name : USB Keyboard
Model : W81281
Date Received : JAN. 11, 1999
Date Tested : JAN. 11, 1999

WE HEREBY CERTIFY THAT: The object of these measurements were made to establish a common and reproducible basis for evaluating the performance of electrical and electronic equipment when were subjected to the immunity test. We assume full responsibility for the accuracy and completeness of these measurements and vouch for the qualifications of all persons taking them.

	Name	Signature	Date
Testing Engineer	J. S. Song		<u>JAN. 12, 1999</u>
Approving Manager	Paul Y. Liao		<u>Jan. 14, 1999</u>

Notes :

1. This report will be invalid if duplicated or photocopied in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid as separately used.
3. This report is invalid without examination stamp and signature of this institute.
4. The tested specimen(s) will be preserved for thirty days from the date issued.

Preliminary



Industrial Technology Research Institute
Electronics Research & Service Organization
 Dldg. 17, D95-4 Sec. 4, Chung Hsing Rd., Chung Hsing, 310
 Taiwan, Republic Of China
 TEL : 886-3-5915717 FAX : 886-3-5825720

Report No. : 500-8801-018
 Page 8 of 12

2.4 Performance criteria

- A. The equipment shall continue to operate as intended. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer.
- B. After the test the equipment shall continue to operate as intended. No degradation of performance or loss of function is allowed after the application of the phenomena below a performance level specified by the manufacturer.
- During the test, degradation of performance is allowed however. No change of actual operating state or stored data is allowed.
- C. Loss of function is allowed, provided the function is self recoverable or can be restored by the operation of the controls by the user in accordance with the manufacturers instructions.

2.5 Uncertainty of electrostatic discharge test

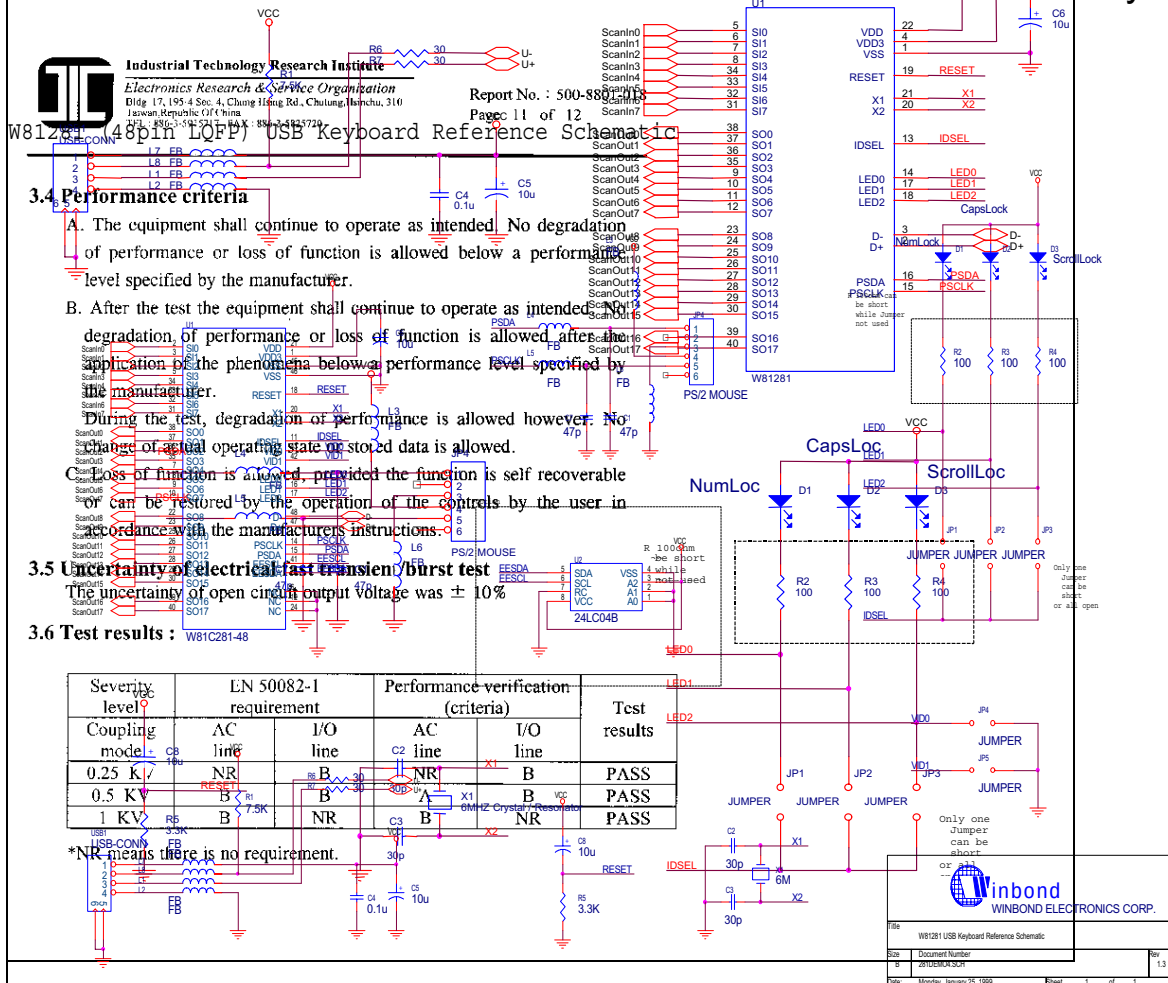
The uncertainty of output voltage indication was $\pm 5\%$

2.6 Test results :

Severity level	EN 50082-1 requirement				Performance verification (criteria)				Test results
	Air discharge	Contact discharge	HCP discharge	VCP discharge	Air discharge	Contact discharge	HCP discharge	VCP discharge	
2 KV	B	B	B	B	A	A	A	A	Pass
4 KV	B	B	B	B	A	A	B	A	Pass
8 KV	B	NR	NR	NR	A	NR	NR	NR	Pass

*NR means there is no requirement

Preliminary



APPENDIX A: WINBOND(W81281-004) DEFAULT MATRIX CODE

VID: 0000 PID: 0801(with PS/2 mouse) PID: 0802(without PS/2 mouse)

101(AT)/102(Europe+Macro)(+Fn)/103(Korean)(Brazilian)/106(Japan.)+Windows 95 keys compatible

Preliminary

	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO10	SO11	SO12	SO13	SO14	SO15	SO16	SO17
SI0	64 K45 Macro	24 7	14 Q	12 O	07 D	34 “	05 B	39 Caps	3F F6	60 P_8	5A P_2	31 K29 _	EC	8B K131 J-NCHG	E1 Shift-L	F5	FA	EB
SI1	29 ESC	25 8	1A W	13 P	09 F	35 ~	11 N	2C SPC	40 F7	61 P_9	5B P_3	4A Home	Wake -up	E3 Win-L	87 K56 J-56	89 K14 J-14	F9	EE
SI2	1E 1	26 9	08 E	2F I	0A G	4D End	10 M	4E PgDn	41 F8	56 P_-	62 P_0	52 Up	E0 Ctrl-L	F1	01	01	91 K150 Kor0-L	EA
SI3	1F 2	27 0	15 R	30 J	0B H	32 K42 _	36 <	3A F1	42 F9	5C P_4	63 P_.	4B PgUp	E4 Ctrl-R	F0	01	01	F8 90 K151 Kor1-R	Shift-R
SI4	20 3	2D -	17 T	28 Enter	0D J	1D Z	37 >	3B F2	43 F10	5D P_5	58 P_Entr	48 Pause	Power	EF	E5 Shift-R	F4 87 K56 B20	E5 Shift-R	94 K107 BZ1
SI5	21 4	2E +	1C Y	51 Down	0E K	1B X	38 ?	3C F3	53 Num	5E P_6	44 F11	50 Left	E9	Sleep	F3	E2 Alt-L	F7	FF
SI6	22 5	2A BKS	18 U	04 A	0F L	06 C	4C Del	3D F4	47 Scroll	57 P_+	45 F12	4F Right	E8	ED	F2	E6 Alt-R	E7 Win-R	FF
SI7	23 6	2B TAB	0C I	16 S	33 ;	19 V	55 *	3E F5	5F P_7	59 P_1	46 PtScr	49 Ins	54 /	8A K132 J-CHG	65 APP	88 K133 J-ROMA	F6	FB

Preliminary

- NOTE 1:** The contents in the table are hexadecimal HID codes and function descriptor.
- 2:** Six are scan-in lines, Sox are scan-out lines.
- 3:** The three ACPI power management keys for Windows 98 are Power (SI4-SO12), Sleep (SI5-SO13) and Wakeup (SI1-SO12).

Multimedia Buttons & Reserved Buttons (W81281-004)

HID Code	Functions (ref. Qtronix)
E8	Play/Pause
E9	Stop/Eject
EA	Rewind
EB	Forward
EC	Record
ED	Volume+
EE	Volume-
EF	Mute
F0	WWW
F1	Previous
F2	Next
F3	Stop
F4	Search
F5	ScrollUp
F6	ScrollDown
F7	Menu
F8	Suspend
F9	Coffee
FA	Xfer
FB	Calculator
FC	Reserved (OnNoPower)
FD	Reserved (OnNoSleep)
FE	Reserved (OnNoWakeup)
FF	Reserved



W81281



Preliminary

HID Codes vs. Legacy Scan-Codes (W81281-004)

	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO10	SO11	SO12	SO13	SO14	SO15	SO16	SO17
SI0	64 <i>K45</i> 56 61 13 08 3D 3D 10 15 15	24 K8 K17	14 K17	12 K25	07 K33	34 K41	05 K50	39 K30	3F K117	60 K96	5A K98	31 K29	EC	8B K131 7B 67 85 2A 12 12	E1 K44	F5	FA	EB
SI1	29 K110 01 76 08	25 K9 09 3E 3E	1A K18 11 1D 1D	13 K26	09 K34	35 K1	11 K51	2C K61	40 K118	61 K101	5B K103	4A K80		E3 K127 5B 1F 8B 73 51 51 7D 6A 5D	87 K56	89 K14	F9	EE
SI2	1E K2 02 16 16	26 K10 0A 46 46	08 K19 12 24 24	2F K27	0A K35	4D K81	10 K52	4E K86	41 K119	56 K105	62 K99	52 K83	E0 K58 1D 14 11	F1 F1 F1 F1 F1	01	01	91 K150 F1 F1 F1	EA
SI3	1F K3 03 1E 1E	27 K11 0B 45 45	15 K20 13 2D 2D	30 K28	0B K36	32 K42	36 K53	3A K112	42 K120	5C K92	63 K104	4B K85	E4 K64 1D 14 58	F0	01	01	F8	90 K151 F0 F2 F2
SI4	20 K4 04 26 26	2D K12 0C 4E 4E	17 K21 14 2C 2C	28 K43	0D K37	1D K46	37 K54	3B K113	43 K121	5D K97	58 K108	48 K126		EF	E5 K57 36 59 59	F4	87 K56 73 51 51	E5 K57 36 59 59
SI5	21 K5 05 25 25	2E K13 0D 55 55	1C K22 15 35 35	51 K84	0E K38	1B K47	38 K55	3C K114	53 K90	5E K102	44 K122	50 K79	E9		F3 K60 38 11 19	E2 K62 38 11 39	F7	94 K107 7E 6D 7B
SI6	22 K6 06 2E 2E	2A K15 0E 66 66	18 K23 16 3C 3C	04 K31	0F K39	06 K48	4C K76	3D K115	47 K125	57 K106	45 K123	4F K89	E8	ED	F2 K62 38 11 39	E6 K62 5C 27 8C	E7 K128	FF
SI7	23 K7 07 36 36	2B K16 0F 0D 0D	0C K24 17 43 43	16 K32	33 K40	19 K49	55 K100	3E K116	5F K91	59 K93	46 K124	49 K75	54 K95 35 4A 77	8A K132 79 64 86	65 K129 5D 2F 8D	88 K133 70 13 87	F6	FB

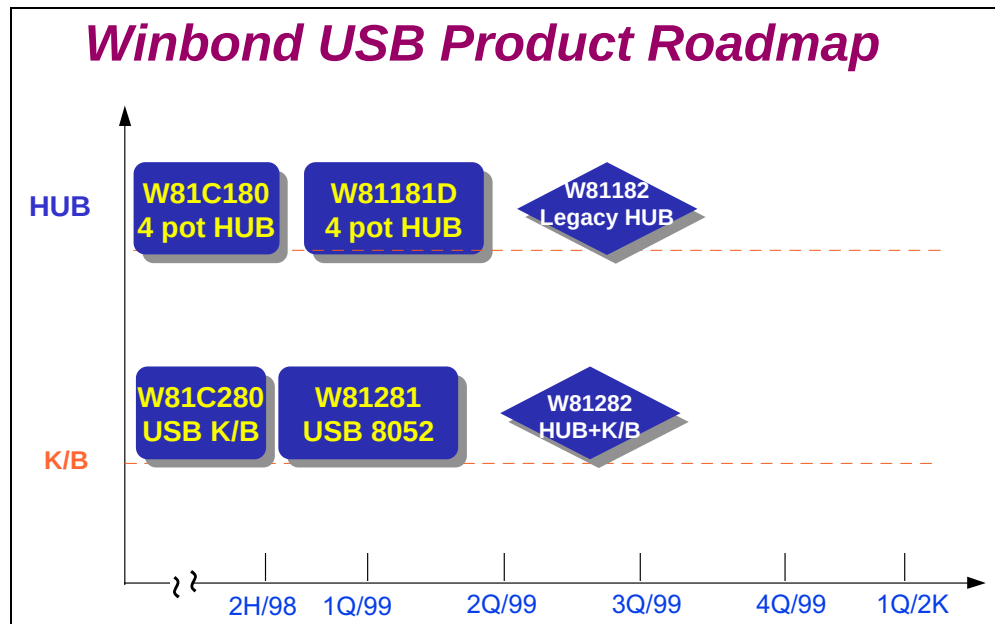


W81281

Preliminary

NOTE: The contents in the table are hexadecimal HID Code + Order Number of Legacy Keys + Legacy Scan-Code (set1 set2 set3).

Preliminary



Winbond USB Product Brief

- **W81C180: USB 4 Port Hub Controller**
- **W81181D: High Integrated USB 4 Port Hub Controller**
- **W81182:USB Legacy Hub, Translate EPP, Serial, PS/2 to USB Connection, Including 4 port USB Hub**
- **W81C280: USB K/B Controller**
- **W81281: High Integrated USB+8052 Controller or USB K/B Controller**
- **W81282:USB 4 Port Hub + K/B Controller**

Preliminary

**Headquarters**

No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: <http://www.winbond.com.tw/>

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

**Winbond Electronics
(North America) Corp.**
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.