W6694

USB Bus ISDN S/T-Controller

Data Sheet

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Revision 0.93

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1. GENERAL DESCRIPTION

The Winbond's single chip USB bus ISDN S/T interface controller W6694 is an all-in-one device suitable for ISDN Internet access. The integrated USB and ISDN design provides low cost, pure passive solution for USB-IDSN application. W6694 also provides two PCM CODEC interfaces for the ability to access ISDN through voice channel.

2. FEATURES

ISDN Features

- Full duplex 2B+D S/T-interface transceiver compatible with ITU-T I.430 Recommendation
  - ♦ Four wire operation
  - ♦ Received clock recovery
  - ♦ Layer 1 activation/deactivation procedure
  - ♦ D channel access control
- Transparent data transmission of 2B+D channels
- Test functions

USB Features

- USB Specification version 1.0/1.1 compliant
- Full-speed, bus-powered USB device
- Integrated transceiver, PLL, SIE, SIL, and voltage regulator
- Built-in fully automatic enumeration procedure
- Support suspend mode
  - ♦ Suspend current requirement
  - ♦ Wake-up by ISDN (remote) and PC (host)

Other Feature

- GCI bus interface (slave mode) for connecting to ISDN U transceiver chip.
- PCM port provides two 64K clear channels to connect to PCM CODEC chips.
- B channel data switching function for selective connection between ISDN/GCI interface, USB, and PCM.
- EEPROM interface for retrieving customized USB device identification data.
- IO pins with LED current drive capability.
- Reset pin for whole-chip reset.

3. PIN CONFIGURATION

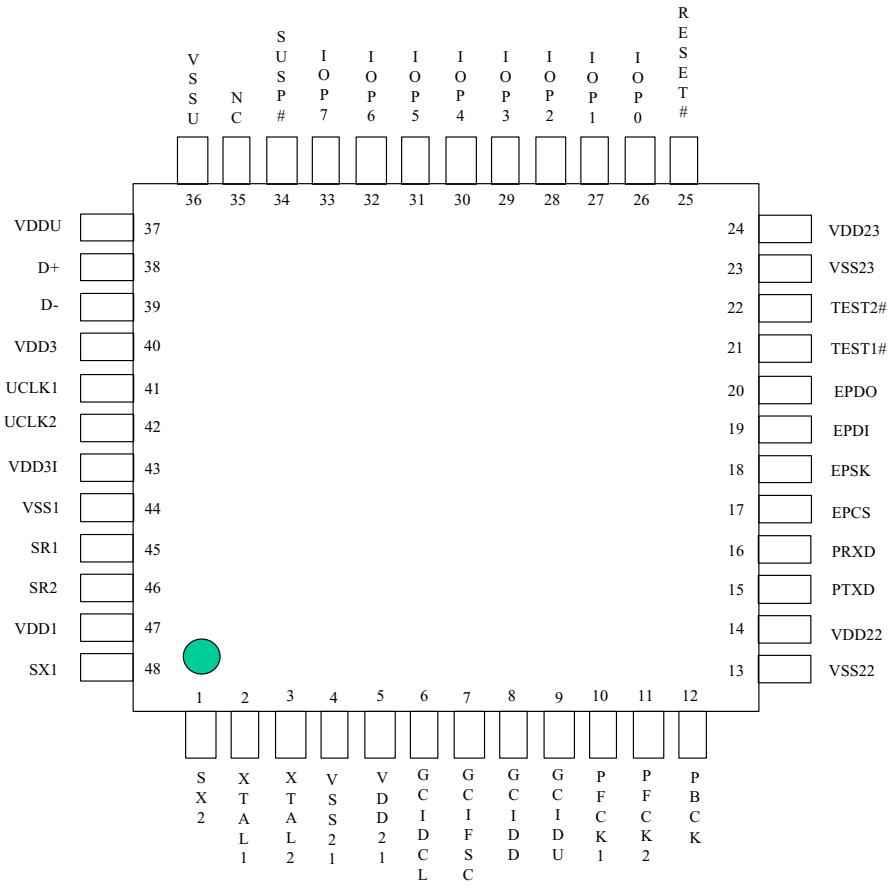


FIG.3.1 W6694 PIN OUT

4. PIN DESCRIPTION

TABLE 4.1 W6694 PIN DESCRIPTIONS

Note : The suffix # indicates active LOW signal.

Symbol	Pin No.	I/O	Function
USB Bus			
D+	38	I/O	USB D+ data line.
D-	39	I/O	USB D- data line.
UCLK1	41	I	24 MHz crystal/oscillator clock input.
UCLK2	42	O	24 MHz crystal clock output. Left unconnected if use oscillator.
ISDN Signals and External Crystal			
SR1	45	I	S/T bus receiver input (-). This is normal polarity. Reverse polarity is also OK.
SR2	46	I	S/T bus receiver input (+).
SX1	48	O	S/T bus transmitter output(+).
SX2	1	O	S/T bus transmitter output(-).
XTAL1	2	I	Crystal or Oscillator clock input. The clock frequency: 7.68MHz±100PPM.
XTAL2	3	O	Crystal clock output. Left unconnected when using oscillator.
GCI Bus			
GCIDCL	6	I	GCI bus data clock 1.536 MHz.
GCIFSC	7	I	GCI bus frame synchronization clock.
GCIDD	8	I	GCI bus data downstream. (input)
GCIDU	9	O	GCI bus data upstream. (output)
PCM Bus			
PFCK1	10	O	PCM port 1 frame synchronization signal with 8 KHz repetition rate and 8 bit pulse width
PFCK2	11	O	PCM port 2 frame synchronization signal with 8 KHz repetition rate and 8 bit pulse width
PBCK	12	O	PCM bit clock of 1.536 MHz.
PTXD	15	O	PCM data output.
PRXD	16	I	PCM data input.
External Serial EEPROM Interface			
EPCS	17	O	Serial EEPROM chip select.
EPSK	18	O	Serial EEPROM data clock.
EPDI	19	I	Serial EEPROM data input
EPDO	20	O	Serial EEPROM data output
Power and Ground			
VDD1,VSS1	47,44	I	ISDN S/T analog power (5V), Ground
VDD21,VSS21	5,4	I	Digital power (5V), Ground

VDD22,VSS22 VDD23,VSS23	14,13 24,23		
VDDU,VSSU	37,36	I	USB core power (5V), Ground
VDD3	40	O	Regulator output (3.3V)
VDD3I	43	I	Regulator input (3.3V)
IO Pins			
IOP0 IOP1 IOP2 IOP3 IOP4 IOP5 IOP6 IOP7	26 27 28 29 30 31 32 33	I/O I/O I/O I/O I/O I/O I/O I/O	IO pin capable of driving LED.
Others			
RESET#	25	I	External reset. Cause internal circuit reset and USB re-enumeration.
TEST1#,TEST2#	21,22	I	Test mode enable. Connected to HIGH for normal operation.
SUSP#	34	O	USB suspended.
NC			
NC	35		No connection.

5. SYSTEM DIAGRAM AND APPLICATIONS

Typical applications include :

- USB passive TA for data only service
- USB passive TA with one data plus one voice

6.BLOCK DIAGRAM

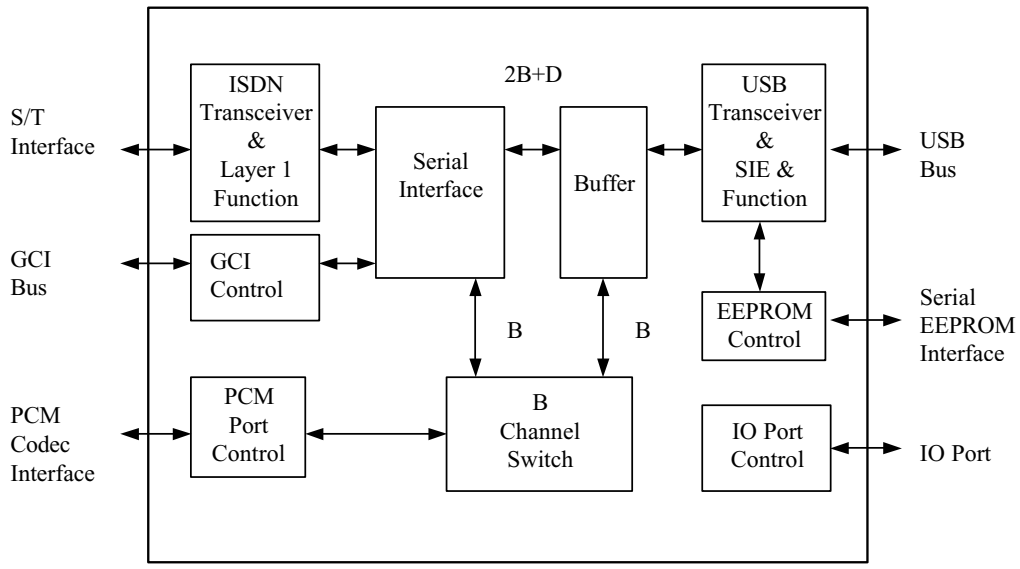


FIG 6.1 W6694 BLOCK DIAGRAM

7. FUNCTIONAL DESCRIPTIONS

7.1 USB Descriptions

TABLE 7.1 W6694 ALL USB ENDPOINTS

End Point	Type	Direction*	Max. Packet Size (Bytes)	Internal Buffer Type and Size (Bytes)
0	Control	IN/OUT	8/8	8, single port x 2
1	Bulk	OUT	8	8, single port x 1
2	Bulk	IN	8	8, single port x 1
3	Interrupt	IN	5	5, single port x 1
4	Isoch.	OUT	(1+3) + (1+18) = 23	96, dual port x 1
5	Isoch.	IN	1+ (1+7) + (1+15) + (1+15) = 41	96, dual port x 1

* Direction: IN – device to host, OUT – host to device

USB standard requests are supported by W6694, and W6694 will respond to requests according to USB specification revesion 1.1. These includes “CLEAR_FEATURE, GET_CONFIGURATION, GET_DESCRIPTOR, GET_INTERFACE, GET_STATUS, SET_ADDRESS, SET_CONFIGURATION, SET_DESCRIPTOR, SET_FEATURE, SET_INTERFACE”. The “SYNC_FRAME” request is not supported.

7.1.1 Control-IN Transactions (Endpoint 0)

7.1.1.1 Get Device Descriptor

Offset	Field	Size	Default Value (Hex)	Updated by EEPROM
0	bLength	1	12	
1	bDescriptorType	1	01	
2	bcdUSB	2	0110	
4	bDeviceClass	1	00	
5	bDeviceSubClass	1	00	
6	bDeviceProtocol	1	FF	
7	bMaxPacketSize	1	08	
8	idVendor	2	1046	Yes *
10	idProduct	2	6694	Yes *
12	bcdDevice	2	0100	Yes *
14	iManufacturer	1	00	
15	iProduct	1	01	

16	iSerialNumber	1	00	
17	bNumConfiguration	1	01	

* Note: Refer to EEPROM session for its layout of contents.

7.1.1.2 Get Configuration Descriptor

Offset	Field	Size	Value (Hex)	Remark
Configuration Descriptor				
0	bLength	1	09	
1	bDescriptorType	1	02	
2	wTotalLength	2	003E	62
4	bNumInterface	1	01	
5	bConfigurationValue	1	01	
6	iConfiguration	1	00	
7	bmAttributes	1	A0	Bus Powered, Remote Wakeup
8	MaxPower	1	32	100 mA
Interface 0 Descriptor				
0	bLength	1	09	
1	bDescriptorType	1	04	
2	bInterfaceNumber	1	00	
3	bAlternateSetting	1	00	
4	bNumEndpoints	1	00	
5	bInterfaceClass	1	00	
6	bInterfaceSubClass	1	00	
7	bInterfaceProtocol	1	FF	
8	iInterface	1	00	
Alternate Interface 0 Descriptor				
0	bLength	1	09	
1	bDescriptorType	1	04	
2	bInterfaceNumber	1	00	
3	bAlternateSetting	1	01	
4	bNumEndpoints	1	05	
5	bInterfaceClass	1	00	
6	bInterfaceSubClass	1	00	
7	bInterfaceProtocol	1	FF	
8	iInterface	1	00	
Endpoint 1 Descriptor				
0	bLength	1	07	
1	bDescriptorType	1	05	
2	bEndpointAddress	1	01	OUT
3	bmAttributes	1	02	Bulk
4	wMaxPacketSize	2	0008	

6	bInterval	1	00	
Endpoint 2 Descriptor				
0	bLength	1	07	
1	bDescriptorType	1	05	
2	bEndpointAddress	1	82	IN
3	bmAttributes	1	02	Bulk
4	wMaxPacketSize	2	0008	
6	bInterval	1	00	
Endpoint 3 Descriptor				
0	bLength	1	07	
1	bDescriptorType	1	05	
2	bEndpointAddress	1	83	IN
3	bmAttributes	1	03	Interrupt
4	wMaxPacketSize	2	0005	
6	bInterval	1	01	
Endpoint 4 Descriptor				
0	bLength	1	07	
1	bDescriptorType	1	05	
2	bEndpointAddress	1	04	OUT
3	bmAttributes	1	01	Isochronous
4	wMaxPacketSize	2	0017	
6	bInterval	1	01	
Endpoint 5 Descriptor				
0	bLength	1	07	
1	bDescriptorType	1	05	
2	bEndpointAddress	1	85	IN
3	bmAttributes	1	01	Isochronous
4	wMaxPacketSize	2	0029	
6	bInterval	1	01	

7.1.1.3 Get String Descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	04	
1	bDescriptorType	1	03	
2	wLanguage ID	2	0409	U.S. English

7.1.1.4 Get String Descriptor 1 (Product)

Offset	Field	Size (Hex)	Value (Hex)	String (UNICODE)
0	bLength	1	18	
1	bDescriptorType	1	03	
2	bString	16		“USB ISDN TA”

7.1.2 Control-OUT Transactions (Endpoint 0)

7.1.2.1 Device Clear Feature, Remote Wake-up

BmRequestType	bRequest	wValue	wIndex	wLength	Data
00H	CLEAR_FEATURE	1	0	0	None

On received this request from host, W6694 will not detect the incoming ISDN broadcast message.

7.1.2.2 Device Set Feature, Remote Wake-up

BmRequestType	bRequest	wValue	wIndex	wLength	Data
00H	SET_FEATURE	1	0	0	None

On received this request from host, W6694 will detect the incoming ISDN broadcast message. This is default setting.

7.1.2.3 Set Interface 0, Alternate Setting 1

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01H	SET_INTERFACE	0	0	0	None

On received this request from host, W6694 will reset and disable the D/B1/B2 channel XFIFO and RFIFO. This is default setting.

7.1.2.4 Set Interface 0, Alternate Setting 0

bmRequestType	bRequest	wValue	wIndex	wLength	Data
01H	SET_INTERFACE	1	0	0	None

On received this request from host, W6694 will enable the D/B1/B2 channel XFIFO and RFIFO.

7.1.3 Bulk-OUT Transaction (Endpoint 1)

Bulk-OUT endpoint is used to write data to register or/and index which register to be read in following Bulk-IN transaction. A pare of two bytes (Address, Data) in Bulk-OUT data packet represents a read or write command on one

register. A maximum of 8 bytes consist one Bulk-OUT transaction. W6694 perform the read/write commands following their order in the packet.

Data packet for Bulk-OUT transaction:

Offset 0	1	2	3	4	5	6	7
address1	data1	address2	data2	address3	data3	address4	data4

Address byte will indicate the read or write action to that register, by assigning highest order bit (bit 7) to 0 (read) or 1 (write).

Contents of address byte:

Bit 7	6	5	4	3	2	1	0
0/1	0	0	A4	A3	A2	A1	A0

Bit 7: 0/1 = Read/Write
Bit 4-0: Address offset of register.

The data byte is the write data (write operation) or 00h (read operation).

7.1.4 Bulk-IN Transaction (Endpoint 2)

Bulk-IN endpoint is for retrieving register data of W6694. It returns the registers data that are requested by most recent Bulk-OUT data-read request. Inside the data packet, one register occupies 2 bytes. The first is register's offset address, the 2nd byte is date. A maximum of 4 register data can be sent to host in one Bulk-IN packet.

Offset 0	1	2	3	4	5	6	7
address1	data1	address2	data2	address3	data3	address4	data4

7.1.5 Interrupt-IN Transaction (Endpoint 3)

Interrupt-IN endpoint is used to periodically poll device interrupt data. W6694 use this endpoint to report interrupt status of all interrupt sources. All four bytes data of interrupt registers will be sent to host if ISTA is not 0. If no interrupt is detected by W6694 when received Interrupt-IN token, A NAK token will return to USB host.

Data packet for Interrupt-IN transaction:

Offset 0	1	2	3	4
ISTA	CIR	PICR	PDATA	MOIR

7.1.6 Isochronous-OUT Transaction (Endpoint 4)

After power-on or hardware reset, all B and D channels transmit FIFO (XFIFO) are disabled. A disabled XFIFO can not receive data from USB. But the transmitter will automatically send inter frame time fill pattern (all 1's) to ISDN

interface. The disabled XFIFO can be enabled by command XEN on each channel. An enabled XFIFO can receive data from USB, and send data to USB host.

Software decides the size of data to transmit depending on available XFIFO space, which is indicated by XFR flag carried by Isochronous-IN packet. When XFR is reported to host, it means that XFIFO has at least half of the total XFIFO size available for that channel. Each channel has its own XFIFO and status flags.

If the incoming Isochronous-OUT packet is detected error, some action will be automatically taken for D and B channel XFIFO. For D channel, the XFIFO is reset and automatically enabled. For B channel, the XFIFO are not reset, and the data remained in XFIFO are still valid and will be transmitted to ISDN later. But the new incoming B channel data will be replaced by FFh, and stored into XFIFO. The continuous FFh will later be transmitted to corresponding B channel of ISDN interface. This Isochronous-OUT packet error will be reported to host, by setting bit ISOE of Isochronous-IN packet to 1. D channel FIFO will recognize and only accept data within HDLC frame (including opening and closing flag), all other data outside HDLC frame are ignored and not stored in FIFO. B channel FIFO accept any data after it is enabled.

The packet format of Isochronous-OUT is as below:

Bit 7	6	5	4	3	2	1	0
						D_LEN1	D_LEN0
D_DATA (1st byte)							
D_DATA (2nd byte)							
D_DATA (3rd byte)							
				B_LEN3	B_LEN2	B_LEN1	B_LEN0
B1_DATA							
...							
B2_DATA							
...							

D_LEN1-0 D Channel Data Length

These bits indicate the data length of the subsequent data for D channel. The length should be from 1 and 3 bytes inclusively, otherwise a transmit FIFO under-run or overflow condition may occur. The valid data are HDLC frame, including opening and closing flag (7Eh), and bit-stuffed data in between. Note that software should transmit the first data byte as opening flag in byte (8-bits) boundary. Due to the nature of HDLC framing, the closing flag may not be in byte-boundary. Software should stuff the remaining bit positions (if any) with binary '1', to fill the last byte, unless the last byte is 7Eh.

D_DATA D Channel Data

These are D channel data space, which always occupy 3 bytes in the packet. Software should put actual data length in D_LEN. If the data length is less then 3, the remaining bytes position should fill with FFh.

B_LEN3-0 B Channel Data Length

These bits indicate the data length of subsequent data for each B channel. The length should be from 7 to 9 bytes inclusively, otherwise a transmit FIFO under run or overflow condition may occur. Note that two B channels have same data length.

B1_DATA B1 Channel Data

These are B1 channel data, the length is indicated by B_LEN.

B2_DATA B2 Channel Data

These are B2 channel data, the length is indicated by B_LEN.

7.1.7 Isochronous-IN Transaction (Endpoint 5)

After power on or reset, all B and D channels receive FIFO (RFIFO) are disabled. A disabled RFIFO can not receive data from ISDN, and will always return zero-length data for Isochronous-IN transaction. RFIFO can only be enabled by command CMDR:REN. Once enabled, an Isochronous-IN transaction can read data from RFIFO of that channel. The data packet also carries XFIFO status for that channel, and the most recent Isochronous-OUT packet error status (if error ever occurred).

The packet format of Isochronous-IN is as below:

Bit 7	6	5	4	3	2	1	0
ISOE							
D_XFR	D_XCOL	D_XDOV	D_XDUN	D_RDOV	D_LEN2	D_LEN1	D_LEN0
D_DATA							
...							
B1_XFR	B1_XDOV	B1_XDUN	B1_RDOV	B1_LEN3	B1_LEN2	B1_LEN1	B1_LEN0
B1_DATA							
...							
B2_XFR	B2_XDOV	B2_XDUN	B2_RDOV	B2_LEN3	B2_LEN2	B2_LEN1	B2_LEN0
B2_DATA							
...							

ISOE Isochronous-OUT Error
This bit is set to indicate that the most recent received Isochronous-OUT packet has CRC error. This bit will remain set, until a CMDR1:CISOE clears it.

XCOL Transmit Collision (D channel only)
This bit indicates a D channel collision on the S-bus has been detected. The data in D channel XFIFO will be automatically re-transmitted, until the whole HDLC frame are successfully transmitted. This bit will remain set, until software issue CMDR1:DXEN to clear this bit.

XFR Transmit FIFO Ready
It is set when XFIFO has at least half of the XFIFO size available for incoming USB data.

XDUN Transmit Data Under-run
The corresponding XFIFO has run out of data. For D and B channel, the XFIFO is reset and disabled for that channel. This bit is cleared when XFIFO is enabled by XEN bit.

XDOV Transmit Data Overflow
The corresponding XFIFO has overflow condition. Data in XFIFO are overwritten by incoming USB data. For D and B channel, the XFIFO is reset and disabled for that channel. This bit is cleared when XFIFO is enabled by XEN bit.

RDOV Receive Data Overflow
The corresponding RFIFO has overflow condition. Data in RFIFO are overwritten by incoming ISDN data. When overflow condition occurred, the D and B channel RFIFO is reset and disabled for that channel. This bit is cleared when RFIFO is enabled by REN bit.

7.1.8 Suspend and Resume

W6694 supports USB suspend and resume function as described in USB specification 1.1. When there is more than three millisecond period of inactivity on the USB, W6694 will automatically enter into a low-power suspend state. In this state, most of the ISDN and USB module will be powered off to consume minimum power. But the internal register values are preserved. Therefore it is recommended that the software perform necessary control to W6694 before power-down. The W6694 will leave suspend mode only when one of the two condition happens: host or device wake-up. A ISTA:WAKE bit will indicate to software which source the wake-up event is originated from.

(i). Host-Initiated Wake-up

The USB host may wake-up W6694 by sending traffic on USB. On detected this wake-up signal, W6694 will automatically resume to normal operation.

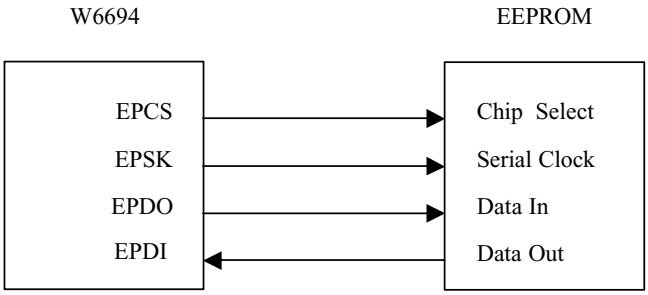
(ii). Device Remote Wake-up

In suspend mode, W6694 will ignore any ISDN traffic on S/T bus, except for incoming broadcast messages. When there is an incoming broadcast message from ISDN switch, such as SETUP message, W6694 will automatically wake-up, and signal USB host that it has left suspend mode. The first few bytes of SETUP message will be saved in D channel RFIFO. After returning from suspend mode, software should immediately read the RFIFO, and perform necessary operation as specified in ISDN protocol.

7.2 Configuration EEPROM

A 9346/93C46 type serial EEPROM can be used to store customized USB device configuration data. These configuration data will be read by W6694 after power on or reset, and sent to USB host during enumeration. If EEPROM is not presented, or the first 16 bits in EEPROM is FFFFh, the default value in W6694 will be sent to USB host instead.

EEPROM wire connection :



EEPROM Contents :

Offset	Size (Byte)	Contents 15 0
0	2	Vendor ID
2	2	Device ID
4	2	Device release number

8. REGISTER DESCRIPTIONS

8.1 Interrupt Registers

These registers will be read by Interrupt-IN packet only, so USB host will periodically receive these data. These registers can not be read by Bulk-IN transfer.

8.1.1 Interrupt Status Register ISTA Read_clear

This register indicates interrupt occurred in various interrupt sources. This register is cleared automatically after it is read and successfully ACKed by USB host.

Values after reset: 00h

7	6	5	4	3	2	1	0
ICC	MOC	PIOIC	0	0	0	0	WAKE

ICC Layer 1 Indication Code Change
A change of value in the received indication code has been detected. The new code is in Layer 1 Command/Indication Register (CIR) register.

MOC Monitor Channel Status Change
A change of value in the GCI mode Monitor Channel Interrupt Register (MOIR) has occurred.

PIOIC Programmable IO Port Input Signal Changed
A change of value in at least one input IO pin is detected. The input IO pins that change value can be identified in PIO Input Change Register (PICR) register.

WAKE Device Remote Wake-Up
This bit indicates that W6694 has left suspend mode by detecting a broadcast SETUP message from ISDN switch. D channel receive FIFO (RFIFO) has buffered the first few bytes of SETUP message. Software should issue Isochronous-IN transaction to read this message.

8.1.2 Layer 1 Command/Indication Register CIR Read

Value after reset: 0Fh

7	6	5	4	3	2	1	0
0	0	0	0	CIR3	CIR2	CIR1	CIR0

CIR3-0 Layer 1 Indication Code

Value of the received layer 1 indication code for S/T interface. Note these bits have a buffer size of two.

Note: If S/T layer 1 function is disabled and GCI bus is enabled (GE=1 in GCR register), CIR register is used to receive layer 1 indication code from U transceiver. In this case, the supported indication codes are :

Indication	Symbol	Code	Descriptions
Deactivation confirmation	DC	1111	Idle code on GCI interface
Power up indication	PU	0111	U transceiver power up

8.1.3 Monitor Channel Interrupt Status MOIR Read_clear

Value after reset: 00h

7	6	5	4	3	2	1	0
0	0	0	0	MDR	MER	MDA	MAB

MDR Monitor Channel Data Receive
MER Monitor Channel End of Reception
MDA Monitor Channel Data Acknowledged
MAB Monitor Channel Data Abort

8.1.4 PIO Input Change Register PICR Read_clear

Value after reset: 00h

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P7-0 Indicator of IO Pin Input Status

0: This IO pin is either output pin, or did not change input value.
1: This IO pin changed value.

NOTE : Registers in sections 8.2 to 8.5 are written/read by Bulk-OUT/Bulk-IN transactions.

8.2 Chip and FIFO Control Registers

8.2.1 Interrupt Mask Register IMASK Read/Write Address 00h

Value after reset: E1h

7	6	5	4	3	2	1	0
ICC	MOC	PIOIC	0	0	0	0	WAKE

Setting '1' to each bits masks the corresponding interrupt sources in ISTA register.

8.2.2 Command Register 1 CMDR1 Write Address 01h

Value after reset: 00h

Writing 1 to the following bits will activate each corresponding function. Writing 0 to these bits has no effect.

7	6	5	4	3	2	1	0
DXRST	DRRST	DXEN	DREN	SRST	CISOE	DLP	RLP

DXRST D Channel Transmitter Reset

Setting this bit resets D channel transmitter, and clear transmit FIFO (XFIFO). The transmitter will immediately transmit inter frame time fill pattern (all 1's) to D channel in ISDN layer 1, but the XFIFO is disabled (not active). Software must issue DXEN to enable (activate) D channel XFIFO. After reset is done, this bit becomes 0. If this bit and other bits are set at the same time, the reset action will be performed first and completed, then other actions will follow.

DRRST D Channel Receiver Reset

Setting this bit resets D channels receiver, and clear receive FIFO (RFIFO). The D channels is disabled (not active). Software must issue DREN to enable (activate) D channel RFIFO, in order to receive D channel data from ISDN, and send data to USB. After reset is done, this bit becomes 0. If this bit and other bits are set at the same time, the reset action will be performed first and completed, then other actions will follow.

DXEN D Channel Transmit FIFO Enable

Setting this bit enables D channel transmit FIFO (XFIFO). After enabled, the D channel XFIFO will begin to receive D channel data from USB, and send data to ISDN. After enabled, this bit becomes 0.

DREN D Channel Receive FIFO Enable

Setting this bit enables D channel receive FIFO (RFIFO). After enabled, the D channel RFIFO will begin to receive D channel data from ISDN, and send data to USB. After enabled, this bit becomes 0.

SRST Software Reset

Setting this bit internally generates a software reset signal. The effect of this reset signal is equivalent to hardware reset pin, except that the USB circuit and all USB configured data are not reset. After reset is done, this bit becomes 0. This bit must be set along, i.e., all other bits in this register must not set at the same time.

CISOE Clear Isochronous-OUT Error

Setting this bit clears error indication bit ISOE of Isochronous-OUT error. This bit is carried by Isochronous-IN packet. After bits are cleared, this bit becomes 0.

DLP Digital Loopback

Setting this bit activates the digital loopback function. The transmitted digital 2B+D channels are looped to the received 2B+D channels. Note that after hardware reset, the internal clocks will turn off if the S bus is not connected or if there is no signal on the S bus. In this case, the C/I command ECK must be issued to enable loopback function. This bit remains set, until cleared by software reset (SRST).

RLP Remote Loopback

Setting this bit activates the remote loopback function. The received 2B channels from the S interface are looped to the transmitted 2B channels of S/T interface. The D channel is not looped in this loopback function.
This bit remains set, until cleared by software reset (SRST).

8.2.3 Command Register 2 CMDR2 Write Address 02h

Value after reset: 00h

Bits in this register act similar to that of CMDR1 register, except that the effect is on B1 or B2 channel XFIFO/RFIFO, instead of on D channel XFIFO/RFIFO.

7	6	5	4	3	2	1	0
B1XRST	B1RRST	B1XEN	B1REN	B2XRST	B2RRST	B2XEN	B2REN

B1XRST **B1 Channel Transmitter Reset**
B1RRST **B1 Channel Receiver Reset**
B1XEN **B1 Channel Transmit FIFO Enable**
B1REN **B1 Channel Receive FIFO Enable**
B2XRST **B2 Channel Transmitter Reset**
B2RRST **B2 Channel Receiver Reset**
B2XEN **B2 Channel Transmit FIFO Enable**
B2REN **B2 Channel Receive FIFO Enable**

8.2.4 Control Register CTL Read/Write Address 03h

Value after reset : 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OPS1	OPS0

OPS1-0 Output Phase Delay Compensation Select1-0

These two bits select the output phase delay compensation.

OPS1	OPS0	Effect
0	0	No output phase delay compensation
0	1	Output phase delay compensation 260ns

1	0	Output phase delay compensation 520 ns
1	1	Output phase delay compensation 1040 ns

8.2.5 Layer 1 Command/Indication Register CIX Read/Write Address 04h

Value after reset: 0Fh

7	6	5	4	3	2	1	0
0	0	0	0	CIX3	CIX2	CIX1	CIX0

CIX3-0 Layer 1 Command Code

Value of the command code transmitted to layer 1. A read to this register returns the previous written value.

Note: If S/T layer 1 function is disabled and GCI bus is enabled (GE=1 in GCR register), CIX register is used to issue layer 1 command code to U transceiver. In this case, the supported command code is:

Command	Symbol	Code	Descriptions
Activate request command	AR	1000	Activate request command

8.2.6 U-layer1 Ready Code L1_RC Read/Write Address 05h

Value after reset: 0Ch

7	6	5	4	3	2	1	0
0	0	0	0	RC3	RC2	RC1	RC0

RC3-0 Ready Code

When GCI bus is being enabled, these four programmable bits are allowed to program different Layer 1_Ready Code (AI: Activation Indication) by user. For example: Siemens PEB2091: AI=1100, Motorola MC145572: AI=1100.

8.3 GCI Mode Registers

8.3.1 GCI Mode Command Register GCR Read/Write Address 06h

Value after reset: 00h

7	6	5	4	3	2	1	0
MAC	0	0	TLP	GRLP	SPU	PD	GE

MAC Monitor Transmit Channel Active (Read Only)

Data transmission is in progress in GCI mode Monitor channel.

0: The previous transmission has been terminated. Before starting a transmission, software should verify that the transmitter is inactive.

1: The previous transmission is in progress.

TLP Test Loopback
When set this bit both the GCIDU and GCIDD lines are internally connected together. The GCI mode loopback test function: GCIDU is internally connected with GCIDD, external input on GCIDD is ignored.

GRLP GCI Mode Remote Loopback
Setting this bit to 1 activates the remote loopback function. The 2B+D channels data received from the GCI bus interface are looped to the transmitted channels.

SPU Software Power Up
PD Power Down

SPU	PD	Description
0	1	After U transceiver power down, W6694 will receive the indication DC (Deactivation Confirmation) from GCI bus and then software has to set SPU → 0, PD →1 to acknowledge U transceiver, by pulling GCIDU line to HIGH. W6694 remains normal operation.
1	0	Setting SPU → 1, PD →0 will pull the GCI bus GCIDU line to LOW. This will enforce connected layer 1 devices (U transceiver) to deliver GCI bus clocking.
0	0	After reception of the indication PU (Power Up indication) the reaction of the microprocessor should be: - To write an AR (Activate Request command) as C/I command code in the CIX register. - To reset the SPU bit and wait for the following ICC (indication code change) interrupt.
1	1	Unused.

GE GCI Mode Enable
Setting this bit to 1 will enable the GCI bus interface. In the same time, the S/T layer 1 function is disabled.

8.3.2 Monitor Channel Control Register MOCR Read/Write Address 07h

Value after reset: 00h

7	6	5	4	3	2	1	0
0	0	0	0	MRIE	MRC	MXIE	MXC

MRIE Monitor Channel 0 Receive Interrupt Enable
Monitor channel interrupt status MDR, MER generation is enabled (1) or masked (0).

MRC MR Bit Control
Determines the value of the MR bit:
0: MR bit always 1. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRIE=1).
1: MR internally controlled according to Monitor channel protocol. In addition, the MDR interrupt is enabled for all bytes according to the Monitor channel protocol (if MRIE=1).

MXIE Monitor Channel Transmit Interrupt Enable
Monitor interrupt status MDA, MAB generation is enabled (1) or masked (0).

MXC MX Bit Control
Determines the value of the MX bit:
0: MX always 1.

1: MX internally controlled according to Monitor channel protocol.

8.3.3 Monitor Channel Receive Register MOR Read Address 08h

Value after reset: FFh

7	6	5	4	3	2	1	0

8.3.4 Monitor Channel Transmit Register MOX Read/Write Address 09h

Value after reset: FFh

7	6	5	4	3	2	1	0

8.4 Programmable IO Registers

8.4.1 PIO Input Enable Register PIE Read/Write Address 0Ah

Value after reset: 00h

7	6	5	4	3	2	1	0
IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0

IE7-0 Input Enable for IO Pin 7-0.
Setting these bits enable corresponding IO pin to become input pin. Default is output pin.

8.4.2 PIO Output Register 1 PO1 Read/Write Address 0Bh

Value after reset: 01h

7	6	5	4	3	2	1	0
OM3_1	OM3_0	OM2_1	OM2_0	OM1_1	OM1_0	OM0_1	OM0_0

OMn_1-0 Output Mode of IO Pin n (n=3..0).
Setting corresponding bits drive output pin with different output mode.
Possible modes are:
00: always LOW
01: 0.5 second HIGH/LOW cycle
10: 1 second HIGH/LOW cycle
11: always HIGH
These bits have no effect on input pin.

8.4.3 PIO Output Register 2 PO2 Read/Write Address 0Ch

Value after reset: 00h

7	6	5	4	3	2	1	0
OM7_1	OM7_0	OM6_1	OM6_0	OM5_1	OM5_0	OM4_1	OM4_0

OMn_1-0 Output Mode of IO Pin n (n=7..4).

8.4.4 PIO Data Register PDATA Read Address 0Dh

Value after reset: 00h

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

D7-0 Read Data of IO Pins 7-0

The corresponding bits are the present values of IO pins 7-0 (LOW=0, HIGH=1).

8.5 B Channel Switch Registers

8.5.1 Layer1 B1 Receiver Select Register L1B1RS Read/Write Address 0Eh

Value after reset: 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	RS2	RS1	RS0

RS2-0 Receiver Select

These bits select the source where layer 1 B1 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
010 (2): receive from Layer1 B1
100 (4): receive from USB B1

8.5.2 Layer1 B2 Receiver Select Register L1B2RS Read/Write Address 0Fh

Value after reset: 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	RS2	RS1	RS0

RS2-0 Receiver Select

These bits select the source where layer 1 B2 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
011 (3): receive from Layer1 B2
101 (5): receive from USB B2

8.5.3 USB B1 Receiver Select Register USBB1RS Read/Write Address 10h

Value after reset: 02h

7	6	5	4	3	2	1	0
0	0	0	0	0	RS2	RS1	RS0

RS2-0 Receiver Select

These bits select the source where USB B1 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
010 (2): receive from Layer1 B1
100 (4): receive from USB B1

8.5.4 USB B2 Receiver Select Register USBB2RS Read/Write Address 11h

Value after reset: 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	RS2	RS1	RS0

RS2-0 Receiver Select

These bits select the source where USB B2 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
011 (3): receive from Layer1 B2
101 (5): receive from USB B2

8.5.5 PCM1 Receiver Select Register PCM1RS Read/Write Address 12h

Value after reset: 00h

7	6	5	4	3	2	1	0
0	0	0	0	EPCM	RS2	RS1	RS0

EPCM Enable PCM Transmit/Receive

0: Disable data transmit/receive to/from PCM port. The frame synchronization clock is held LOW. The bit synchronization clock is LOW if both PCM ports are disabled.
1: Enable data transmit/receive to/from PCM port. The frame synchronization clock is active. The bit synchronization clock is active.

RS2-0 Receiver Select

These bits select the source where PCM1 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
010 (2): receive from Layer1 B1
100 (4): receive from USB B1

8.5.6 PCM2 Receiver Select Register PCM2RS Read/Write Address 13h

Value after reset: 00h

7	6	5	4	3	2	1	0
0	0	0	0	EPCM	RS2	RS1	RS0

EPCM Enable PCM Transmit/Receive

0: Disable data transmit/receive to/from PCM port. The frame synchronization clock is held LOW. The bit synchronization clock is held LOW if both PCM ports are disabled.
1: Enable data transmit/receive to/from PCM port. The frame synchronization clock is active. The bit synchronization clock is active.

RS2-0 Receiver Select

These bits select the source where PCM2 channel will receive data from. Possible values are:
000 (0): receive from PCM1
001 (1): receive from PCM2
011 (3): receive from Layer1 B2
101 (5): receive from USB B2

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Rating

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	-0.4 to V_{DD}+0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Maximum voltage on V_{DD}	V_{DD}	6	V

9.2 Power Supply

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
5V Input voltage	V_{DD}	4.75	5.0	5.25	V	Pins VDD1, VDD21, VDD22, VDD23, VDDU
3.3V regulator output	V_{DD3}		3.3		V	Pins VDD3I, VDD3
Analog ground	V_{SSA}		0		V	Pins VSS1
Digital ground	V_{SSD}		0		V	Pins VSS21, VSS22, VSS23, VSSU

9.3 DC Characteristics

T_A=0 to 70 °C; V_{DD}=5 V ± 5 %, V_{SSA}=0 V, V_{SSD}=0 V

Parameter	Symbol	Min	Max	Unit	Test conditions	Remarks
Low input voltage	V_{IL}	-0.4	0.8	V		
High input voltage	V_{IH}	2.0	V_{DD} +0.4	V		
Low output voltage	V_{OL}		0.4	V	I_{OL}= 12 mA	
High output voltage	V_{OH}	2.4		V		
Power supply current: suspended	I_{CC}			mA	V_{DD}=5V, S/T layer 1 in state "F3 Deactivated without clock", USB in suspended mode	
Power supply current: activated	I_{CC}			mA	V_{DD}=5V, S/T layer 1 in state "F7 Activated", USB is configured and active	
Absolute value of output pulse amplitude (V_{SX2}-V_{SX1})	V_X	2.03 2.10	2.31 2.39	V V	R_L=50 Ω [1)] R_L=400 Ω [1)]	SX1,2
Transmitter output current	I_X	7.5	13.4	mA	R_L=5.6 Ω [1)]	SX1,2
Transmitter output impedence	R_X	30 23		kΩ Ω	Inactive or during binary ONE During binary ZERO (R_L=50 Ω)	SX1,2

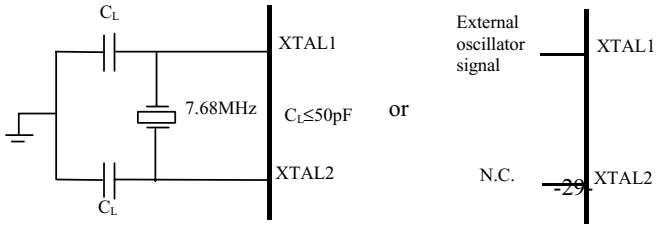
Note: [1)] Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances of ISDN pins

T_A=25 °C, V_{DD}= 5 V ± 5 %, V_{SSA}= 0V, V_{SSD}=0V, fc=1 Mhz, unmeasured pins grounded.

Parameter	Symbol	Min.	Max.	Unit	Remarks
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_L		50	pF	XTAL1,2

Recommended oscillator circuits



Publication Release Date: March., 2000
Revision 0.93

Crystal specifications

Parameter	Symbol	Values	Unit
Frequency	*f*	7.680	MHz
Frequency calibration tolerance		Max. 100	ppm
Load capacitance	C_L	Max. 50	pF
Oscillator mode		Fundamental	

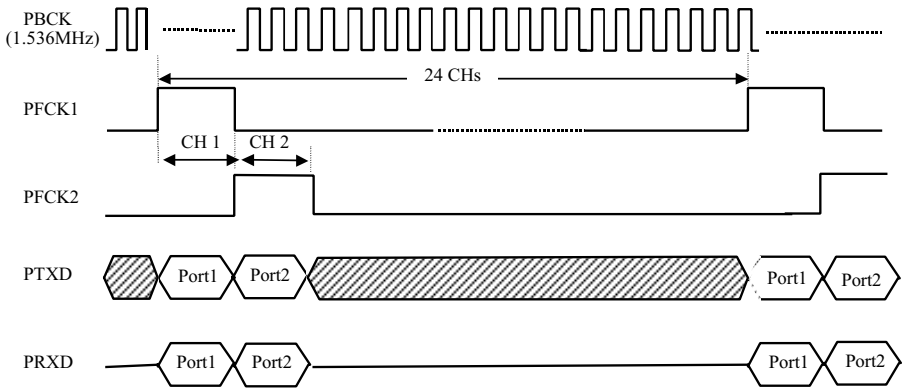
Note: The load capacitance C_L depends on the crystal specification. The typical values are 33 to 47 pF.

External ocsillator input (XTAL1) clock characteristics

Parameter	Min.	Max.
Duty cycle	1:2	2:1

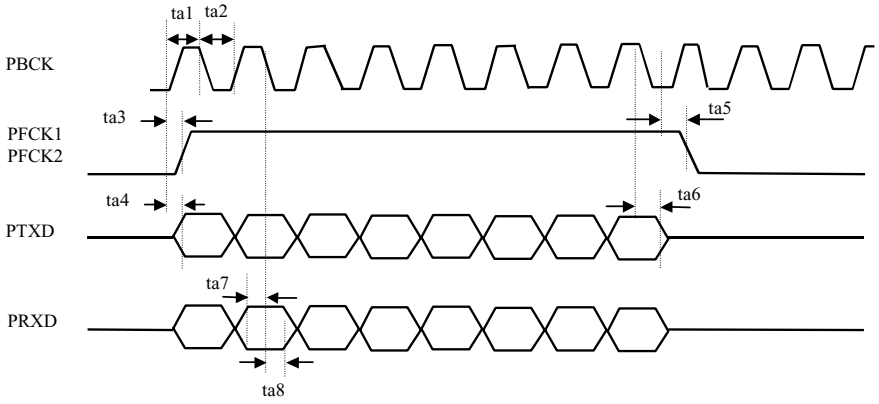
9.4 Preliminary Switching Characteristics

9.4.1 PCM Interface Timing



Note 1: These drawings are not to scale.
Note 2 : The frequency of PBCK is 1536 kHz which includes 24 channels of 64 kbps data. The PFCK1 and PFCK2 are located at channel 1 and channel 2, each with a 8 x PBCK duration.

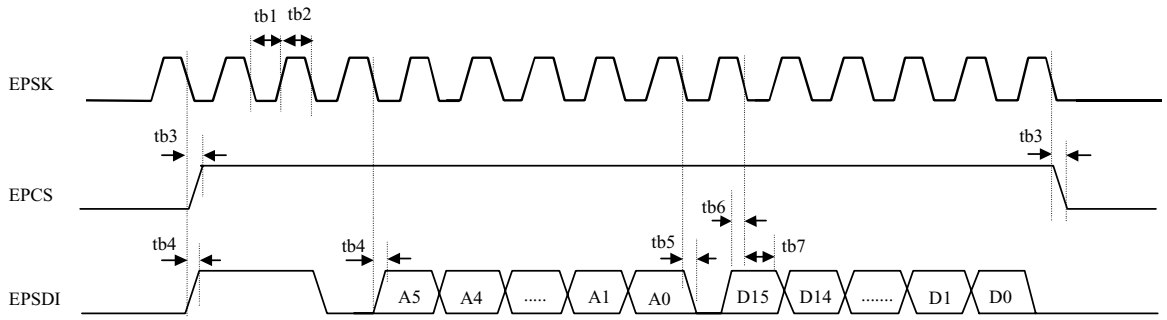
Detailed PCM timing



Parameter	Parameter Descriptions	Min.	Nominal	Max.	Remarks
ta1	PBCK pulse high		325		Unit = ns
ta2	PBCK pulse low	195	325	455	
ta3	Frame clock asserted from PBCK			20	
ta4	PTXD data delay from PBCK			20	
ta5	Frame clock deasserted from PBCK			20	
ta6	PTXD hold time from PBCK	10			
ta7	PRXD setup time to PBCK	20			
ta8	PRXD hold time from PBCK	10			

Note : The PCM clocks are locked to the S/T receive clock. At every two or three PCM frame time (125 μs), PBCK and PFCK1, PFCK2 may be adjusted by one local oscillator cycle (130 ns) in order to synchronize with S/T clock. This shift is made on the LOW level time of PBCK and the HIGH level time is not affected. This introduces jitters on the PBCK, PFCK1 and PFCK2 with jitter amplitude 260 ns (peak-to-peak) and jitter frequency about 2.67~4 kHz.

9.4.2 Serial EEPROM Timing



Parameter	Parameter Descriptions	Min.	Max.	Remarks
tb1	EPSK low	2500		Unit = ns
tb2	EPSK high	2500		
tb3	EPCS output delay		30	
tb4	EPSD output delay		30	
tb5	EPSD tri-state delay		30	
tb6	EPSD input setup time	30		
tb7	EPSD input hold time	30		