Winbond Electronics Corp.

Voice Synthesizer
(ROM-LESS High Fidelity PowerSpeech ™)

GENERAL DESCRIPTION

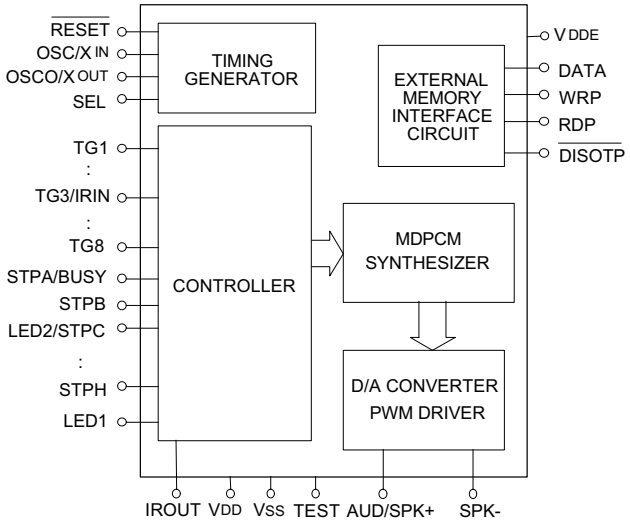
The High Fidelity PowerSpeech™ family is a new member of the PowerSpeech™ synthesizer series, with voice quality which is even better than before. The W58300 is a ROMless chip that can support up to maximal 16M bits memory size; the voice length can reach 8.5 minutes. Combined with flash memory W55Fxx, this chip can be used to demonstrate real chip function before mass-production.

This family has adopted the same architecture as the PowerSpeech™ synthesizers while replacing the 4-bit ADPCM algorithm with Winbond's high fidelity synthesis algorithm to produce better quality voice. W58300 provides hardware Infrared(IR) circuit, CPU interface and voice output in D/A converter (DAC) or PWM type.

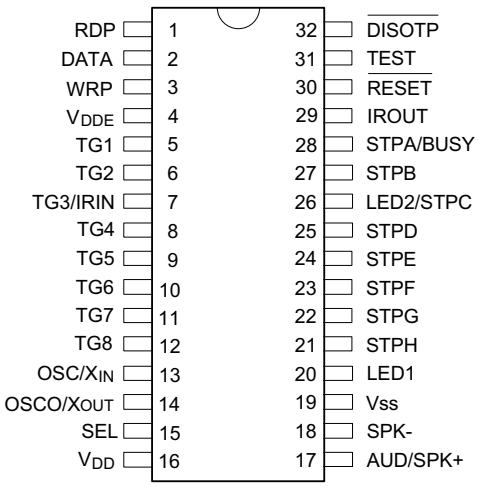
FEATURES

- Programmable voice synthesizer
- Proprietary synthesis algorithm
- Direct drive speaker by PWM output or by 8-bit DAC with external transistor
- Wide operating voltage range: 2.4–5.5 Volts
- Addressing capability up to 16M bits
- IR interface for command Transmission and Receiving
- TX, INC and MV instruction provided
- 8 trigger inputs - with separate control of falling/rising edge trigger
- 8 STOP outputs
- Supports CPU interface operation
- Pad option for Ring or Crystal oscillator
- Symbolic compiler supported
- Instruction cycle ≤ 400 μS typically
- Section control
  - Variable frequency: 4.8/6/8/12 KHz
  - LED: ON/OFF
- Eight general-purpose registers R0–R7
- Number of interrupt vector/label up to 2,048

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
TG1	I	Direct trigger input 1, internally pulled high
TG2	I	Direct trigger input 2, internally pulled high
TG3/IRIN	I	Direct trigger input 3 or IR input, internally pulled high. Once this pin is pulled low, the oscillation circuit will be active, even in the standby mode.
TG4	I	Direct trigger input 4, internally pulled high
TG5	I	Direct trigger input 5, internally pulled high
TG6	I	Direct trigger input 6, internally pulled high
TG7	I	Direct trigger input 7, internally pulled high
TG8	I	Direct trigger input 8, internally pulled high
LED1	O	LED1 output
STPA/BUSY	O	Stop signal A or Busy signal
STPB	O	Stop signal B
LED2/STPC	O	LED2 output or Stop signal C
STPD	O	Stop signal D
STPE	O	Stop signal E
STPF	O	Stop signal F
STPG	O	Stop signal G
STPH	O	Stop signal H
IROUT	O	IR signal output pin, active low
V_{SS}	-	Negative power supply
$\overline{RESET}$	I	Reset all, functions as POR, internally pulled high
AUD/SPK+	O	Current type output or PWM output for speaker
SPK-	O	PWM output
V_{DDE}	-	Positive power supply for serial interface
V_{DD}	-	Positive power supply
OSC/X_{IN}	I	Ring oscillator input or crystal input
OSCO/X_{OUT}	O	Ring oscillator clock output or crystal clock output
SEL	I	Ring/Crystal oscillator select, internally pulled high. Floating for Ring and grounded for crystal.
TEST	I	Test pin, internally pulled low
RDP	O	READ pulse clock output for serial interface
DATA	I/O	DATA pin for the serial interface
WRP	O	WRITE pulse clock output for serial interface
$\overline{DISOTP}$	I	Disable all of the serial interface pins

FUNCTIONAL DESCRIPTION

The High Fidelity PowerSpeech™ is a derivative of Winbond's PowerSpeech™ synthesizers, which are becoming dominant in the consumer market, especially for toy applications.

There are 8 trigger inputs and 8 STOP outputs in W58300. The maximal number of software key pad by scanning matrix is up to 8 × 9 = 72 keys. There are 8 general purpose registers, R0–R7. R0–R7 can apply not only for "LD" and "JP" instruction but also for "MV" instruction. Only R0 can apply for "INC" instruction. CPU interface is the same as the W581xx series. IR interface is a new feature in PowerSpeech™. You can use IR interface to transmit and receive a command. For example, when X chip executes the "TX R1" instruction, the Pulse Position Modulation waveform (with 38 KHz carrier) outputs from IROUT pin to drive a photo diode. Y chips within a certain distance will receive the IR signal through an IR receiver module to TG3 pin and execute a "JP" to the interrupt vector/label pointed by R1 of X chip.

There are two kinds of events that can cause the W58300 to enter the POI (Power On Initialization) process: one is power on, and the other is direct trigger from $\overline{\text{RESET}}$ pin. The interrupt vector "32" is allocated for this special event, and has the 1st priority, i.e., no triggers can override the POI process if they all happen simultaneously. So the user can write a program in this interrupt vector to set the power on initial state. If the user does not wish to execute a program on power on, he should write an "END" instruction in interrupt vector "32". During the POI process, triggers can then override it successfully; if the EN0, EN1 and MODE0, MODE1 registers are set properly.

If more than two events happen simultaneously, the priority that is set by the internal H/W is: POI > TG1F > TG1R > TG2F > TG2R > TG3F > TG3R > TG4F > TG4R > TG5F > TG5R > TG6F > TG6R > TG7F > TG7R > TG8F > TG8R > "JP" instruction.

Register Definition and Control

The register file of the W58300 is composed of 14 registers, including 8 general purpose registers and 6 special purpose registers. They are defined to facilitate the operations for various purposes. The default setting values of the registers are given in the following table.

REGISTER	NAME	DEFAULT SETTING
General Register	R0–R7	00100000B
Special Register	EN0, EN1	11111111B
	MODE0, MODE1	11111111B
	STOP	11111111B
	PAGE	00000000B

1. MODE0 Register

BIT	DESCRIPTION	DEFINITION
7	LED Mode	1: Flash
		0: DC

1. MODE0 Register, continued

BIT	DESCRIPTION	DEFINITION
6	LED2/STPC Pin Selection	1: LED2 Output
		0: STPC Output
5	IR Output Source	1: Hardware Control IR Output
		0: STPC Control IR Output
4	Debounce Time	1: Long
		0: Short
3, 1, 0	Reserved	-
2	STPA/BUSY Pin Selection	1: STPA Output
		0: BUSY Output

MODE0.7 controls the output type of LED1 (and LED2) pin. MODE0.6 controls the configuration of LED2/STPC pin. MODE0.5 controls the output source of IR. If hardware control IR output is selected, IR output can have signal with carrier or without carrier which is selected by MODE1.0. MODE0.4 controls the trigger pin debounce time. MODE0.2 controls the behavior of the STPA/BUSY pin which is usually used as Busy signal in CPU mode.

2. MODE1 Register

BIT	DESCRIPTION	DEFINITION
7, 6, 1	Reserved	-
5	LED Flash Type	1: Alternate
		0: Synchronous
4	LED1 Section Control	1: YES
		0: NO
3	LED2 Control	1: Section Control
		0: STPC Control
2	LED1 Volume Control	1: OFF
		0: ON
0	IR Output Format	1: IR Output Carrier with Duty Cycle 75%
		0: IR Output Without Carrier

MODE1.5 is for LED flash type control. MODE1.4 is for LED1 section control ON/OFF. MODE1.3 is for LED2 Section/STPC control. MODE1.2 is for LED1 volume control. MODE1.0 is for IR output with or without carrier and this bit is useful only MODE0.5 is "1". For STPC control IR output (MODE0.5 is 0), the IR output always has 38 KHz carrier signal no matter what the setting of MODE1.0 is.

3. PAGE Register

BIT	7	6	5	4	3	2	1	0
PAGE	-	-	-	PG4	PG3	PG2	PG1	PG0

Bits 5–7 of PAGE register are reserved; bits 0–4 are used for page selection. The user must set the page mode configuration described in the Option Control declaration. Once the page mode is decided, the working page is selected by the bits 0–4 of PAGE register. Hence, the user can execute "LD PAGE, value" instruction to change the working page of the interrupt vector/label. Not all of the bits 0–4 of PAGE register are used in different page mode; they are listed below.

PAGE MODE	PG4	PG3	PG2	PG1	PG0
1-page	×	×	×	×	×
8-page	×	×	√	√	√
16-page	×	√	√	√	√
32-page	√	√	√	√	√

Where "×" means don't care and "√" means must be set properly.

4. EN0, EN1 Registers

BIT	7	6	5	4	3	2	1	0
EN0	TG4R	TG3R	TG2R	TG1R	TG4F	TG3F	TG2F	TG1F
EN1	TG8R	TG7R	TG6R	TG5R	TG8F	TG7F	TG6F	TG5F

A "1" means "enabled", while a "0" means "disabled" for that edge of the particular TG pin. For example, the instruction "LD EN0, 0x0F" enables all the falling edge triggers of TG1–TG4, while disabling all the rising edge triggers of TG1–TG4. The user can modify the EN0 and EN1 registers during operation of the W58300 to achieve various kinds of trigger functions, like retriggerable or not, one shot or level hold play mode, etc.

That is to say, users can change the contents of EN0, EN1 register during synthesis at will to determine which trigger pin is to be enabled or disabled for its falling/rising edge.

5. STOP Register

BIT	7	6	5	4	3	2	1	0
STOP	STH	STG	STF	STE	STD	STC	STB	STA

The STOP register is used to control the status of the STPA–STPH pins. For example, STB = 1 means that pin is in high state and STB = 0 means low state.

6. R0–R7 Registers

These eight registers are general purpose registers. They can be used to hold interrupt vector/label. R0 is a special register which can be incremented by "INC" instruction.

Option Control Function

There are four types of option that can be determined by a declaration in the user's program file, but can not be controlled by register.

FUNCTION	OPTION CONTROL DECLARATION	DEFINITION
Page Mode Configuration	DEFPAGE 1	256 interrupt vector/label for 1 page, 1 page in total (1-page mode)
	DEFPAGE 8	256 interrupt vector/label for 1 page, 8 pages in total (8-page mode)
	DEFPAGE 16	128 interrupt vector/label for 1 page, 16 pages in total (16-page mode)
	DEFPAGE 32	64 interrupt vector/label for 1 page, 32 pages in total (32-page mode)
Operation Mode	NORMAL	Normal mode operation
	CPU	CPU mode operation
Oscillator Frequency	OSC_3MHz	3 MHz oscillator
	OSC_1.5MHz	1.5 MHz oscillator
Voice Output Type	VOUT_DAC	DAC (AUD) output
	VOUT_PWM	PWM output

"DEFPAGE" decides the page operation mode of W58300. The default setting of the page mode is 1-page mode. The 8-page, 16-page or 32-page mode must be declared in order to reach the interrupt vector/label from 256 to 2047 when the interrupt vector/label is beyond 0–255.

The W58300 can communicate with an external microprocessor through the simple serial CPU interface, which is the same as the W581xx series. The CPU interface consists of the TG1, TG2, and STPA/BUSY pins. "NORMAL" and "CPU" decide whether the operation mode of W58300 will be normal mode or CPU mode.

"OSC_3MHz" and "OSC_1.5MHz" select the frequency of the system clock. "VOUT_DAC" and "VOUT_PWM" select the voice output type. OSC_1.5MHz is recommended.

Interrupt Vector Allocation

The W58300 provides a total of 8 trigger inputs to communicate with the outside world. Each trigger pin can invoke 2 dedicate interrupt vectors depending on TG pin status. The table below show the relationship between TG pin status and interrupt vectors.

INTERRUPT VECTORS	TRIGGER STATUS	INTERRUPT VECTORS	TRIGGER STATUS
0	TG1F	8	TG5F
1	TG2F	9	TG6F
2	TG3F	10	TG7F
3	TG4F	11	TG8F

Continued

INTERRUPT VECTORS	TRIGGER SOURCE	INTERRUPT VECTORS	TRIGGER SOURCE
4	TG1R	12	TG5R
5	TG2R	13	TG6R
6	TG3R	14	TG7R
7	TG4R	15	TG8R
32	POI	-	-

Instruction Set

There are two types of instruction in W58300, unconditional and conditional instructions. The first type of instructions are executed immediately after they are issued. The second type of instructions are executed only when the conditions specified in the instruction are satisfied. All the instructions are listed in the following table.

The cycle time for each instruction is 2/Sampling Frequency(Fs). For Fs = 6.0 KHz, the cycle time is 333 μS.

UNCONDITIONAL		CONDITIONAL		
JP	G	JP	G	@STS
JP	Rn	JP	Rn	@STS
LD	ENi, Value	LD	ENi, Value	@STS
LD	MODEi, Value	LD	MODEi, Value	@STS
LD	STOP, Value	LD	STOP, Value	@STS
LD	PAGE, Value	LD	PAGE, Value	@STS
LD	Rn, Value	LD	Rn, Value	@STS
END		END		@STS
MV	Rn, Rm	MV	Rn, Rm	@STS
INC		INC		@STS
TX	Rn	TX	Rn	@STS

Legend:

G: Interrupt vector/label

Rn: R0–R7

Rm: R0–R7

ENi: EN0, EN1

MODEi: MODE0, MODE1

Value: 8-bit data

@STS can be the following: @TGn_HIGH for n = 1–8, @TGn_LOW for n = 1–8, @LAST.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	V_{DD}–V_{SS}	-	-0.3 – +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS} -0.3 – V_{DD} +0.3	V
Storage Temp.	T_{STG}	-	-55 – +150	°C
Operating Temp.	T_{OPR}	-	0 – +70	°C

Note: Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{SS} = 0V, V_{DD} = 4.5V unless otherwise specified.)

DC Characteristics

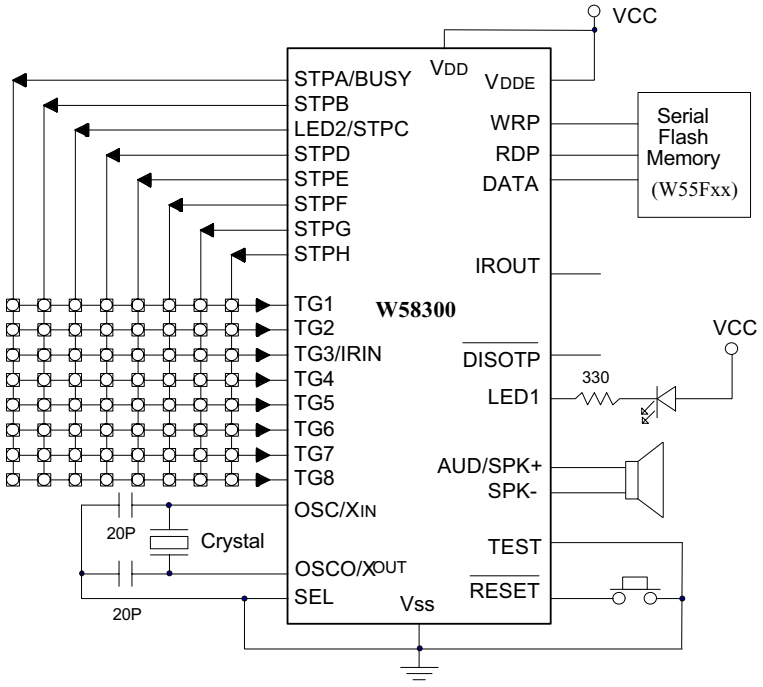
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}		2.4	3.0	5.5	V
Input Voltage	V_{IL}		V_{SS} -0.3	-	0.3 × V_{DD}	V
	V_{IH}		0.7 × V_{DD}	-	V_{DD}	
Standby Current	I_{SB1}	V_{DD} = 3V, All I/O Pins Unconnected, No Playing			1	µA
	I_{SB2}	V_{DD} = 5V, All I/O Pins Unconnected, No Playing			1	µA
Operating Current (Ring type)	I_{OP1}	V_{DD} = 3V, No Load			500	µA
	I_{OP2}	V_{DD} = 5V, No Load			1	mA
Operating Current (Crystal type)	I_{OP3}	V_{DD} = 3V, No Load			600	µA
	I_{OP4}	V_{DD} = 5V, No Load			1.2	mA
Input Current of TG1–TG8 Pins	I_{IN1}	V_{DD} = 3V, V_{IN} = 0V			-8	µA
Input Current of TEST Pin	I_{IN2}	V_{DD} = 3V, V_{IN} = 3V			50	µA
Input Current of SEL, $\overline{\text{RESET}}$ and $\overline{\text{DISOTP}}$	I_{IN3}	V_{DD} = 3V, V_{IN} = 0V			-8	µA
SPK (D/A Full Scale)	I_{DAC}	V_{DD} = 4.5V, Rl = 100 Ω	-4.0	-5.0	-6.0	mA
Output Current of STPA–STPH	I_{OL1}	V_{DD} = 3V, V_{OUT} = 0.4V	0.8			mA
	I_{OH1}	V_{DD} = 3V, V_{OUT} = 2.7V	-0.8			mA
Output Current of SPK+, SPK-	I_{OL2}	V_{DD} = 3V, Rl = 8 Ω	100			mA
	I_{OH2}		-100			mA
Output Current of WRP, RDP and DATA	I_{OL3}	V_{DD} = 3V, V_{OUT} = 0.4V	0.8			mA
	I_{OH3}	V_{DD} = 3V, V_{OUT} = 2.7V	-0.8			mA

AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency[1]	Fosc	Ring Oscillator, Rosc = 270 KΩ	2.7	3	3.3	MHz
		Ring Oscillator, Rosc = 560 KΩ	1.3	1.5	1.7	
Oscillation Frequency Deviation by Voltage Drop	$\frac{\Delta Fosc}{Fosc}$	$\frac{F(3V)-F(2.4V)}{F(3V)}$			7.5	%
Instruction Cycle Time	TINS	Fosc = 3 MHz, SR = 6 KHz		1/3		mS
POI Delay Time	TPD	Fosc = 3 MHz		160		mS
Long Debounce Time	TDEBL	Fosc = 3 MHz, SR = 6 KHz	50			mS
Short Debounce Time[2]	TDEBS		400			µS

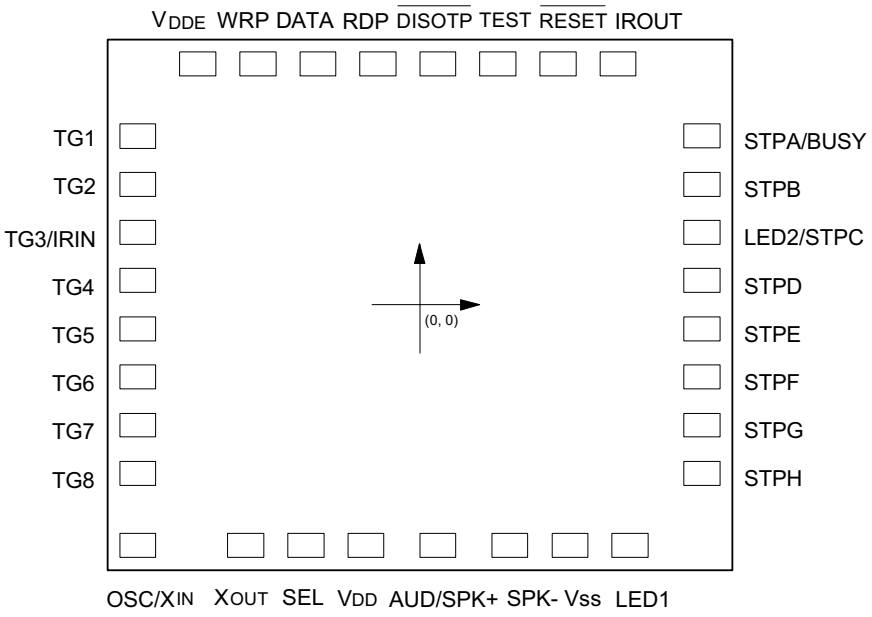
1. This parameter is different from that of W583xxx.
2. For ring oscillator only.

TYPICAL APPLICATION CIRCUIT



(PWM type voice output)

BONDING PAD DIAGRAM



REVISION HISTORY

Revision A1 to A2

1. FEATURE
   Change operating voltage range to 2.4-5.5 Volts
2. PIN DESCRIPTION
   Add description on TG3/IRIN
3. MODE0 Register
   Reserve bit MODE0.0
   Revise definition of MODE0.4
   Add description on bit MODE0.5
4. MODE1 Register
   Add description on bit MODE1.0
5. Instruction Set
   Add instruction cycle time
6. DC CHARACTERISTIC
   Revise Operating Voltage parameter

Revise Output Current of SPK+, SPK- parameter

7. AC CHARACTERISTIC

Revise Oscillation Frequency parameter

Revise Oscillation Frequency Deviation by Voltage Drop parameter

Revise Long Debounce Time parameter

Revise Short Debounce Time parameter

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