60" Voice/Melody/LCD Controller (ViewTalk™ Series)

GENERAL DESCRIPTION

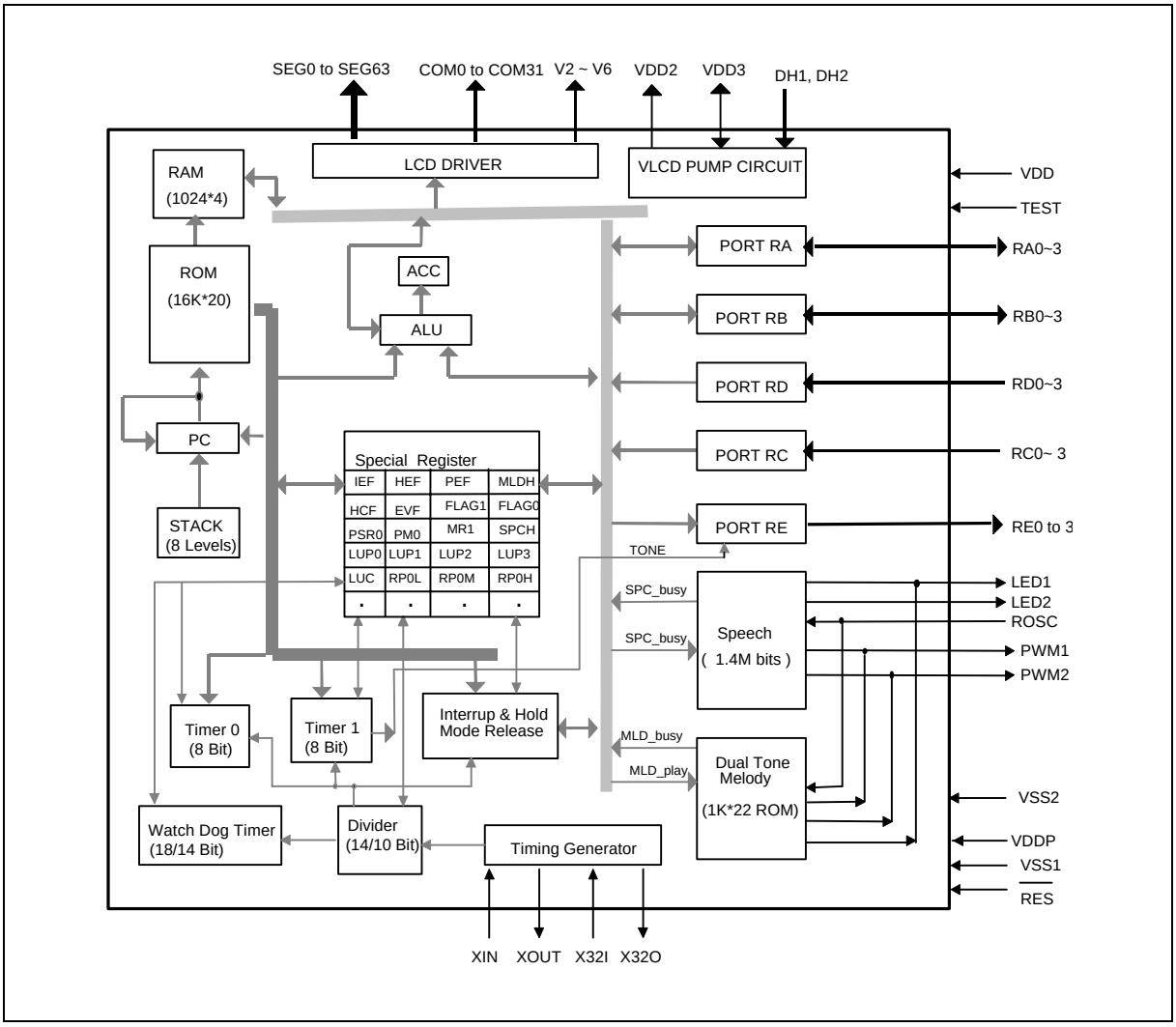
The W53322/W53342 are high-performance 4-bit microcontrollers (µC) with built-in speech, melody and 32*48/32*64 LCD driver which includes internal pump circuit. The 4-bit uc core contains dual clock source, 4-bit ALU, two 8-bit timers, one divider, 20 pin input or output, 7 interrupt sources , 8-level subroutine nesting for interrupt applications. Speech unit can be implemented with Winbond 60 sec Power Speech using ADPCM algorithm. Melody unit provides dual tone output and can store up to 1k notes. Power reduction mode is also built in to minimize power dissipation. It is ideal for games, educational toys, remote controllers, watches, clocks and other application' products which incorporate both LCD display and melody.

FEATURES

- Operating voltage: 2.4 volt ~ 5.5 volt
- Dual clock operating system
  - –RC/Crystal (400 KHz to 4 MHz) for main clock
  - – 32.768 KHz crystal oscillation circuit for sub-oscillator
- Memory
  - – 16k × 20 bit program ROM
  - – 512 × 4 bit data RAM
  - – 384 x 4/512 × 4 bit LCD RAM for W53322/W53342
- 20 input/output pins
  - –Ports for input only: 2 ports/8 pins
  - –Input/output ports: 2 ports/8 pins
  - –Port for output only: 1 port /4 pins
- Power-down mode
  - –Hold function: no operation (except for 32kHzoscillator)
  - – Stop mode function: no operation (include 32kHz oscillator)
- Seven types of interrupts
  - –Five internal interrupts (Divider ,Timer 0, Timer 1, Speech, Melody)
  - –Two external interrupts (Port RC, Port RD)
- One built-in 14-bit clock frequency divider circuit
- Two built-in 8-bit programmable countdown timers
  - –Timer 0: one of two internal clock frequencies (FOSC/4 or FOSC/1024) can be selected
  - –Timer 1: built-in auto-reload function includes internal timer, external event counter from RC.0 or TONE output function (can be used as IR carrier output if main clock is 455 kHz)
- Built-in 18/14-bit watchdog timer for system reset by mask code option
- Powerful instruction sets
- 8-level subroutine (including interrupt) nesting

- LCD driver output
  - –32 common × 48 segment/32 common × 64 segment for W53322/W53342 respectively
  - – 1/16 or 1/32 duty, 1/5 or 1/7 bias, internal pump circuit option by special register
- Speech function
  - –Provides 1.4M bits dedicated speech ROM
  - –Direct driving output for speaker
  - –Maximum 256 sections available
- Melody function
  - –Provides 22 kbits dedicated melody ROM
  - –Provides 6 kinds of beat, 16 kinds of tempo, and pitch range from G3# to C7
  - –Tremolo, triple frequency and 3 kinds of percussion available
  - –Direct driving output for speaker
  - –Maximum 32 scores available
- Mix speech with melody available
- Multi-engine controller
- PWM output current option
- Chip On Board available

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN	I	Input pin for oscillator. It can be connected to crystal, or can connect a resistor to VDD to generate main system clock. Oscillator can be stopped when SCR.1 is set to logic 1.
XOUT	O	Output pin for oscillator which is connected to another crystal pin.
X32I	I	32.768 KHz crystal input pin.
X32O	O	32.768 KHz crystal output pin.
RA0 ~ RA3	I/O	General Input/Output port specified by PM1 register. If output mode is selected, PM0 register can be used to specify CMOS/NMOS driving capability option. Initial state is input mode.
RB0 ~ RB3	I/O	General Input/Output port specified by PM2 register. If output mode is selected, PM0 register can be used to specify CMOS/NMOS driving capability option. Initial state is input mode.
RC0 ~ RC3	I	4-bit schmitt input with internal pull high option specified by PM0 register. RC0 can be used as clock source for Timer 1. Each pin has an independent interrupt capability specified by PEFL special register.
RD0 ~ RD3	I	4-bit schmitt input port with internal pull high option specified by PM0 register. Each pin has an independent interrupt capability specified by PEFH special register.
RE0~RE3/TONE	O	Output port only. RE3 may use as TONE if bit 0 of MR0 special register is set to logic 1.
$\overline{\text{RES}}$	I	System reset pin with internal pull-high resistor is active low.
TEST	I	Test pin. Connected to low for normal use.
ROSC	I	Connects resistor to VDD to generate speech or melody clock source.
VDDP	I	Power source for PWM output.
LED1	O	Synchronous LED1 output while speech play/melody is active.
LED2	O	Synchronous LED2 output only while speech play is active.
PWM1	O	Speaker direct driving output 1 while speech or melody is active.
PWM2	O	Speaker direct driving output 2 while speech or melody is active.
SEG0–SEG63	O	LCD segment output pins.
COM0–COM31	O	LCD common signal output pins. The LCD alternating frequency is fixed at 64Hz.
DH1, DH2	I	Connection terminals for voltage doubler capacitor.
VDD2	O	Connects a 1uF capacitor to VSS1 to double VDD voltage output if triple pump option is enabled. Otherwise, VDD2 connects to VDD directly if double pump option is enabled.
VDD3	O/I	An output if internal pump circuit is enabled. It connects a 1uF capacitor to VSS. Triple VDD voltage will be output if triple pump option is enabled. Otherwise, double VDD voltage will be output if double pump option is enabled. An input if internal pump voltage is disabled.

V2 ~ V5	O	LCD COM/SEG output driving voltage. If internal shunt resistor is disabled, external resistors need to be supplied to V2, V3, V4, V5 . A capacitor is suggested for stable LCD voltage level.
V6	I	External variable resistor connects between VDD3 and V6 to adjust LCD maximun voltage level.
VDD	I	Microcontroller Positive power supply (+).
VSS1	I	Negative power supply (-).
VSS2	I	Negative power supply (-).

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C
VDD3 Input Voltage	12	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(VDD–VSS = 3.0V, Fm =1 MHz, Fs = 32.768 KHz, TA = 25° C, LCD on; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}		2.4		5.5	V
Op. Current (No Load)	I_{OP1}	Dual clock with crystal	-	250	300	uA
		Dual clock with RC type		250	300	uA
		Single Clock		60	100	uA
Halt Mode Current (No Load, LCD OFF)	Iop2	Dual clock with crystal		120	150	uA
		Dual clock with RC type		120	150	
		Single clock		6	10	
Stop Mode Current	Iop3	LCD OFF			1	uA
Input Low Voltage	V_{IL}	-	VSS	-	0.3*VDD	V
Input High Voltage	V_{IH}	-	0.7	-	1	VDD
Port RA, RB Output Low Voltage	V_{ABL}	IOL = 2.0 mA	-	-	0.4	V
Port RA, RB Output High Voltage	V_{ABH}	IOH = -2.0 mA	2.4	-	-	V
Port RE Sink Current	I_{EL}	VOL = 0.4V	2	-	-	mA
Port RE Source Current	I_{EH}	VOH = 2.4V	-2	-	-	mA

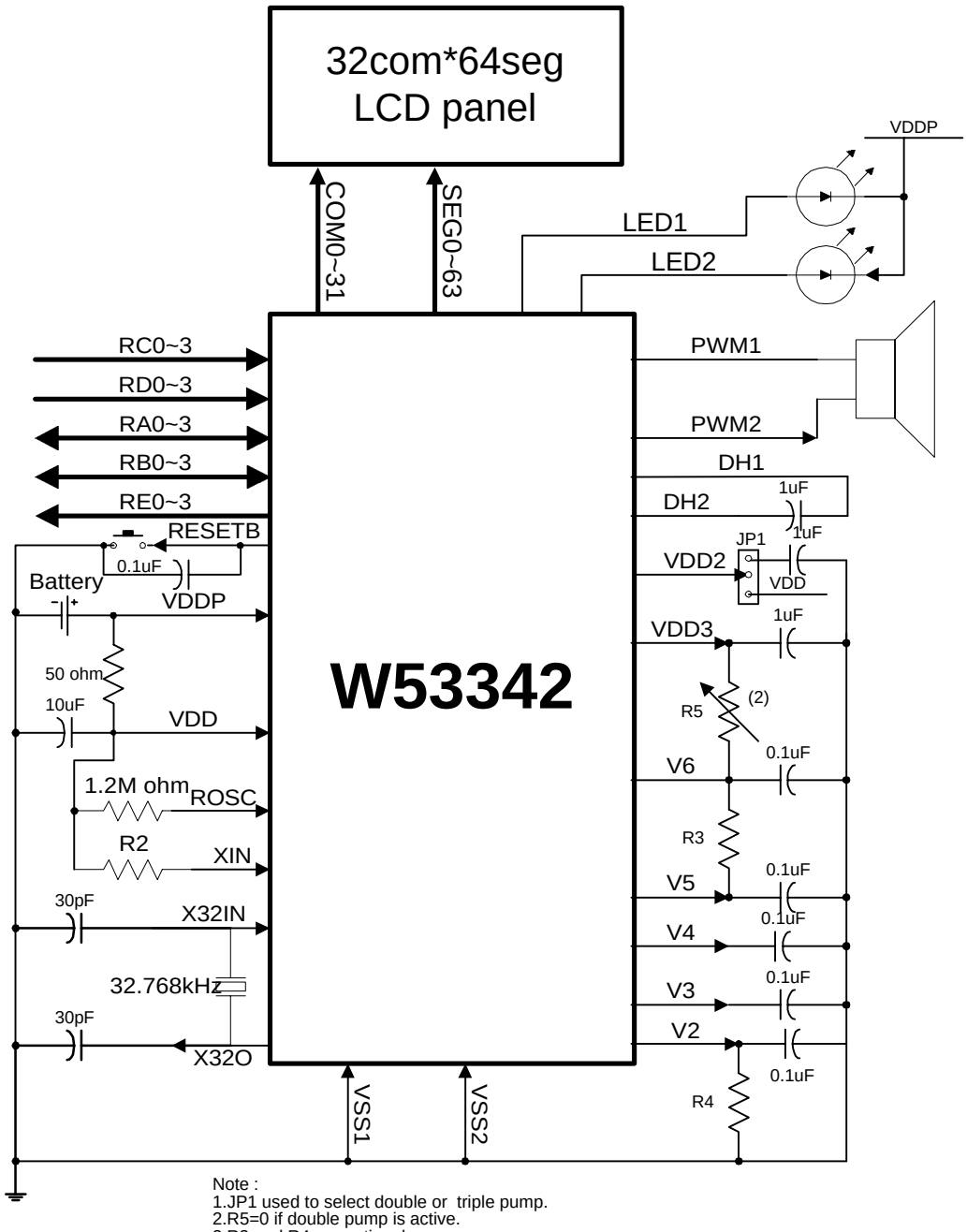
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pull-up Resistor	RCD	Port RC, RD	100	350	1000	KΩ
RES Pull-up Resistor	RRES	-	20	100	500	KΩ
LED1/LED2 Sink Current	ILED	VO=1 volt		8		mA
PWM1/2 Source Current	ISPH	VOL = 2.4V CUR1~0=00	-30			mA
		VOL = 2.4V CUR1~0=01	-60			
		VOL = 2.4V CUR1~0=10	-90			
		VOL = 2.4V CUR1~0=11	-120			
PWM1/2 Sink Current	ISPL	VOL = 0.6V CUR1~0=00	30			mA
		VOL = 0.6V CUR1~0=01	60			
		VOL = 0.6V CUR1~0=10	90			
		VOL = 0.6V CUR1~0=11	120			
LCD Supply Current	ILCD	No Load, All Seg. ON	-	50	-	μA
COM/SEG On Resistor	Ron	IOH = ± 50 μA		5K	10K	Ω
VDD2 output voltage	VDOB	VLCDEXT=0 & PMPV3B=0		2		VDD
		VLCDEXT=0 & PMPV3B=1		1		
VDD3 output Voltage	VTRI	VLCDEXT=0 & PMPV3B=0		3		VDD
		VLCDEXT=0 & PMPV3B=1		2		
VDD3 Input Voltage	VLCD	VLCDEXT=1		7	10	V

AC CHARATERISTICS

(VDD–VSS = 3.0V, Fm = 1 MHz, Fs = 32.768 KHz, TA = 25° C, LCD on; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	FS	Crystal type		32768		Hz
Main-clock Frequency	FM	RC type/Crystal type	400	-	4190	KHz
Op. Frequency	FOSC	SCR.0=1		32768		KHz
		SCR.0=0	400	-	4190	
Instruction Cycle Time	TCYC	One machine cycle	-	4/FOSC	-	S
Reset Active Width	TRAW	FOSC = 32.768 KHz	1	-	-	μS
Interrupt Active Width	TIAW	FOSC = 32.768 KHz	1	-	-	μS
Main clock RC frequency	FRXIN	RXIN =2.4 MΩ		400K		Hz
		RXIN =1.2 MΩ		800K		
		RXIN =910 KΩ		1M		
		RXIN =160 KΩ		4M		
Frequency Deviation of main-clock FRXIN =1MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$	-	-	10	%
ROSC Frequency	FROSC	ROSC =1.2MΩ		3.23		MHz
Frequency Deviation of FROSC = 3MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$	-	-	10	%
Frame frequency	FLCD			64		Hz

TYPICAL APPLICATION CIRCUIT



Note :
1.JP1 used to select double or triple pump.
2.R5=0 if double pump is active.
3.R3 and R4 are optional.
4.LCD duty and bias are programmed by registers .

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792697
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-7197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668