Winbond Electronics Corp.

ADPCM VOICE SYNTHESIZER
(ROM-less PowerSpeech)

GENERAL DESCRIPTION

The W5280 is a CMOS IC that is used solely for the purpose of demonstrating W528X series PowerSpeech products.

The W5280 employs the same JUMP-GO architecture as most of Winbond's other speech synthesizers. Unlike standard products, however, the W5280 does not include a built-in memory, because the chip is designed to serve only as a demonstration chip for the W528X series PowerSpeech ICs. The W5280 has an ADPCM synthesizer, an 8-bit D/A converter, and all other necessary control and timing logic, but it must be operated with an external memory device (OTP). The W5280's LOAD and JUMP commands and four programmable registers provide powerful user-programmable functions that make this chip suitable for an extremely wide range of speech IC applications.

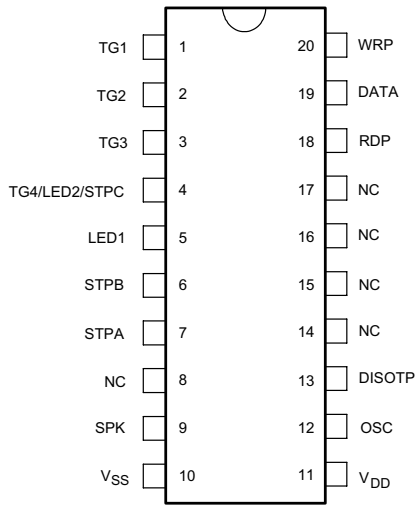
FEATURES

- Serves as demo chip for W528X series products (no built-in ROM)
- Oscillator frequency adjustable by external resistor
- Wide operating voltage range: 2.4 to 5.0 volts
- 4-bit ADPCM synthesizer method and built-in 8-bit D/A converter
- Provides 4 direct trigger inputs that can easily be extended to 8 or 12 matrix trigger inputs
- Two trigger input debounce time settings (20 to 40 mS or 160 to 320 μS) through register control
- Provides up to 2 LEDs and 3 STOP outputs
- Every LED pin drives up to 3 LEDs simultaneously
- LED flash frequency: 3 Hz
- AUD output current: 5 mA
- Flexible functions programmable through the following:
  - LD (load), JP (jump) commands
  - Four registers: R0, EN, STOP, and MODE
  - Conditional instructions
  - Speech equation
  - END instruction
  - Global repeat (GR) setting
  - Output frequency and LED flash type setting
- Programmable power-on initialization (POI) (can be interrupted by trigger inputs)
- POI delay time of 160 mS to maintain stable voltage when chip is powered on

Publication Release Date: March 1996
Revision A2

- Can be programmed for the following functions:
  - Interrupt or non-interrupt for rising or falling edge of each trigger pin (this feature determines retriggerable, non-retriggerable, overwrite, and non-overwrite features of each trigger pin)
  - Four playing modes:
    One Shot (OS)
    Level Hold (LH)
    Single-cycle level hold (S_LH)
    Complete-cycle level hold (C_LH)
  - Stop output signal setting
  - Serial, direct, or random trigger mode setting
- Four frequency options (4/4.8/6/8 KHz) and LED On/Off control can be set independently in each GO instruction of speech equation
- Independent control of LED 1 and LED 2
- Total of 256 voice group entries available for programming
- Provides the following mask options:
  - LED flash type: synchronous/alternate
  - LED 1 section-controlled: Yes/No
  - LED 2 section-controlled/STPC-controlled
  - LED volume-controlled: No/Yes

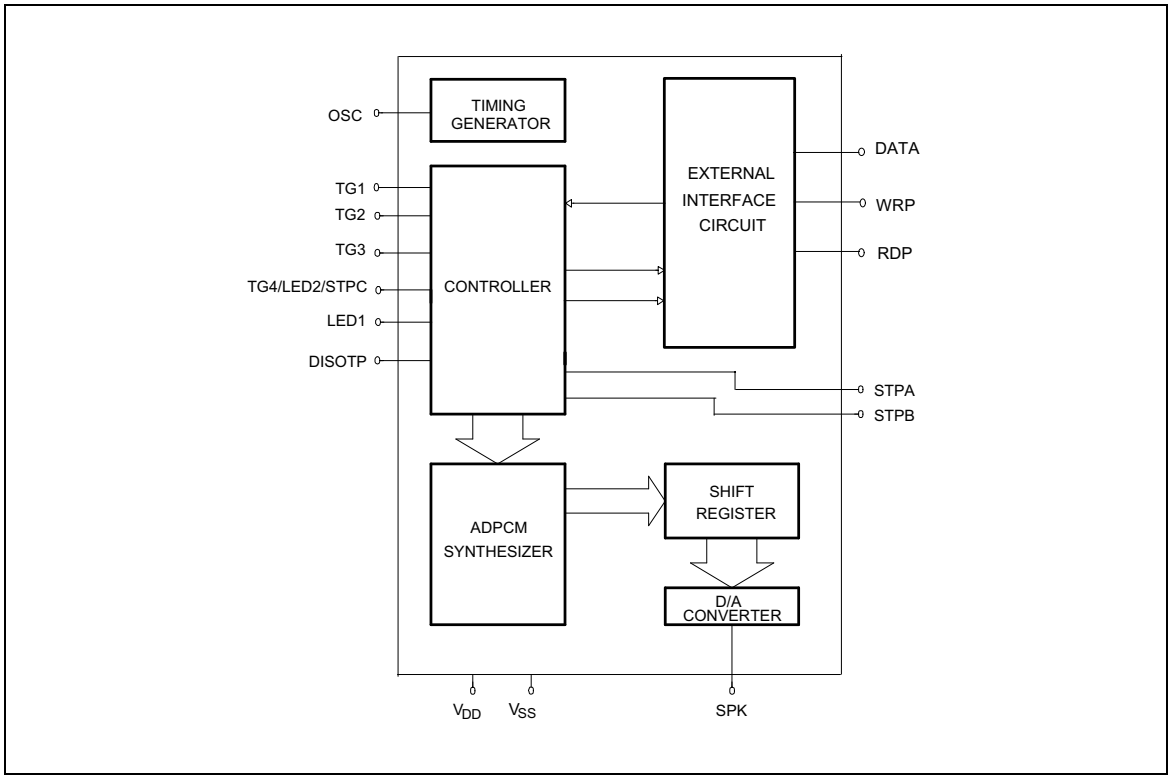
PIN CONFIGURATION



PIN DESCRIPTION

NO.	NAME	I/O	FUNCTION
1	TG1	I	Trigger Input 1
2	TG2	I	Trigger Input 2
3	TG3	I	Trigger Input 3
4	TG4/LED2/STPC	I/O	Trigger Input 4 or LED 2 or Stop Signal C
5	LED1	O	LED 1
6	STPB	O	Stop Signal B
7	STPA	O	Stop Signal A
8	NC	-	Not Connected
9	SPK	O	Current Output for Speaker
10	V_{SS}	-	Negative Power Supply
11	V_{DD}	-	Positive Power Supply
12	OSC	I	Oscillation Frequency Control
13	DISOTP	I	Connects to ground to disable OTP and speech interface; data can then be burned into OTP directly
14	NC	-	Not connected
15	NC	-	Not connected
16	NC	-	Not connected
17	NC	-	Not connected
18	RDP	O	Read pulse clock output for serial interface
19	DATA	I/O	Bidirectional data pin for serial interface
20	WRP	O	Write pulse clock output for serial interface

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W5280 provides up to four direct trigger pins (which can be extended to eight or twelve matrix trigger inputs), up to three stop signal output pins, an LED section control, and powerful programmable features. The JUMP and LOAD commands and four programmable registers can be used to program the desired playing mode, stop output signal form, LED flash type, and trigger pin interrupt modes.

The chip's programmable features can also be used to develop new, customized functions for a wide variety of innovative applications.

A. Instruction Set Description

This section describes three types of instructions:

- Unconditional instructions, which are executed immediately after they are issued.
- Conditional instructions, which are executed only when the conditions specified in the instructions are satisfied.
- END instruction, which is used to stop all device activity.

Instructions are programmed by writing LOAD and JUMP commands into the R0, EN, STOP, and MODE registers.

Unconditional Instructions:

1. LOAD (LD) Command:

LD R0, value: This instruction is used to load a voice-group entry value into register R0. The voice-group entry value may range from 0 to 255. The initial value of the R0 register is "00000000."

LD EN, operand: This instruction is used to define the trigger interrupt settings by loading the operand message into register EN. The initial value of the EN register is "11111111."

a. The operand is an 8-bit value that can be entered in decimal (default) or hexadecimal (with "0x" as a prefix).

b. EN is an 8-bit register that is used to enable/disable the rising/falling edge of each of the four trigger inputs.

The 8 bits correspond to the rising/falling edges of the triggers as shown below:

Bit:	7	6	5	4	3	2	1	0
TG:	4R	3R	2R	1R	4F	3F	2F	1F

where "nR/F" represents the rising/falling edge of the n-th trigger pin.

c. When any one of the eight bits is set to "1" (default), the corresponding trigger will interrupt the current state at the edge indicated. When the bits are set to "0," the triggers will be disabled.

d. The voice group entry addresses correspond to the interrupt vectors as follows:

TG:	4R	3R	2R	1R	4F	3F	2F	1F
Group:	7	6	5	4	3	2	1	0

EXAMPLE:

The instruction "LD EN, 0x41" is programmed.

EXPLANATION:

a. "41" is a hexadecimal value equal to the binary value "0100 0001."

b. These 8 bits of data represent the following trigger interrupt settings:

TG:	4R	3R	2R	1R	4F	3F	2F	1F
Bit	0	1	0	0	0	0	0	1

RESULT:

a. When the rising edge of TG3 (3R) is activated, the EN register will cause TG3 to interrupt the current playing state and jump immediately to voice group 6, the voice group that corresponds to 3R.

b. When the falling edge of TG1 (1F) goes active, the EN register will cause TG1 to interrupt the current playing state and jump immediately to voice group 0, the voice group that corresponds to 1F.

c. No action will be taken when the other trigger pins are pressed, because the corresponding bits are set to "0."

LD STOP, operand: This instruction loads the operand message into the STOP register to set the output levels of the stop signals. The initial value of the STOP register is "XXXXX111."

a. This register is used to program the output levels of the three STOP signals, STPA, STPB, and STPC. Only three of the bits in the register are used, as shown below (an "X" indicates "Don't care"):

Bit:	7	6	5	4	3	2	1	0
STOP:	X	X	X	X	X	STPC	STPB	STPA

b. When a particular STOP bit is set to "1," The corresponding stop signal will be a high output; when a bit is set to "0," the corresponding stop signal will be a low output.

EXAMPLE:

The instruction "LD STOP, 0x43" is programmed.

EXPLANATION:

a. "43" is a hexadecimal value equal to a binary value of "0100 0011."

b. These 8 bits of data represent the following settings:

Bit:	0	1	0	0	0	0	1	1
STOP:	X	X	X	X	X	STPC	STPB	STPA

RESULT:

a. The STPA and STPB outputs will be high outputs.

b. The STPC signal will be a low output.

c. The sixth bit "1" is a "Don't Care" bit and so has no effect on the stop signal output settings.

LD MODE, operand: This instruction is used to select among various operating modes. It loads an operand message into the MODE register to select one mode from each of four pairs of modes, which correspond to bits 4 through 7 of the register (bits 0 to 3 are "Don't Care" bits). The four pairs of modes and the corresponding bits are as follows:

Bit:	7	6	5	4	3	2	1	0
MODE:	Flash/DC	LED2/STPC	TG4/LED2_STPC	20 mS/160 µS	X	X	X	X

A "1" for one of these bits selects the first of the pair of modes indicated; a "0" selects the second of the pair. The initial value of the mode register is "1111XXXX."

EXAMPLE 1:

The four bits are programmed as "1111," so that the eight bits of the register are as follows (an "X" indicates a "Don't Care" bit):

Bit:	1	1	1	1	X	X	X	X
MODE:	Flash/DC	LED2/STPC	TG4/LED2_STPC	20 mS/160 μS	X	X	X	X

RESULT:

The mode settings are as follows:

a. Pin 4 (TG4/LED2_STPC) is configured as a trigger pin (TG4), and the LED2/STPC option will be ignored.

b. The LED is set as a flash type, with a flash frequency of 3 Hz.

c. The debounce time of the trigger inputs is set to 20 mS.

EXAMPLE 2:

The four bits are programmed as "0000," so that the eight bits of the register are as follows (an "X" indicates a "Don't Care" bit):

Bit:	0	0	0	0	X	X	X	X
MODE:	Flash/DC	LED2/STPC	TG4/LED2_STPC	20 mS/160 μS	X	X	X	X

RESULT:

The mode settings are as follows:

a. Pin 4 (TG4/LED2_STPC) is configured as either the LED2 or STPC output (determined by bit 6, LED2/STPC; see next item).

b. Pin 4 is configured as the STPC output pin.

c. LED will be lit constantly during operation.

d. The debounce time of the trigger inputs is set as 160 μS.

2. JUMP (JP) Command:

JP value: Instructs device to jump directly to the voice group corresponding to the value indicated. The voice group value may range from 0 to 127 (direct jump).

JP R0: Instructs device to jump to whatever voice group is indicated by the value currently stored in register R0, from 0 to 255 (indirect jump).

Conditional Instructions:

Conditional instructions are executed only when the conditions specified in the instructions hold. The conditional instructions are listed below. An explanation of the notation used in the instructions follows.

(Note: There are no conditional instructions for LD MODE.)

LD R0, VALUE @LAST: VALUE can be set from 0 to 255.

LD R0, VALUE @TGn_STATUS: VALUE can be set from 0 to 255.

LD EN, OPERAND @LAST: EN–4R, 3R, 2R, 1R, 4F, 3F, 2F, 1F.

LD STOP, OPERAND @LAST: STOP–X, X, X, X, X, STC, STB, STA.

JP VALUE @LAST: VALUE can be set from 0 to 127

JP R0 @LAST

JP VALUE @TGn_STATUS: VALUE can be set from 0 to 127

JP R0 @TGn_STATUS

EXPLANATION:

@LAST: At last time of global repeat.

@TGn_STATUS: When the status of the trigger specified (TGn) is in the condition specified, where the possible triggers and conditions are the following:

TG1_HIGH
TG1_LOW
TG2_HIGH
TG2_LOW
TG3_HIGH
TG3_LOW
TG4_HIGH
TG4_LOW

End Instruction:

END: This command instructs the chip to cease all activity immediately.

B. Program Structure Features and Execution Rules

1. There are eight hardware group entry points and 248 software group entry points, as follows:

		Group
8 H/W entries:	TG1F:	0
	TG2F:	1
	TG3F:	2
	TG4F:	3
	TG1R:	4
	TG2R:	5
	TG3R:	6

Continued

	TG4R:	7
248 S/W entries:		8
		9
		. . .
	POI:	32
		33
		. . .
		254
		255

2. Execution begins from group entry and is terminated by END instruction.
3. A H/W trigger interrupt stops the group currently being executed immediately and begins a new group.

C. Mask Options

There are several mask options for the W5280; the mask options are used to select features that can be demonstrated when the chip is used with an OTP. (The LED flash frequency (3 Hz fixed) and the AUD output current (5 mA fixed) cannot be adjusted.)

The mask options that can be demonstrated are the following:

LED flash type (synchronous/alternate)

LED volume-controlled: No/Yes

LED1 section-controlled: Yes/No

LED2: section-controlled/STPC-controlled

D. Speech Equation Description

The format of the speech equations for the W5280 is as follows:

GR = N

H4+m1*SOUND1_FL+m2*SOUND2_FL+[1FFFF]+... +T4

END

where

GR = N defines the number of global repeats (from 1 to 16);

m1 and m2 define the number of local repeats (from 1 to 7);

SOUND1 and SOUND2 are the *.WAM files of ADPCM converted voice data;

_FL is the section control setting, for which the parameters F and L are as follows:

F: Voice output frequency setting:

F	0	1	2	3
Frequency (KHz)	4	4.8	6	8

L: LED output setting:

L	0	1
LED state	Off	On

[1FFFF] is a period of silence of length 1FFFF;

H4, T4: Represent head and tail ADPCM files, respectively.

E. Programmable Power-on Initialization

Whenever the W5280 is powered on, the program contained in the 32th voice group will be executed after the power-on delay (about 160 mS), so the user can write a program into this group to set the power-on initial state. If the user does not wish to execute a program at power-on, an "END" instruction should be entered in group 32. The W5280 power-on initialization process can be interrupted by trigger inputs.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	V_{DD}–V_{SS}	-	-0.3 to +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS} -0.3 to V_{DD} +0.3	V
Storage Temp.	T_{STG}	-	-55 to +150	°C
Operating Temp.	T_{OPR}	-	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(T_A = 25° C, V_{SS} = 0 V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V_{DD}	-	2.4	3	5.0	V
Input Voltage	V_{IL}	All Input Pins	V_{SS} -0.3	-	0.3 V_{DD}	V
	V_{IH}		0.7 V_{DD}	-	V_{DD}	

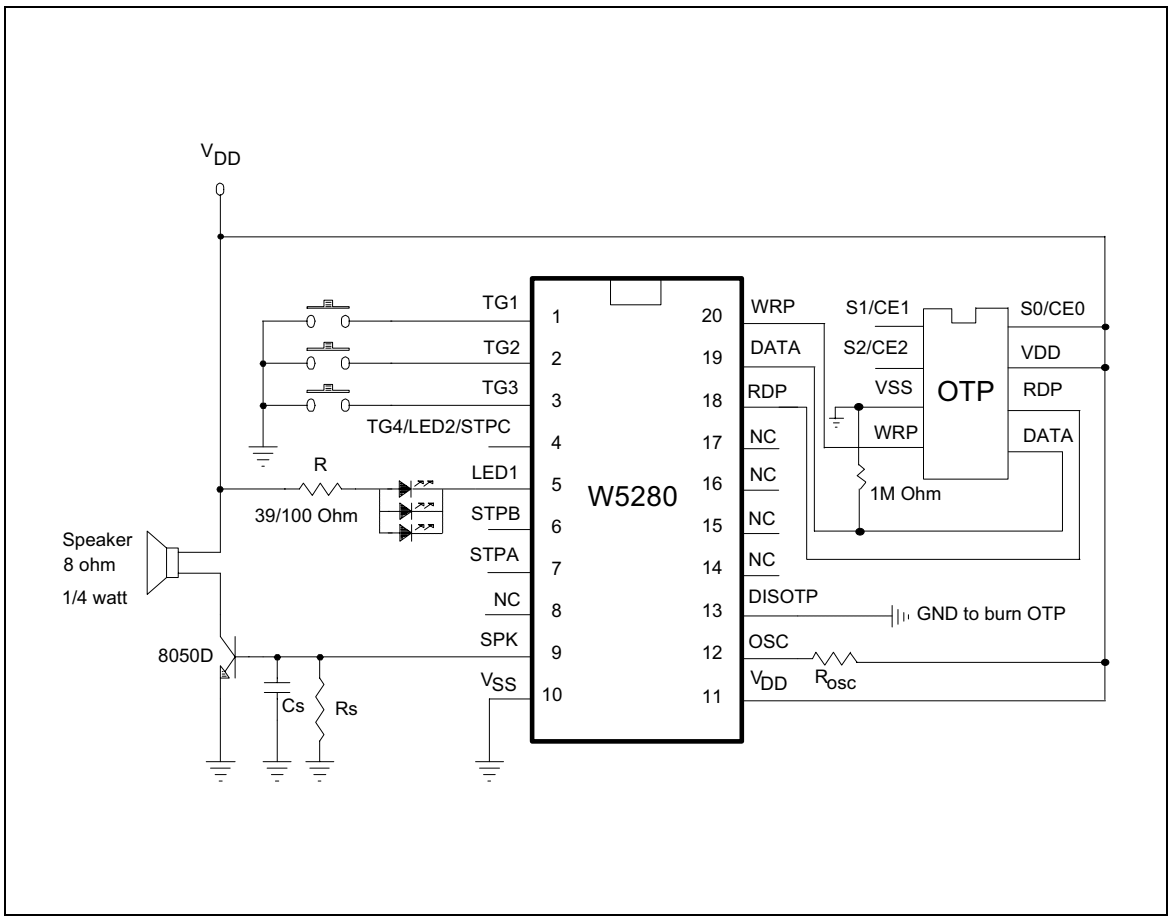
DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	

Standby Current		I_{DD1}	V_{DD} = 3 V, No Playing	-	-	0.2	μA
		I_{DD2}	V_{DD} = 5 V, No Playing	-	-	0.4	
Operating Current		I_{OP1}	V_{DD} = 3 V, No Load	-	-	400	μA
		I_{OP2}	V_{DD} = 5 V, No Load	-	-	800	
Input Current for TG1–TG4		I_{IN}	V_{DD} = 3 V, V_{IN} = 0 V	-	-	6	μA
SPK (D/A Full Scale)		I_{O1}	V_{DD} = 4.5 V, R_L = 100 Ω	-4.0	-5.0	-6.0	mA
Output Current of STPC		I_{OL}	V_{DD} = 3 V, V_{OUT} = 0.4 V	1	-	-	mA
		I_{OH}	V_{DD} = 3 V, V_{OUT} = 2.7 V	-0.5	-	-	
Output Current	LED1	I_O	V_{DD} = 3 V, V_{OUT} = 1 V	10	-	-	mA
	LED2		V_{DD} = 4.5 V, V_{OUT} = 1 V	15	-	-	
	STPA	I_{OL}	V_{DD} = 3 V, V_{OUT} = 0.4 V	1	3	-	
	STPB	I_{OH}	V_{DD} = 3 V, V_{OUT} = 2.7 V	-1	-3	-	
Oscillation Freq.		F_{OSC}	V_{DD} = 3 V, R_{OSC} = Typ.	2.7	3	3.3	MHz
			V_{DD} = 4.5 V, R_{OSC} = Typ.	2.7	3	3.3	
Oscillation Freq. Deviation by Voltage Drop		$\frac{\Delta F_{OSC}}{F_{OSC}}$	$\frac{F(3\ V) - F(2.4\ V)}{F(3\ V)}$	0	4	7.5	%
Input Debounce Time		T_{DEB1}	F_{OSC} = 3 MHz	20	30	40	mS
		T_{DEB2}		160	240	320	μS

Note: R_{OSC} = Typ. = 1.2 MΩ.

TYPICAL APPLICATION CIRCUIT



Notes:

1. In principle, the playing speed determined by R_{OSC} should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varying R_{OSC}, however.
2. Rs is an optional current-dividing resistor. If Rs is added, the resistance should be between 470 and 750 Ω.
3. R is used to limit the current on the LED. Case 1: V_{DD} = 3 V, R = 39 Ω for 1/2/3 LEDs. Case 2: V_{DD} = 4.5 V, R = 39 Ω for 2/3 LEDs and R = 100 Ω for 1 LED.
4. Cs is optional.
5. The DC current gain β of transistor 8050 ranges from 120 to 200.
6. All unused trigger pins can be left open because of their internal pull-high resistance.
7. No warranty for production.

Winbond Electronics Corp.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792697
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-7197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27516023
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668