



PowerSpeech LOW VOLTAGE ADPCM VOICE SYNTHESIZER

GENERAL DESCRIPTION

The W5230 is a CMOS IC that is used solely for the purpose of demonstrating W523X series Low Voltage PowerSpeech products.

The W5230 employs the same JUMP-GO architecture as Winbond's other PowerSpeech products. Unlike standard products, however, the W5230 does not include built-in memory, because the chip is designed to serve only as a demonstration chip for the W523X series ICs. Hence the W5230 must be operated with an external memory device (e.g., an OTP memory). The W5230's LOAD and JUMP commands and four programmable registers provide powerful user-programmable functions that make this chip suitable for a wide range of speech IC applications.

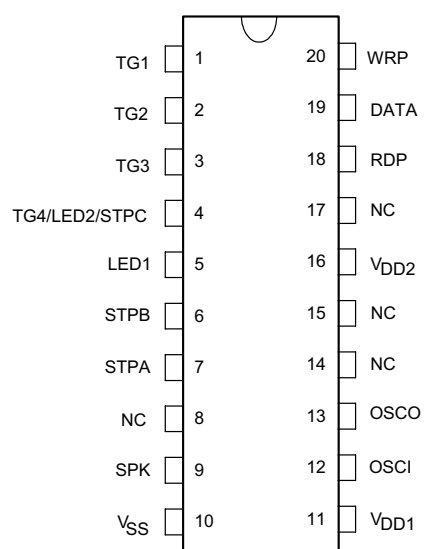
FEATURES

- Wide operating voltage range: 1.2 to 3.6 volts
- Serves as demo chip for W523X series products (no built-in ROM)
- Programmable speech synthesizer
- 4-bit ADPCM synthesis method and 8-bit D/A converter
- RC oscillator with built-in capacitor; voice output frequency typically at 6 KHz
- Provides 4 trigger inputs
- Drives 2 flash LEDs for two batteries
- 3 STOP output signals
- Flexible functions programmable through the following:
 - LD (load), JP (jump) commands
 - Four registers: R0, EN, STOP, and MODE
 - Conditional instructions
 - Speech equation
 - Global repeat (GR) setting
- Programmable power-on initialization (POI), which can be interrupted by trigger inputs
- Interrupt or non-interrupt for rising or falling edge of each trigger pin (this feature determines retriggerable, non-retriggerable, overwrite, and non-overwrite features of each trigger pin)
- LED On/Off control can be set independently in each GO instruction of speech equation
- Independent control of LED 1 and LED 2
- Total of 256 voice group entries available for programming
(Including eight hardware and 248 software group entry points)
- 20 to 40 mS debounce time
- Provides the following mask options:



- LED flash frequency: 3 Hz/6 Hz/Off
- LED1 section-controlled: Yes/No
- LED2 section-controlled/STPC-controlled
- AUD output current: 1 mA with one battery, 3 mA with two batteries

PIN CONFIGURATION





PIN DESCRIPTION

NO.	NAME	I/O	FUNCTION
1	TG1	I	Trigger Input 1
2	TG2	I	Trigger Input 2
3	TG3	I	Trigger Input 3
4	TG4/LED2/STPC	I/O	Trigger Input 4 or LED 2 or Stop Signal C
5	LED1	O	LED 1
6	STPB	O	Stop Signal B
7	STPA	O	Stop Signal A
8	NC	-	Not Connected
9	SPK	O	Current Output for Speaker
10	Vss	-	Negative Power Supply
11	VDD1	-	1.5 V or 3 V Positive Power Supply
12	OSCI	I	Oscillator Input Connect Resistor
13	OSCO	O	Oscillator Output Connect Resistor
14	NC	-	Not Connected
15	NC	-	Not Connected
16	VDD2	-	5 V Positive Power Supply
17	NC	-	Not Connected
18	RDP	O	Read Pulse Clock Output for Serial Interface
19	DATA	I/O	Bidirectional Data Pin for Serial Interface for OTP
20	WRP	O	Write Pulse Clock Output for Serial Interface

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Power Supply	VDD-VSS		-0.3 to +5.0	V
Input Voltage	VIN	All Inputs	Vss -0.3 to VDD +0.3	V
Storage Temp.	TSTG		-55 to +150	°C
Operating Temp.	TOPR		0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.



ELECTRICAL CHARACTERISTICS

(TA = 25° C, VSS = 0 V)

PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN.	TYP.	MAX.	
Operating Voltage		VDD	One or Two Batteries	1.2	2.4	3.6	V
Input Voltage		VIL	All Input Pins	VSS -0.3	-	0.3 VDD	V
		VIH		0.7 VDD	-	VDD	
Standby Current		IDD1	VDD = 3 V, No Playing	-	-	0.5	μA
		IDD2	VDD = 1.5 V, No Playing	-	-	0.3	
Operating Current		IOP1	VDD = 3 V, No Load	-	-	400	μA
		IOP2	VDD = 1.5 V, No Load	-	-	250	
Input Current for TG1–TG4		IIN1	VDD = 3 V, VIN = 0 V	-	-	2.5	μA
		IIN2	VDD = 1.5 V, VIN = 0 V	-	-	5	
SPK (D/A Full Scale)	Option1	Io1	VDD = 1.5 V, RL = 200 Ω	-0.8	-1.0	-1.2	mA
	Option2	Io2	VDD = 3 V, RL = 200 Ω	-2.0	-3.0	-4.0	
Output Current of SPTC		IOL1	VDD = 3 V, VIN = 0.4 V	1	-	-	mA
		IOL2	VDD = 1.5 V, VIN = 0.4 V	1	-	-	
		IOH1	VDD = 3 V, VIN = 2.7 V	-0.5	-	-	
		IOH2	VDD = 1.5 V, VOUT = 1.2 V	-0.3	-	-	
Output Current	LED1	Io	VDD = 3 V, VOUT = 1 V	6	-	-	mA
	STPA STPB	IOL1	VDD = 3 V, VOUT = 0.4 V	1	3	-	
		IOL2	VDD = 1.5 V, VOUT = 0.4 V	1	2	-	
		IOH1	VDD = 3 V, VOUT = 2.7 V	-1	-3	-	
		IOH2	VDD = 1.5 V, VOUT = 1.2 V	-0.3	-	-	
Oscillation Freq.		FOSC1	VDD = 3 V, ROSC = Typ.	320	384	460	KHz
		FOSC2	VDD = 1.5 V, ROSC = Typ.	320	384	460	
Osc. Freq. Deviation by Voltage Drop		$\frac{\Delta F_{OSC}}{F_{OSC}}$	$\frac{F(1.5V) - F(1.2V)}{F(1.5V)}$	0	10	20	%
			$\frac{F(1.8V) - F(1.5V)}{F(1.8V)}$	0	4	7.5	%
			$\frac{F(3.0V) - F(2.4V)}{F(3.0V)}$	0	4	7.5	%
Input Debounce Time		TDEB	FOSC = 384 KHz	20	30	40	mS

Note: Typ. Rosc = 110 KΩ for two batteries; 100 KΩ for one battery.

The diagram shows the W5230 microcontroller (20 pins) interfaced with an 8050D transistor, a speaker, and an OTP memory. The microcontroller's pins are connected as follows:

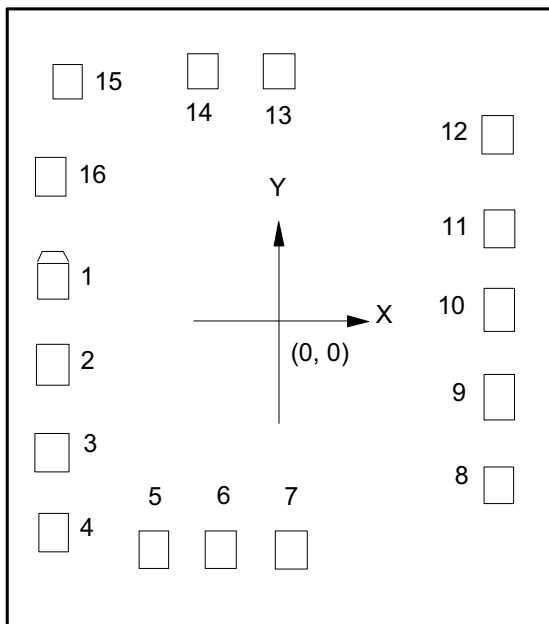
- Pin 1 (TG1):** Connected to a pull-up resistor to V_{DD1} .
- Pin 2 (TG2):** Connected to a pull-up resistor to V_{DD1} .
- Pin 3 (TG3):** Connected to a pull-up resistor to V_{DD1} .
- Pin 4 (TG4/LED2/STPC):** Connected to a pull-up resistor to V_{DD1} .
- Pin 5 (LED1):** Connected to a resistor R and an LED.
- Pin 6 (STPB):** Connected to the base of the 8050D transistor.
- Pin 7 (STPA):** Connected to the base of the 8050D transistor.
- Pin 8 (NC):** Not connected.
- Pin 9 (SPK):** Connected to the emitter of the 8050D transistor.
- Pin 10 (V_{SS}):** Connected to ground.
- Pin 11 (V_{DD1}):** Connected to V_{DD1} .
- Pin 12 (OSCI):** Connected to a resistor R_{osc} and a capacitor C_s .
- Pin 13 (OSCO):** Connected to a resistor R_{osc} and a capacitor C_s .
- Pin 14 (NC):** Not connected.
- Pin 15 (NC):** Not connected.
- Pin 16 (V_{DD2}):** Connected to V_{DD2} .
- Pin 17 (NC):** Not connected.
- Pin 18 (RDP):** Connected to the RDP pin of the OTP memory.
- Pin 19 (DATA):** Connected to the DATA pin of the OTP memory.
- Pin 20 (WRP):** Connected to the WRP pin of the OTP memory.

The 8050D transistor is connected to a speaker (8 ohm, 1/4 watt) and a pull-up resistor to V_{DD1} . The OTP memory is connected to V_{DD2} and V_{SS} .

1. In principle, the playing speed determined by R_{osc} should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varying R_{osc} , however.
2. R_s is an optional current-dividing resistor. If R_s is added, the resistance should be between 470 and 750.
3. R is used to limit the current the LED.
4. C_s is optional.
5. The DC current gain β of transistor 8050 ranges from 120 to 200.
6. All unused trigger pins can be left open because of their internal pull-high resistance.
7. No warranty for production.



BONDING PAD DIAGRAM



NO.	PAD NAME
1	TG1
2	TG2
3	TG3
4	TG4/LED2/STPC
5	LED1
6	STPB
7	STPA
8	SPK
9	Vss
10	VDD1
11	OSCI
12	OSCO
13	VDD2
14	RDP
15	DATA
16	WRP

Note: Substrate is tied to Vss.



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792697

<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-7197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27516023
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

Note: All data and specifications are subject to change without notice.