Two ports 10/100Mbps Ethernet Switch Controller

Winbond LAN
W89C871F
Two Ports Switch Controller

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Revision A1

OVERVIEW DESCRIPTION

The W89C871F is a two-port 10/100Mbps Ethernet switch/bridge single chip controller that provides an excellent performance with extremely low packet lost rate. It is able to forward packets with full wire speed, and bridges the network segments between two auto-negotiated ports. The W89C871F is specifically designed to construct the unmanaged network applications with minimum cost, which are suitable for seamless connecting 10M and 100M Ethernet network segments, bridging two Ethernet network segments and extending 100M Fast Ethernet segments scope.

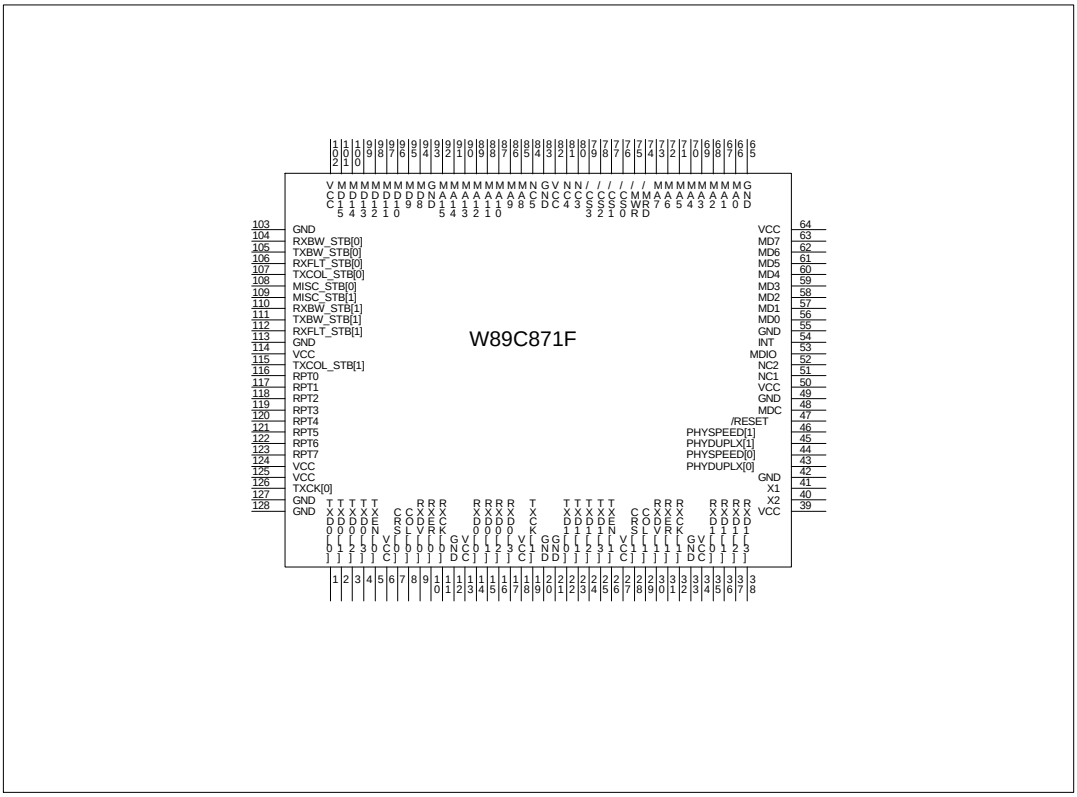
For bridging network segments or forwarding/filtering any data stream, even Virtual LAN tagged frame with unicast or multicast/broadcast addresses at wire speed, W89C871F is implemented many intelligent functions which are hardware address self-learning, filtering and forwarding algorithms supporting up to 4k address entries, as well as advanced active aging algorithm for fully utilizing the space of address table. An active back-pressure flow control for half duplex operation is also implemented to keep buffer memory from overflow.

With its high performance capability, W89C871F implements two deep independent FIFOs on each port with enhanced 32-bit DMA channel to share the packet buffer for full/half duplex operation and different speed network operation. Specially, W89C871F offers a loading balance-like function for the communication between 10M Ethernet and 100M fast Ethernet to prevent from extreme low forwarding performance for 10M network segment if 100M network segment is very busy. Configurable SRAM interface supports a maximum of 512k bytes with different type of SRAM easily sourced, in which 128kx8 or 64kx8 SRAM is fine, as well as a group of control and status registers programmable through MII bus for design and productivity.

FEATURES

- Store and forward switching
- Shared memory for packet buffering
- 14880/148800 forwarding rate for 10M/100M operation respectively
- 4K entries routing table supported
- Two 10M/100M auto-sensing MII ports provided
- Half duplex and full duplex function provided
- Back pressure flow control for half duplex operation provided
- Packet buffer congestion control function provided
- Hardware aging function provided
- Supports VLAN tagged frame
- Network activity status LED displaying function provided
- 128Kx8 or 64Kx16 SRAM interface provided
- Jumper setting for system configuration
- Single 25 MHz clock source
- Single 5V power supply with Winbond advanced low power CMOS process
- 128 pin QFP package

PIN ASSIGNMENT



PIN CONFIGURATION

MII INTERFACE PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
CRS[1:0]	**28,7**	**I**	MII Carrier Sense Input of port 1 and port 0. Asserted by physical layer device(PHY) when media is busy, and de-asserted when media is idle. CRS[1:0] stay asserted, even at the duration of a collision. High means carrier is presenting on the medium.
COL[1:0]	**29,8**	**I**	MII Collision input of port 1 and port 0. Asserted by PHY device (Physical layer controller) once a collision occurred. It will be asserted and lasted until the collision condition thoroughly vanishes. High means collision is presenting on the transmitting and receiving channel of PHY device.
TXEN[1:0]	**26,5**	**O**	MII Transmit Enable Output of port 1 and port 0. High means transmit enable. Transmitted data on each port

			will be valid when its responded signal TXEN[1:0] is high.
TXD0[3:0]	**1-4**	**O**	MII Transmit Data of port 0. Port 0 transmit data bus. This indicates transmission of activity to an external PHY and is synchronized with TXEN[0]. The bus is valid only when the TXEN[0] is high.
TXD1[3:0]	**22-25**	**O**	MII Transmit Data of port 1. Port 1 transmit data bus. This indicates transmission of activity to an external PHY and is synchronized with TXEN[1]. The bus is valid only when the TXEN[1] is high.
TXCK[1:0]	**19,126**	**I/O**	MII Transmit Clock of port 0 and port 1. Both TXCK[1:0] are continuous uniformed clock from external PHY, which provides the timing reference for TXEN[1:0], TXD1 and TXD0. The TXCK[1:0] is either 2.5 MHZ or 25 Mhz clock pulse, determined by each PHY they connected to, respectively. The TXCK is always active after powerup.
RXDV[1:0]	**30,9**	**I**	MII Receive Data Valid of port 1 and port 0. Received data valid signal. Both signals are driven by PHY device. They will assert when data is present, and will be de-asserted at the end of the data frame. RXDVs are synchronized with RXCKs. The received data is valid only when RXDV is high.
RXD0<3:0>	**14-17**	**I**	MII Receive Data of port 0. Receive data from port 0. They are driven by PHY; synchronized with RXCK; valid only when RXDV[0] asserts. RXD0[0] is the least significant bit.
RXD1<3:0>	**35-38**	**I**	MII Receive Data of port 1. Receive data from port 1. They are driven by PHY; synchronized with RXCK; valid only when RXDV[1] asserts. RXD1[0] is the least significant bit.
RXER[1:0]	**31,10**	**I**	MII PHY Receive Error of port 1 and port 0. These pins are driven by PHY device. They indicate that a data conversion error from PHY is detected. The assertion of RXER[1:0] will last for a time longer than a period of RXCK[1:0]. When RXERs assert, W89C871F will report a receive error and a CRC error. High means a receiving error occurred.
RXCK[1:0]	**32,11**	**I**	MII Receive Clock input of port 0 and port 1. The RXCK[1:0] is either 2.5 MHZ or 25 Mhz clock. RXCKs are active all the time after power-up. RXCK and TXCK are allowed to be asynchronous.

SRAM INTERFACE PINS			
MA[15:0]	**92-85, 73-66**	**O**	SRAM Address Bus. W89C871F supports up to 512k bytes SRAM buffer which is capable of being configured to fit 128Kx8 or 64Kx16 SRAM, and stores the received packets, addresses and routing information. The MA[15:0] should be directly connected to the A[15:0] of the memory device.
MD[15:0]	**101-94, 63-56**	**I/O/Z**	SRAM Data Bus. This is a 16-bit width data channel to forward packets between W89C871F and external SRAM devices, and access routing information between W89C871F and external SRAM devices.
MRDB	**74**	**O**	SRAM Read Enable. This signal has SRAM ready to output data to W89C871F. This pin is active low.
MWRB	**75**	**O**	SRAM Write Enable. This signal has SRAM ready to receive data. This pin is active low.
CSB0	**76**	**O**	SRAM Chip Select 0. This pin is internally pulled down and is active low. This pin determines the type of memory configuration and bank. Memory Configuration: Both CSB0 and CSB1 are used to configured the size and the type of buffer memory after power is on or W89C871F is reset. A 4.7k ohm pull-up resistor has to be connected to CSB0 if 256k bytes buffer memory is specified; Floating CSB0 if 512k bytes buffer memory is specified. During the reset operation, W89C871F detects the signal combination of CBS0/CBS1 to tell its memory size and type configuration. The following table shows the memory size configuration in terms of CSB0 and CSB1. CSB0/CSB1 1/1 1/0 0/1 0/0 Memory size 64k16x2 128k8x2 64k16x4 128k8x2 Memory Bank Selection: When CSB0 is active, W89C871F can address the buffer memory space ranged from 0000H to 0FFFH in the configuration mode of 64k16x2 and 64k16x4, or from 0000H to 1FFFH in the configuration mode of 128k8x2 and 128k8x4. See the section Buffer Memory and Bus for details.
CSB1	**77**	**O**	SRAM Chip Select 1.

			This pin is internally pulled down and is active low. This pin acts dual roles, memory configuration and memory bank selection. Memory Configuration: This pin and CSB0 configure the size and the type of buffer memory when power-up or reset. A 4.7k ohm pull-up resistor has to be connected to CSB1 if 64k16 SRAM memory is specified; Floating CSB1 if 128k8 SRAM memory is specified. During the reset operation, W89C871F detects the signal combination of CBS0/CBS1 to know its memory size and type configuration. For simpler, the following table shows the memory size configuration in terms of CSB0 and CSB1. CSB0/CSB1 1/1 1/0 0/1 0/0 Memory size 64k16x2 128k8x2 64k16x4 128k8x2 Memory Bank Selection: When CSB1 is active, W89C871F can address the buffer memory space ranged from 1000H to 1FFFH in the configuration mode of 64k16x2 and 64k16x4, or ranged from 2000H to 3FFFH in the configuration mode of 128k8x4.
CSB2	**78**	**I/O**	SRAM Chip Select 2 and Back Pressure. This pin is internally pulled down and active low. After W89C871F reset, this pin is effective only in the configuration mode of 64k16x4. In any other cases, it is in high impedance. When CSB2 is active, W89C871F will address the buffer memory space ranged from 4000H to 5FFFH. Within about 1ms after powerup/reset time, CSB2 detects if voltage is pulled high by a 4.7k ohms resistor or not. If CSB2 is pulled high, the back pressure function is disabled, if CSB2 is floating, W89C871F will perform the function.
CSB3	**79**	**I/O**	SRAM Chip Select 3 and Back Pressure. This pin is internally pulled down and active low. In the configuration mode of 64k16x4, after W89C871F reset, this pin only acts as a memory chip select signal. In the configuration mode of 256/512k bytes data buffer with the type of 128k8 memory, this pin CBS3 has to be connected to A16 of SRAM. When active, W89C871F will address the buffer memory space ranged from 6000H to 7FFFH. Within about 1ms after powerup/reset time, if CSB3 is

			pulled high with a 4.7k ohms resistor, W89C871F will issue back-pressure pattern for forwarded packet only. If CSB3 is floating, W89C871F will issue back pressure pattern for any packet, included local packet and forwarded packet.

LED INTERFACE PINS			
RPT[7:0]	**123-116**	**I/O**	LED report output and VLAN frame. This pin is internally pulled down and active low. After power-up/reset, W89C871F will have the network status output on the RPT[0:7] with different display mode messages determined by hardware settings. Device ID Select : RPT[0:4] is also used to set ID code for W89C871F being able to be accessed through MDC and MDIO. Setting ID code can be achieved by pulling some of RPT[0:4] high with 4.7k ohms beforehand at system power-up/reset. Within about 1ms after powerup/reset time, RPT[5:7] have the following special functions. At this time frame, RPT[5] will enable VLAN frame function to allow forwarding VLAN tagged frame with 1522 bytes long if it detects a pulled high voltage from a 4.7k ohms resistor. If this is floated, W89C871F will process each packet with the maximum of 1518 bytes long. If RPT[6] is connected to a 4.7k ohm pull high resistor, both MII ports will shrink the backoff time with the same scale to speed up packet processing. If RPT[7] is connected to a 4.7k ohm resistor for pull high, it will perform discontinuous back pressure function when the buffer utilization reaches threshold. W89C871F will lost one packet after every 55 consecutive back pressure pattern in 100M port and every 23 consecutive back pressure pattern are respectively issued.
RXBW_STB[1:0]	**110,104**	**O**	Bandwidth utilization report strobe. A strobe signal to latch each port network utilization report data.
TXBW_STB[1:0]	**111,105**	**O**	Forwarding ratio report strobe. A strobe signal to latch each port forwarding ratio report data.
RXFLT_STB[1:0]	**112,106**	**O**	Filtering ratio report strobe. A strobe signal to latch each port filtering ratio report data.
TXCOL_STB[1:0]	**115,107**	**O**	Collision ratio report strobe. A strobe signal to latch each port collision ratio report

			data.
MISC_STB[1:0]	**108,109**	**I/O**	Miscellaneous Report Strobe. These pins are internally pulled down and active low These two pins are used to latch each port network status report in terms of memory buffer full, Tx/Rx activity, speed, duplex and collision and have them showed on RPT[0:7]. See the section of LED Displaying Interface for details. Duplex Definition: The duplex mode is determined by the combination of MISC_STB[0] and PHYDUPLX from the connected PHY that has completed auto-negotiation. When this pin is active, duplex mode will present on RPT[4]. The following table is the combination of the MISC_STB[0] and PHYDUPLX. There are two kinds of PHYDUPLX output for different brands of PHY, either low or high. MISC_STB[0] PHYDUPLX Duplex mode 0 0 full duplex 0 1 half duplex 1 0 half duplex 1 1 full duplex Speed Definition: The speed of each port is determined by the combination of MISC_STB[1] and PHYSPEED from the connected PHY which has completed auto-negotiation. When this pin is active, Line speed will present on RPT[3]. The following table is the combination of MISC_STB[1] and PHYSPEED. Like PHYDUPLX, PHYSPEED also has two kinds of output for brands of PHY. MISC_STB[1] PHYSPEED Port Speed 0 0 100M 0 1 10M 1 0 10M 1 1 100M

MISCELLANEOUS			
RSTB	**47**	**I**	System Reset. Active low. Minimum 50 us reset pulse width is required when VDD valid.
X1	**41**	**I**	System Clock Source :

			It is required to offer a steady and stable 25Mhz clock source with +/- 50 PPM. This pin should be directly connected to clock source. Oscillator or crystal is available.
X2	**40**	**I**	System Clock Source : This pin should be directly connected to clock source if crystal is applied; floating if an oscillator is applied.
PHYSPEED [1] **PHYSPEED [0]**	**46,44**	**I**	External PHY Device Speed for port 1 and port 0: These two pins detect the line speed status from the responded PHY to determine each port operating speed. W89C871F will blend this bit with MISC_STB[1] to display the speed of each port of W89C871F.
PHYDUPLX [1] **PHYDUPLX [0]**	**45,43**	**I**	External PHY Device Duplex for port 1 and port 0: These two pins detect the duplex mode status from the responded PHY to determine each port duplex mode. W89C871F will blend this bit with MISC_STB[0] to display the duplex mode of each port.
MDC	**48**	**I**	MII Reference Clock : A reference clock for accessing MII management data. The maximum clock rate is 25Mhz.
MDIO	**53**	**I/O**	MII Data Input/Output Bus : MII management data bus.
INT	**54**	**O**	Interrupt Output : An interrupt output indicates that there is an abnormal event detected by W89C871F itself.

POWER&GROUND PINS			
VDD	**6,13,18, 27,34,39 ,50,64,8 2,102,11 4,124,12 5**	**P**	Power supply.
VSS	**12,20,21 ,33,42,4 9,55,65, 83,93,10 3,113,12 7,128**	**G**	Ground.
NC	**51,52,80 ,81,84,**	**G**	No contact.

Note :

P : power pin; G : ground pin; I : input pin; O : output pin; I/O : bidirection pin;

I/O/Z : bidirection pin with high-z state

SYSTEM DIAGRAM

Constructing a dual speed hub or a single 10/100M converter, you can use W89C871F to design them with minimum cost and effort. Like the following example of system application, a typical application, only SRAMs and LED driver has to be implemented. Switching and its related functions are integrated on a chip. This is not only simplifying design effort but saving its size, as well as assembly time.

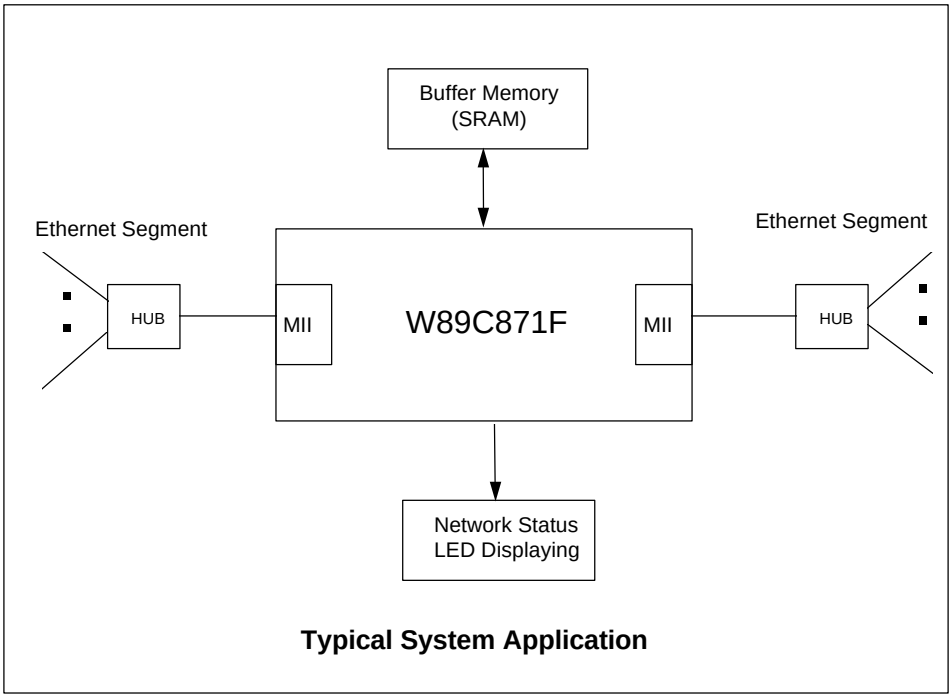


Fig. 1

BLOCK DIAGRAM

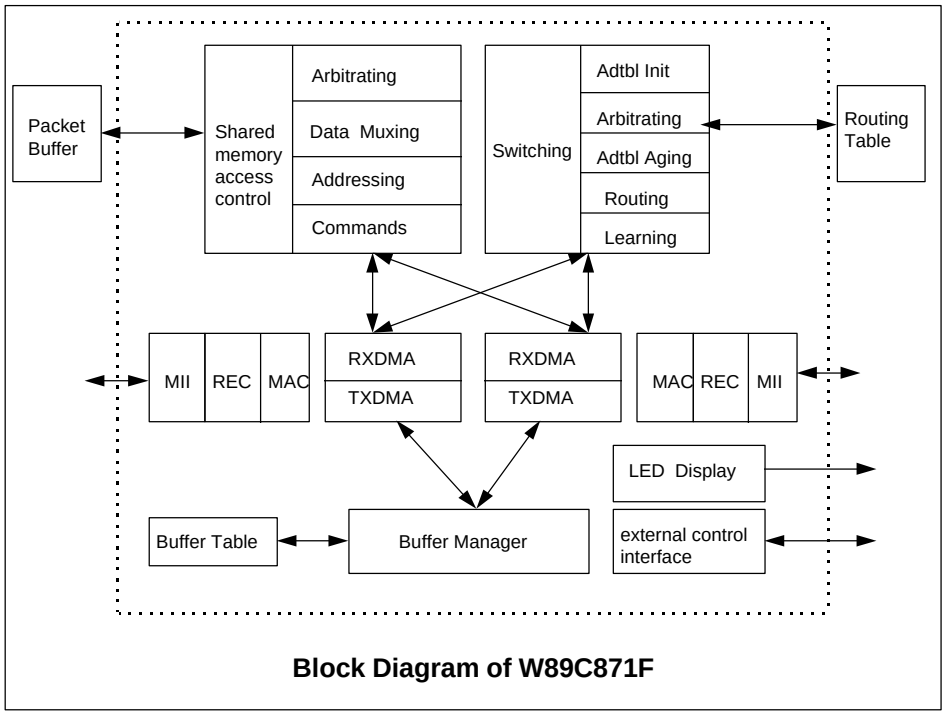


Fig. 2

FUNCTIONAL DESCRIPTION

W89C871F is constructed by the function blocks shown in above diagram. It consists of the function units of switch fabric, buffer management and memory access control, routing, address self-learning and aging, media access controller(MAC) and its DMA, and LED display logic. They will be detailedly described in the coming paragraph.

Buffer Memory and Bus

W89C871F is implemented a configurable memory interface, tied with external SRAM, to construct the packet buffer memory. The size of buffer memory can be configured as either 256K bytes or 512K bytes in the aspect of buffer capacity. There are four configurations available: 64Kx16x2, 64Kx16x4, 128Kx8x2 and 128Kx8x4. All of them have 16-bit data width that can afford totally 400Mbps aggregation bandwidth at 25M Hz operating frequency.

For selecting one configuration out of four, W89C871F supports two pins CSB0 and CSB1 to reach this at power-up stage. After power is on, W89C871F reset itself to its preset initial status. But some status, like memory configuration, are detected from outside at this time interval. CSB0 and CSB1 are some of them. CSB0 and CSB1 must be previously set by hardware before powered on. As soon as power-up, W89C871F detects CSB0 and CSB1 to the memory configuration. CSB0 is for the size of packet buffer and CSB1 is for the type of memory device.

Usually, they are output pins and connect to Chip Select pin(CS) of SRAM, but during the power-on stage after reset, they are input pins for detecting configuration. At this period, W89C871F latches these two signals to initialize internal configure table for the size of packet buffer and its type. The following table shows the combination of the CSB0 and CSB1 at the power-on time. Both CSB0 and CSB1 are pull down internally. When preset it to high, a 4.7k ohm resistor must be serialized to VDD. When preset it to low, just let it floating.

CSB0	CSB1	
1	1	packet buffer size = 256K bytes, memory device = 64Kx16
1	0	packet buffer size = 256K bytes, memory device = 128Kx8
0	1	packet buffer size = 512K bytes, memory device = 64Kx16
0	0	packet buffer size = 512K bytes, memory device = 128Kx8

Table 1

For the above four memory configurations, each corresponds to a different memory space. The following diagram(Fig. 3) shows all configuration and each address map they will be. In CFG1 and CFG3, they are configured to the maximum size of buffer memory. In the former, 4 pcs of 64k16 bytes SRAMs are used; in the later, 4 pcs of 128k8 bytes SRAMs are used. Both are total 512k bytes.

In CFG2 and CFG4 modes, they are the same as that of CFG1 and CFG3 modes, except they are configured to be a half of buffer memory in CFG1 and CFG3.

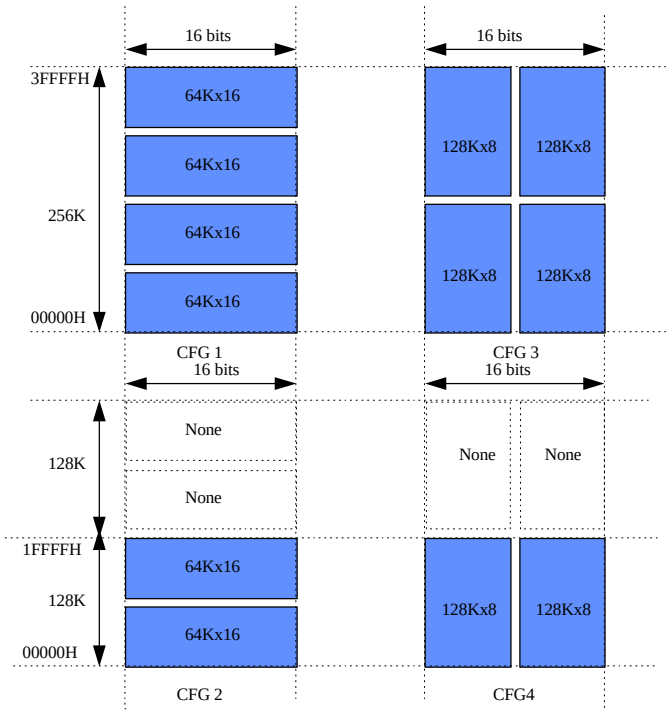


Fig. 3

To successfully configure the memory buffer in a practical application, CSB3 and CSB4 have to be involved. For simplicity, we compose a configure table in which the most left column is the symbols on W89C871F and the remains are the symbols at the memory devices. CSB2 is active only in the CFG1 mode and is floating in the rest modes. CSB3 is floating in CFG2 mode; connected to A16 of SRAM in CFG3&4 modes; connected to Chip Select(CS1) of SRAM in CFG1.

W89C871F	CFG1	CFG2	CFG3	CFG4
D0 ~ D15	D0 ~ D15	D0 ~ D15	D0~D7/D0~7	D0~D7/D0~7
A0 ~ A15	A0 ~ A15	A0 ~ A15	A0 ~ A15	A0 ~ A15
CSB3	CS1	Floating	A16	A16
CSB2	CS1	Floating	Floating	Floating
CSB1	CS1	CS1	CS1/CS1	Floating
CSB0	CS1	CS1	CS1/CS1	CS1/CS1
MWRB	MWRB	MWRB	MWRB	MWRB
MRDB	MRDB	MRDB	MRDB	MRDB

Table 2

In the fig. 4, the practical connections between W89C871F and the external packet buffer are shown. There are four optional pull up resistors shown, which depend on the configurations of the size of buffer memory and the type of memory.

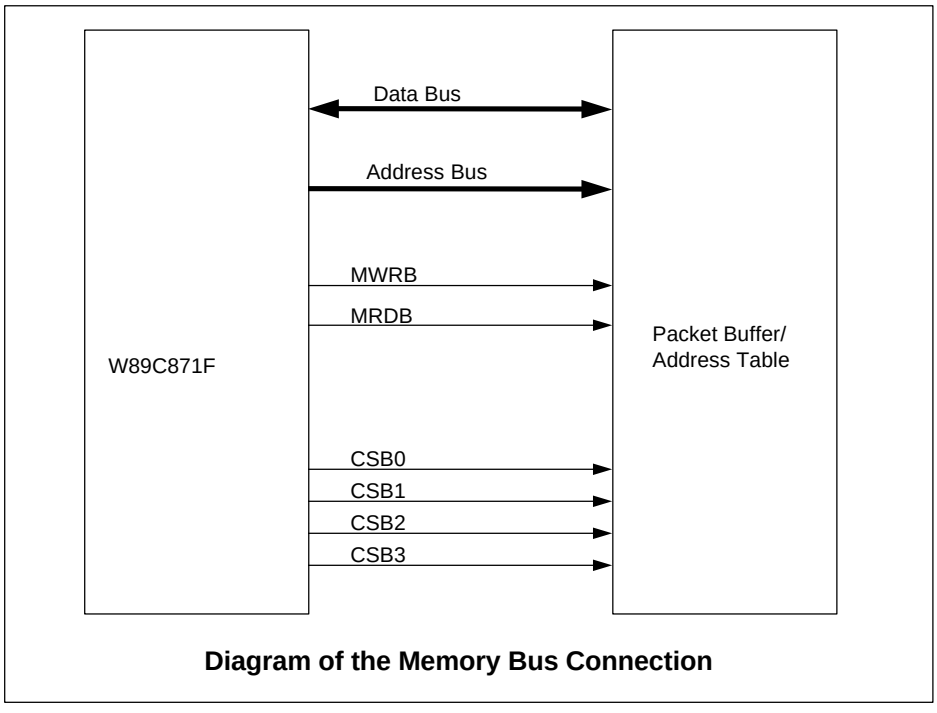


Fig. 4

External Memory Configuration

The external memory is divided into two portions, buffer memory, a place to temporarily store the packets ready to be delivered, and routing information table, a place to store every nodes address and its routing information, came from both ports.

As the description above, W89C871F supports either 256k bytes or 512k bytes, in both of which the first 16k words, counted from the address 0000H to 03FFFH, are reserved for routing information, each of which occupies a consecutive 64 bits, and next, 0.5k words are reserved for future. The mapping is shown in the Fig. 5.

In 512k-byte mode, 239.25k words are allocated for packet buffer that is totally divided to 319 pre-partitioned buffer units each of which is fixed in 1536 bytes long.

In 256k-byte mode, there are totally 158 buffer units that were pre-partitioned and are addressed from 04200H by step of 600H bytes.

VLAN-tagged Frame

Normally, Ethernet packet is 1518 bytes long, but in some special cases, the packet length is more than 1518 bytes. The most well known is VLAN-tagged frame of which the length of packet is 1522 bytes. W89C871F supports this VLAN-tagged packet by only connecting a 4.7k ohms resistor to pull RPT[5] high.

There are at most four thousands (4096) of address entry stored in the address look-up table of W89C871F. Each of them is composed of the information included used flag, port number, aging flag, vendor ID part I, aging index and vendor ID part II. All of which will clearly explain in the next paragraph.

The memory map below detailedly shows the allocated space and its address range. In the diagram of fig. 5, 512k bytes buffer memory is used.

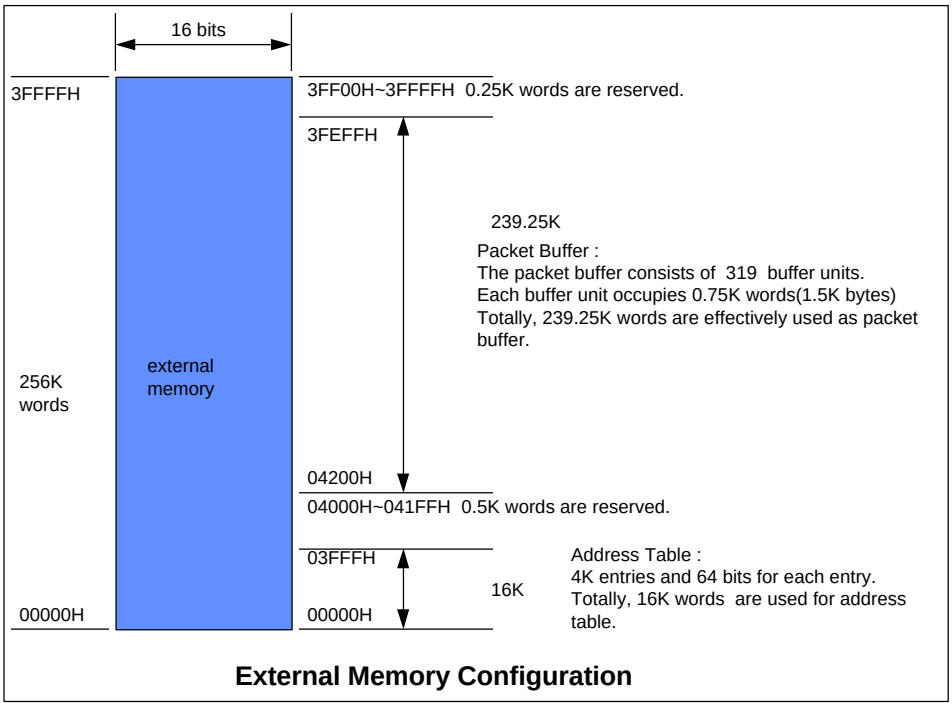


Fig. 5

Address Table Format

The table 5 shows the format of the address entry and the structure of the first five entries each of which has the same structure as that of the rest entries. There are totally 32k bytes reserved for the address look-up table, in which each entry is allocated continuous 4 words of memory, i.e. 64 bits, starting from the address in bytes of 0000H to 7FFFH of the external memory device.

As table 5 shows, address table stores the routing information and is linked to the buffer memory through the transfer of the buffer management unit. When a packet comes, W89C871F will parse the packet and memorize(the so-called self-learning) its source MAC address, and stores this and some specific routing information such as FLG, AGFLG etc., in the address table with the format as Table 5 no matter where this packet was from.

If W89C871F finds that destination address and source address are from the same network segment, i.e. has the same port number, it will not forward the packet and keep quiet listening the source port. If destination and source is located at different network segment, W89C871F will first parse this packet to learn if it is a good packet or not. In case of short packet or packet with errors happened, W89C871F discards the packet or will store it to buffer memory if the packet is good, and meanwhile, write its source address, destination address and routing information to address table, and packet data to buffer memory respectively. This guarantees the packets in the buffer are good.

After having updated routing information, W89C871F starts counting down the aging index of the new updated address entry. When time is out, default value 5 minutes, the address entry will be marked available by cleaning AGFLG and no more count down for this address entry. In W89C871F, when an address entry is accessed, the aging index is updated to be BFH and also set AGFLG.

In half duplex operation mode, if buffer memory is full and next packet is coming, the back pressure flow control of W89C871F will be invoked. W89C871F issues a JAM packet to the

source port to eliminate the possible errors and to suppress transmit action temporarily on that network segment. This will last for a period of time as long as the length of the incoming packet.

If a collision happens, the MAC of W89C871F will start backoff timer to wait for a period of random time and transmit again. When collisions happen continuously 16 times, the packet ready to be forwarded will be discarded and release its buffer space. If W89C871F can not get media, the packet ready to be transferred will be kept in the buffer memory all the time.

In the cases of broadcast and multicast, W89C871F unconditionally forwards all the packet and updates specific entries in the address table to which the source physical address points.

When the opposed segment is idle, W89C871F will forward the packet from memory to that port according to the sequence of the content of the buffer identifier in the buffer ID link list which is controlled by buffer management control unit.

The detail meaning of each field in the address entry is described as following.

FLG: This flag bit determines the content of the bit[0:11] of the address entry in the address look-up table. It is dependent on the address learning machine to set or reset this bit. When set, the content of bit[0:11] of the address entry is composed by the lower twelve bits of the physical address of the source node. When reset, composed by the upper half bits of the lower 24 bits of physical address of source node.

If there is a MAC of which the lower 12 bits of the physical address is mapped into an address entry which is not available in the address look-up table, then an address collision happens. In this case, W89C871F will automatically choose the next available address entry.

PNO: Port number bit. When set, means the packet is from port 1, when reset, means the packet is from port 0. W89C871F receives each packet from either port 0 or port 1, but will be released immediately when it detects that the destination port of the received packet is the same as its source port. If the destination port is different from its source port, the packet will be stored in buffer memory. W89C871F then updates the address entry and starts to count down aging index.

For the case of which there are two same MAC address from different port, W89C871F will have the packet stored in the same buffer location and update the content of the address entry storing the routing information of the previous packet alternately according to their arrival time.

AGFLG:Aging flag bits. These two bits are used to designate if the address entry is in use or not. When set, means in use, when reset, means available.

ID pattern: This field contains the content of the bits 0-11 or bits 12-23 of the Ethernet physical address. If FLG bit is set, this field contains the content of the lower twelve bits of the first half of the physical address; if reset, it contains the content of the upper twelve bits of the first half of the physical address.

Vendor ID part I:This field contains the content of the bit39-24 of the Ethernet physical address. This is a part of the Organizational Unique Identity code(OUI) and should be applied to IEEE.

Aging Index: This index indicates if the entry is time-out. If it is time-out, i.e., this entry has not been accessed within five minutes, then W89C871F will reset AGFLG bit and release the address entry for other use. W89C871F checks this field many times a second, and updates its content as BFH if it is accessed. In W89C871F, Default aging time is five minutes.

Vendor ID part II: This field contains the content of the bit47-40 of the Ethernet physical address. A full OUI code is constructed by combining this field and Vendor ID part I. This is a part of the Organizational Unique Identity code(OUI) and should be applied to IEEE.

Reserved: This field is free for future use.

No.of entry	memo. addr.	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0
0000H	0000H	flg	pno	ageflg		ID Pattern (12 bits)											
	0001H	vendor ID part 1															
	0002H	age index													vendor ID part 2		
	0003H	reserved															
0001H	0004H	flg	pno	ageflg		ID Pattern (12 bits)											
	0005H	vendor ID part 1															
	0006H	age index													vendor ID part 2		
	0007H	reserved															
0002H	0008H	flg	pno	ageflg		ID Pattern (12 bits)											
	0009H	vendor ID part 1															
	000aH	age index													vendor ID part 2		
	000bH	reserved															
0003H	000cH	flg	pno	ageflg		ID Pattern (12 bits)											
	000dH	vendor ID part 1															
	000eH	age index													vendor ID part 2		
	000fH	reserved															
0004H	0010H	flg	pno	ageflg		ID Pattern (12 bits)											
	0011H	vendor ID part 1															
	0012H	age index													vendor ID part 2		
	0013H	reserved															

Table 3.

The Operation of the Address table

Initialization

After power-up/reset, the initialization of the address table starts. The hardware reset can be reached by power-up or hardwiring the reset pin to ground. The following diagram shows the initial operation of the address table.

At the initial phase, W89C871F will have the first word(16 bits width) of each address entry of the address table cleaned as 0000H, in which a continuous 64-bit long memory was allocated to each address entry. Hence, this 0000H will be in orderly written to each entry, addressed at 1FFEH, 1FFAH, ... , 000AH, 0006H, and 0002H. After finished initialization, the state machine enters the idle state and waits for servicing the incoming packet.

During initialization, W89C871F allows to stop the initial operation for some purpose by resetting the bit 7 of the control register. This will have some un-initialized address entries

uncertained so that less than 4k address entries are available within 5 minutes after power up. All 4k address entries are available at 5 minutes later after power-up. The bit 7 of the control register has the highest priority on the machine control. The state machine will stay at the idle state whenever the StopAblInit signal is asserted.

The following diagram shows the initial sequence and its related state in the next paragraph.

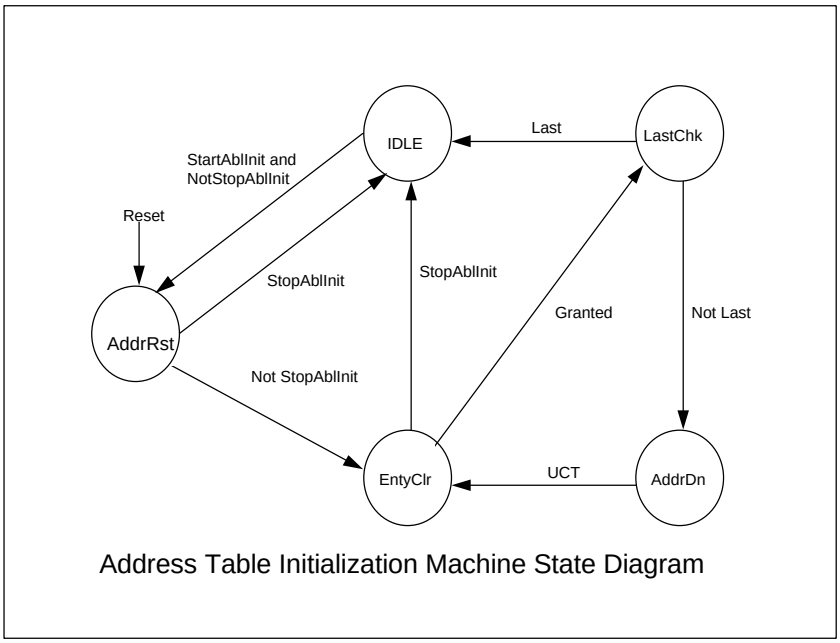


Fig. 6

In Figure 6, we will see how the state machine of the address table works at the initial phase. Here, we will explain the meaning of the states and the events to next state.

IDLE : Idle state.

The state machine always stays at the IDLE state whenever compulsorily stopping the initialization operation(StopAblInit) happens or the initialization is normally completed(Last). If the initial command from the control register is issued, the state machine will enter AddrRst state to perform the initialization of the address table. Normally, the address state machine always completes the initialization and is ready for identifying the routing information status of the income packet.

AddrRst :Address reset state.

This is the entry point of the address state machine. After power on hardwire reset, the state machine automatically enters this state. Another way is by programming the control register

through MDIO to have StartAblInit set and StopAblInit reset, shown in the diagram. This will have address state machine interrupted and force to be in the AddrRst state. In W89C871F, no matter it is reset by hardware or software, the state machine starts formatting the address entries in sequence from the top high address of the address table, i.e. 4096 to 0.

EntyClr :Address entity clear state.

A request to write 0000H to the address table will be issued to get a grant from buffer management control unit to clean the first 16 bits of each address entry when the address state machine stays at the EntyClr state.

LastChk :Last entity check state.

As soon as the address entry clean request is finished, the address state machine enters LastChk state to check if the current address entry being serviced is the last one in the address table or not. If the last one is reached, the address state machine will go to the IDLE state, otherwise, it will enter to the AddrDn state.

AddrDn :Address count down state.

In this state, the address state machine will count down by one and point to the next address entry in the address table.

Address Aging

It is possible to move a MAC address crossing over a network bridge, especially for notebook PC. In such a case, W89C871F can detect the change soon and update its address table accordingly. W89C871F implements an intelligent address recognition mechanism to support this operation. It supports hardware aging function with default value 300 seconds which is fixed and no need to re-configure it. W89C871F checks each address entry 191 times per second based on 25Mhz system operation clock. If any address entry is not accessed within 300 seconds, it will be removed automatically from the address table. There is an age timer to generate the trigger signal pulse with the width of 120ns for starting aging the address entry of the address table. The frequency of the trigger signal is depended on the LifeTime setting. If LifeTime is set to be 1, it means that aging time is one second. If the LifeTime is set to be 100, it means the aging time is 100 seconds.

For getting the time reference, there is a 5 bits ripple counter implemented to generate a 781.25 Khz clock based on 25 Mhz Clock input. This 781.25 Khz clock is fed to the input of a twenty bits count down counter which was preloaded an initial value the same as the LifeTime had been set previously. Each time the counter reaches zero, W89C871F will issue an AgeTrig pulse as well as reload the value of LifeTime to the twenty bits count down counter for next trigger. The LifeTime can be set by programming the age time register through MDIO and MDC, MII serial management interface.

When AgeTrig pulse is issued, the age index of all the 4096 address entries will be counted down by 1. Hence, if LifeTime is set to be 2 and all the age index of the 4096 address entries are 191(BFH), all the 4096 entries can be aged out 2 seconds later.

The aging mechanism can not be started if the bit 3 of the control register is reset to low, and the aging timer is inhibited as well.

The following equation shows the above conclusion, based on 25Mhz operating clock and LifeTime=2.

40ns x 32 x 2 x 4906 x 191 = 2.00278016 second

The following diagram shows the state diagram of the aging operation.

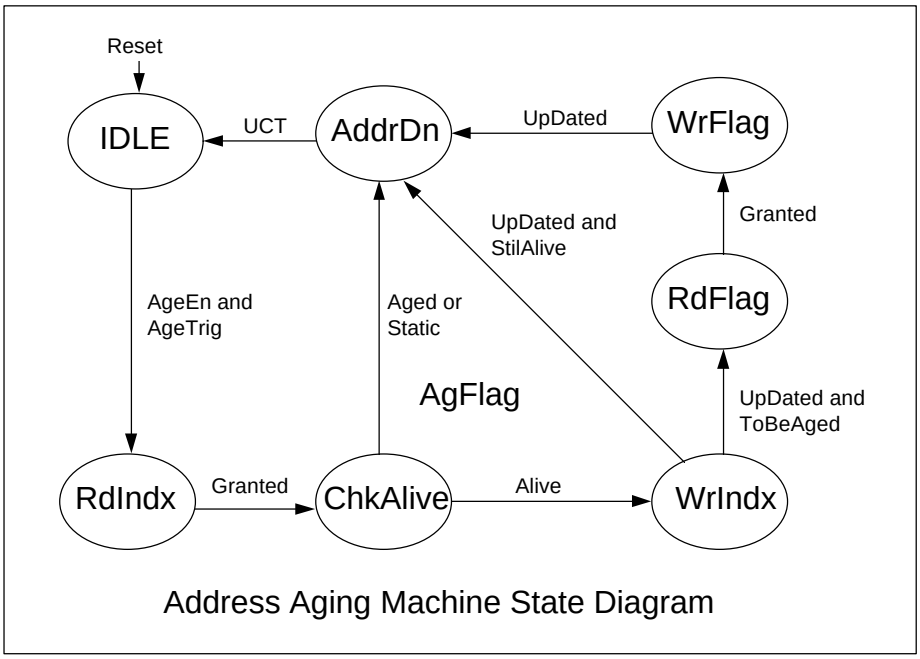


Fig. 7

The Operation of Address Aging

The address aging operation shown above states how it works detailedly. After power-up or reset, W89C871F have the address aging state machine entered into IDLE state to wait for servicing. When a packet is receiving, both AgeEn and AgeTrig will be set to allow accessing the age index of the address entry(RdIndx state). If granted by buffer management control unit, the address aging device reads the age index and parse it to learn if the address entry is still alive. If it is not alive, then the address aging device will enter into AddrDn state. If it is alive, the address aging device will update the address entry and directly enter into AddrDn state. If the address aging device detects the address entry is time-out, it will update its contents and reset its Ageflg and Age Index to mark available for this entry. The following paragraph describes the states of the address aging state machine and its relations.

IDLE :Idle state.

The address aging device always keeps in the IDLE state whenever the aging function is disabled or the aging timer is still counting down. The machine will leave the IDLE state if the aging function is enabled and the AgeTrig signal is received.

RdIndx :Read the age index of the address entry

At this state, the address aging machine issues a data read request to the buffer management control device to get a grant for accessing the aging index of the address entry, stored in SRAM. The address aging machine reads the third word of the address entry to get the age index value.

ChkAlive :Age index check state.

After the age index is read and parsed, the aging state of the address entry will be checked. The aging state has three types: alive, aged and static. Alive state means that the age index of the address entry is larger than 00H but smaller than or equal to C0H. Aged state means that the address entry has released for other`s use, and has an age index with 00H. Static state means that the address entry is blank and available, and its age index has valued other than 00H~BFH.

WrIndx :Update aging index.

At the WrIndx state, the address aging machine issues a write request to the buffer management control unit for getting a grant to update the age index of the current address entry. The age index will be decreased by one each time the age index is updated, i.e. the age index is count down when the age index is updated.

AddrDn :Address count down state.

The addressing logic of the aging device will count down the pointer of the address entry when the address aging machine enters AddrDn state.

RdFlag:Read back the age flag state.

The age flag indicates the aging state of the address entry. If it is still alive, the age flag is equal to 1H. If it is aged out, the age flag is equal to 0H. If it is static, the age flag is equal to 3H. The age flag with the value 2H means nothing. Not all the aging operation needs to update the age flag. The address aging machine will update the age flag only when the age index counting down from 01H to 00H. Before updating the age flag, the rest bits of the first word of the address entry pointer currently pointed to must be read back for keeping the consistency.

WrFlag:Write the age flag state.

After the data of the first word of the address entry has been read and parsed, the address aging machine updates the age flag only at the WrFlag state.

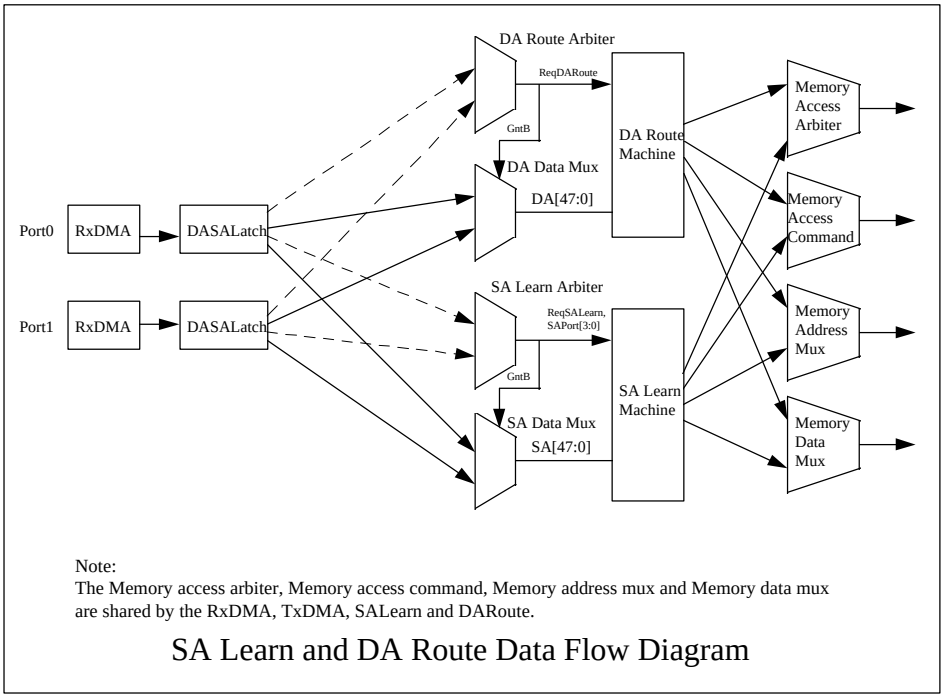
THE OPERATION OF THE PACKET SWITCH

Data Flow of Switching

The switching operation of W89C871F is receiving incoming packets from ports, and searching the address table for the destination MAC address according to the destination address of the packet, and then forwarding the packet to the other port if the port number of destination and source is different. For multicast and broadcast packets, W89C871F forwards packets directly

without identifying. During the time to forward the packet, W89C871F abstracts all the source MAC address(SA) and keep them, accompanied with other information, in the address table with the structure form as shown in the Table 3. This is hence building an address table for filtering. The destination MAC address is used to tell the port where a packet should be routed to.

The following diagram shows how the packet data flows.



Note:
The Memory access arbiter, Memory access command, Memory address mux and Memory data mux are shared by the RxDMA, TxDMA, SALearn and DARoute.

SA Learn and DA Route Data Flow Diagram

Fig. 8

All the packet is received by RXDMA in which a receive FIFO is constructed to queue the data temporarily. The DASALatch extracts the destination address(DA) and the source address(SA) from RXDMA device. When DASALatch completed latching DA and SA, it will issue a request to the address state machine for routing and learning. The address state machine includes the SA learning machine and DA routing machine. The former is responsible for serving the learning request, and the later is responsible for the routing request. These two operations are done by the cooperation of the memory access arbiter, memory access command control and memory address/data MUX. They may conflict while accessing the buffer memory at the same time. It is arbitrated by memory access arbiter. Due to implement such an intelligent memory access arbiter, W89C871F can perform a loading balance-like operation between the communication of 10M and 100M network segments. In the case, 10M network transmits/receives packets slower 10 times than Fast network does, the packets from 100M segment will always wait for 10M segment digestion or the port to 100M segment will always wait for getting the packets. This could degrade the system performance. W89C871F improved this by balancing the packet loading ratio for 10M and 100M Ethernet.

MAC Address Learning Procedures

W89C871F implements a smart address searching algorithm to perform the operation of searching, learning, and updating the address entry of the address table. For the MAC address learning operation, W89C871F extracts the source MAC address(SA) of an incoming packet and searches if the same one existed in the address table. If SA is found, W89C871F updates the aging index, if not found, W89C871F creates and updates the address entry of the address table with all data with the structure shown in Table 3, and stores the packet in the buffer memory pointed by buffer ID. But packet will be released soon if the destination MAC address(DA) is a unicast address and the address was found in the address table and the port number is the same as that of source port. This means the packet is filtered.

Physical address is sorted to be three types of address:unicast, multicast and broadcast. If the first bit of the DA is 0, the packet is unicast, which means that the packet can only be received by a single network node. If the first bit of the DA is 1, the packet is multicast, which means a group of network nodes will receive it. If DA is composed of all 1s, the packet is broadcast, a special type of multicast, all nodes in the network will receive it.

According to the rule of IEEE. The MAC address, 48 bits long, consists of two parts, one is the vendor ID field, higher 24 bits, and the other is the customers` serial number, lower 24 bits. The address searching algorithm compares the full address of the source MAC address(SA). The 24 bits of the serial number is divided to two halves. Either of these two halves may be used as an address index of the address entry of the address table. There is a search flag defined for the search operation of the address table. The search flag is 0 if the address learning machine searches the address table based on the lower half of the 24 bits serial number of the source MAC address of the received packet, and is 1 if the address learning machine searches the address table based on the upper half of the 24 bits serial number of the source MAC address of the received packet.

During the learning procedures, there will be three words read for each entry search. They will include, 8 bits age index, 24 bits vendor ID, 1 bit input port ID, 1 bit addressing flag, 2 bits age flag and 12 bits serial number. The age flag indicates that if the address entry is in use or available or not. If alive, the age flag is equal to 1H. If dead, the age flag is equal to 0H and means available. The value of 2H and 3H of the age flag means nothing and will not be allowed. An alive address entry means that the value of the age index is larger than 00H and lower than C0H and is active. An aged address entry means that the address entry has an age index equal to 00H and has been released. The age index with number larger than C0 has not been defined and will be not allowed.

If the address table is full, and no one address entry is aged out, and a packet with new source address comes at this moment, W89C871F will perform the address recognition procedures the same as that of normal case, i.e. update the oldest address entry with the new information of the received packet. Thus the old one is wiped out from the address table.

A hit to an address entry must meet the following requirements, this means the matched was found.

1) The contents of the 24-bit vendor ID in Table 3. = that of the upper half 24 bits of the source MAC address of the received packet.

2) The age index is not equal to 00H and not larger than BFH.

3) The age flag is 1H.

4) The addressing flag is 0

5) The serial number, i.e. ID pattern bits of the data structure in Table 3, is equal to the contents of the upper 12 bits of the serial number of the source MAC address of the received packet.

6) search flag is 0

or

1) The contents of the 24-bit vendor ID in Table 3. = that of the upper half 24 bits of the source MAC address of the received packet.

2) The age index is not equal to 00H and not larger than BFH.

3) The age flag is 1H.

4) The addressing flag is 1

5) The serial number, i.e. ID pattern bits of the data structure in Table 3, is equal to the contents of the upper 12 bits of the serial number of the source MAC address of the received packet.

6) search flag is 1

The following diagram shows the operation of the address self-learning.

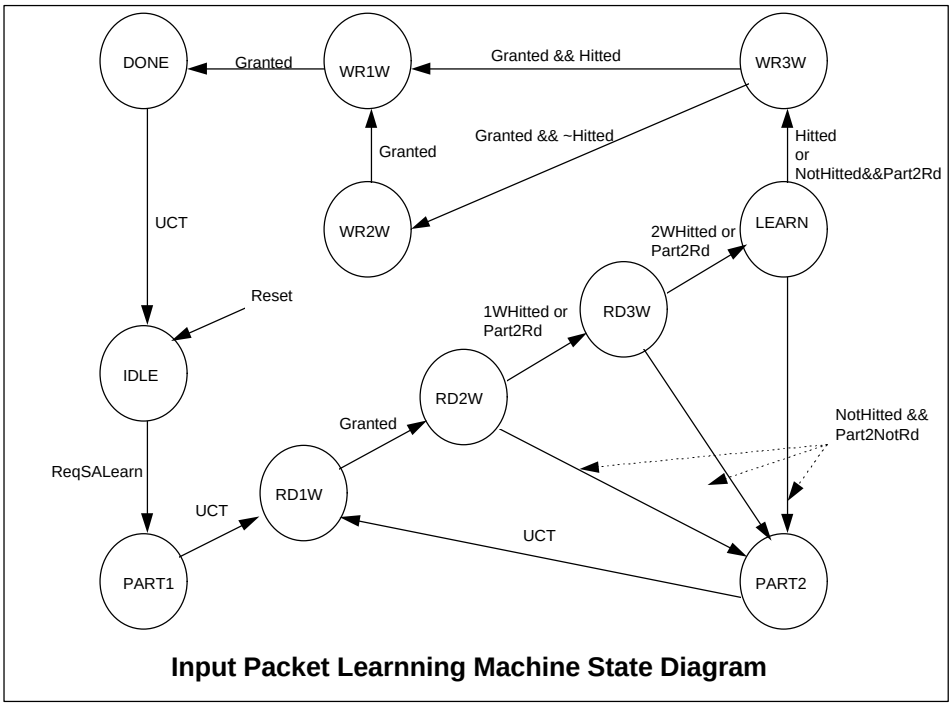


Fig. 9

IDLE :idle state.

The address learning machine keeps idle when no packet is coming or system is power-up/reset or state machine just finished the job.

PART1 :set search flag state.

The address learning machine resets the search flag to 0 at this state. The bits 0-11 of the serial number of the source MAC address (SA) will be used as the address search index.

PART2 :set search flag state.

The address learning machine resets the search flag to 1 at this state. The bits 12-23 of the serial number of the source MAC address will be used as the address search index.

RD1W, RD2W, RD3W :read data state.

The address learning machine read the first 3 words of the address entry at the state of the RD1W, RD2W and RD3W respectively.

LEARN :learning state.

The address learning machine identifies if an address entry is matched or not at this state.

WR1W, WR2W, Wr3W :write entity data state.

The address learning machine will write the routing data to the first 3 words of the address entry at the state of WR1W, WR2W and WR3W respectively.

DONE :Done state.

DA Routing Procedure(address recognition and aging)

W89C871F forwards the packet between ports according to destination MAC address(DA). In the routing procedures, the DA routing machine first do the address recognition which detects if the packet is an unicast one. If yes, it will search the address table to find the matched address entry and compare if the port number of the matched address entry is the same as the source port. If they are different, then the packet is forwarded, otherwise, the packet is discarded. If the DA can not be found in the address table, W89C871F will unconditionally forward the packet to the opposed network segment, as if it is multicast/broadcast packet and memorize its source address and related information in the address table with the form of the structure as table 3.

When finishing the address recognition, W89C871F checks if the following requirements are matched. They are addressing flag, age flag, serial number, and vendor ID etc. Should they meet the requirements, the routing machine will route the packet to its destination.

1) The age flag is 1H.

2) The addressing flag is 0

3) The serial number, i.e. ID pattern bits of the data structure in Table 3, is equal to the contents of the upper 12 bits of the serial number of the destination MAC address of the received packet.

4) search flag is 0

or

1) The age flag is 1H.

2) The addressing flag is 1

3) The serial number, i.e. ID pattern bits of the data structure in Table 3, is equal to the contents of the lower 12 bits of the serial number of the destination MAC address of the received packet.

4) search flag is 1

The operation of the routing state machine is shown in the figure 10. After power-up/reset or no routing activity, the routing state machine stays at IDLE state. When capturing DA of a received packet, the routing state machine enters the PART I state which searches the matched address entry based on the address index claimed by the content of the lower twelve bits of the serial number of the physical address of the received packet. And next, read the first word(16 bits) of the matched address entry, which is composed of address entry flag, port number, age flag and ID pattern bits. After extracting these data, the routing machine parses and identifies them if the address entry is a matched one which meet the requirements listed above. If matched, the second and the third word will be reading in order, which are composed of age index and vendor identifier. If unmatched, the routing machine will alternatively use the higher twelve bits of the serial number of the DA of the received packet and repeat the operation it just did.

With them, the routing machine can detect if the received packet has the same vendor ID as that of the matched entry, and if the matched address entry is available or in use. If available, it means the DA does not exist in the address table. If it is in use, routing state machine will set search flag as 0, and alternatively, re-searches another address entry addressed by the content of the higher twelve bits of the serial number of the DA of the received packet and repeat the operation it did. If the entry found in second time is still in use, it means that the DA does not exist in the address table. The packet will be forwarded directly.

When finished parsing the first three words and ascertained that the DA of the received packet was found in the table, the port ID will be compared to decide if the packet should be forwarded or not. When finishes, routing state machine will enter the DONE state and next to IDLE state.

The following paragraph describes the operation and meaning of the states of the routing machine.

IDLE :

idle state.

The routing machine keeps idle when no routing activity or after power-up/reset.

PART1 :

set search flag state 1.

The routing machine reset the search flag to 0 at this state. The content of the lower twelve bits of the serial number portion of the destination MAC address will be used as the search address index to get routing information.

PART2 :

set search flag state 2.

The routing machine set the search flag to 1 at this state. The content of the upper twelve bits of the serial number portion of the destination MAC address will be used as the search address index to get routing information.

RD1W, RD2W, RD3W :

read entity data state.

The routing machine read the 1st, 2nd and 3rd long word of the entity at RD1W, RD2W and RD3W respectively.

3WLRN :

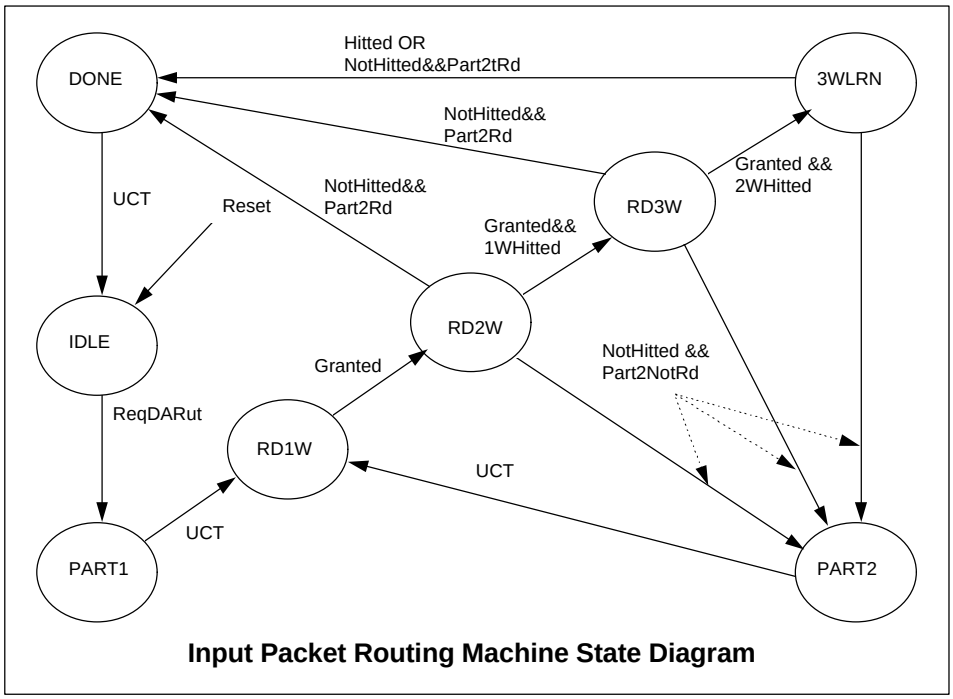
one entity learning state.

The routing machine identify if the whole entity is a hit entity or not at this state.

DONE :

done state.

It implies that the routing process for current routing request is done when the routing machine entering this state.



Input Packet Routing Machine State Diagram

Fig. 10

External Memory Access Control

W89C871F only supports store-and-forward mode. All packet which is necessary to cross over the bridge will be stored in the external memory which is openly accessed by many devices(see Fig 11) inside W89C871F. The external memory access control function of W89C871F includes the following 4 sub-functions.

1) The external memory access arbitration function.

2) The external memory access addressing function

3) The external memory access data multiplexing function

4) The external memory access commands control function

Memory Access Arbitrating

Due to store the address table and the packet data in the external SRAM, and the address table is accessible by the SA learning machine, the DA routing machine, the address table initial machine and the address entries aging machine, as well as by the TXDMA and RXDMA state machine for the packets. Furthermore, both of the data of the address table and the packet are accessible by the external CPU in the test mode. The memory access arbiter is used to handling the arbitration of the memory access requests issued from different devices.

The following diagram shows how the arbitration operation is done and its related devices which need to access the external memory device. In the diagram, all the device which needs to access the external SRAM is shown.

Each of all the device shown in the diagram will issue a request to the memory access arbiter when some condition, which was described in its related paragraph, is satisfied. They are independent one another. Among them, the operation priority is dynamic, but basically, there is a rough operation priority existed and listed below.

Routing operation has the highest priority. The second priority is for receive operation and next is for transmit operation. The priority of 100M operation is slightly higher than that of 10M operation. The SA learning operation has lower priority to access memory device. Updating the aging index of the address table and initializing the address table have the lowest priority. For more clear, expresses the related priority among them in the form of list.

DAroute > 100M Receive operation > 100M transmit operation > 10M Receive operation > 10M Transmit operation > SA learning operation > Updating Aging Index > Initializing Address table.

This is a basic rule, not an absolute one. The arbiter dynamically assigns the operation priority to each device for different operation.

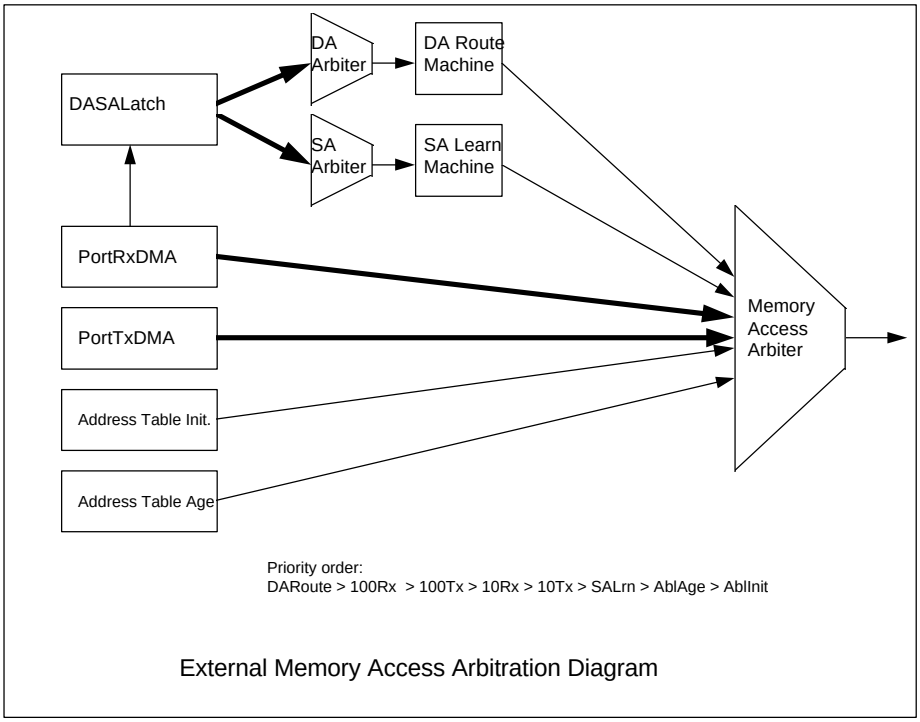


Fig. 11

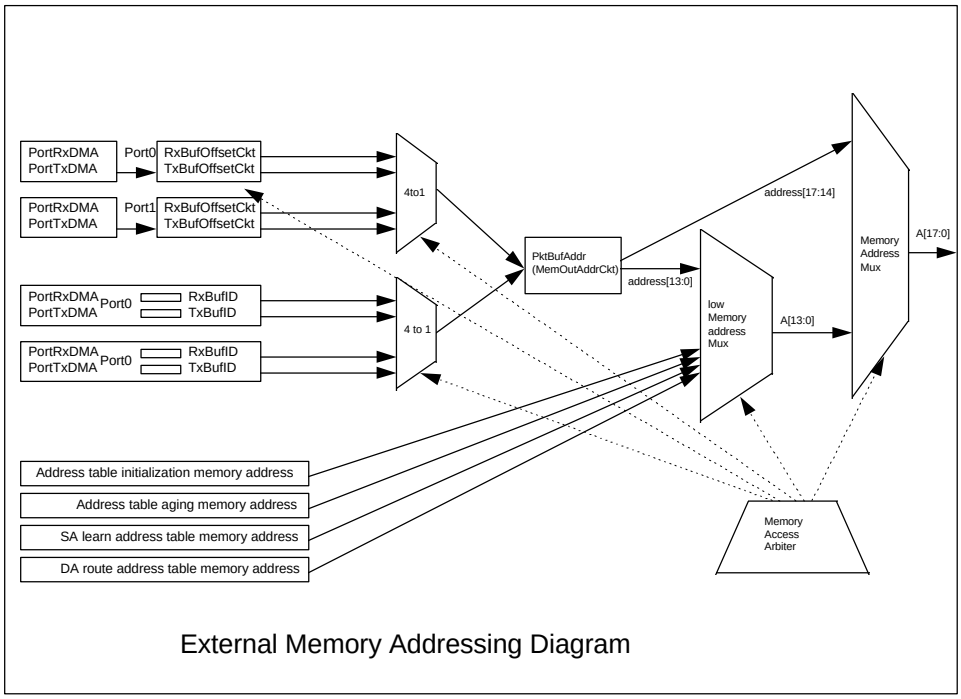
Memory Access Addressing

The data accessed in the memory has to be addressed. In W89C871F, data is stored/retrieved by 16-bit word, not a whole packet. It is necessary to claim each word absolute address which is determined by the addressing logic based on the information from the buffer management unit, described in the next paragraph. The diagram below(Fig. 12) shows how it works, operating blocks and flow path.

All of the MUX(multiplexer) is controlled by the memory access arbiter. The DA routing, SA learning, address table initialization and address table aging devices will generate its own absolute address which occupies the first 16k words of external SRAM.

For the path of RXDMA and TXDMA, the address to store each packets is combined by the BufID pointer and the BufOffset. The BufIDs are pointers stored in the buffer management link list and are used to compose of the base address of each packet buffer unit. The BufOffset is the offset address of each packet buffer unit, which always exactly points to the address being accessed within the packet buffer unit.

After combining these two address pointers, Memory Address Multiplexer can come out a unique 18-bit long absolute word address to access the data. As concerns which path will be enabled to allow passing data, it is wholly determined by the memory access arbiter. Though more than one device issues memory access request. based on the base address of the specific packet buffer and the offset address of the long word data, only one request will get grant to access memory. In Figure 12, Dash line means arbiter control signal.



External Memory Addressing Diagram

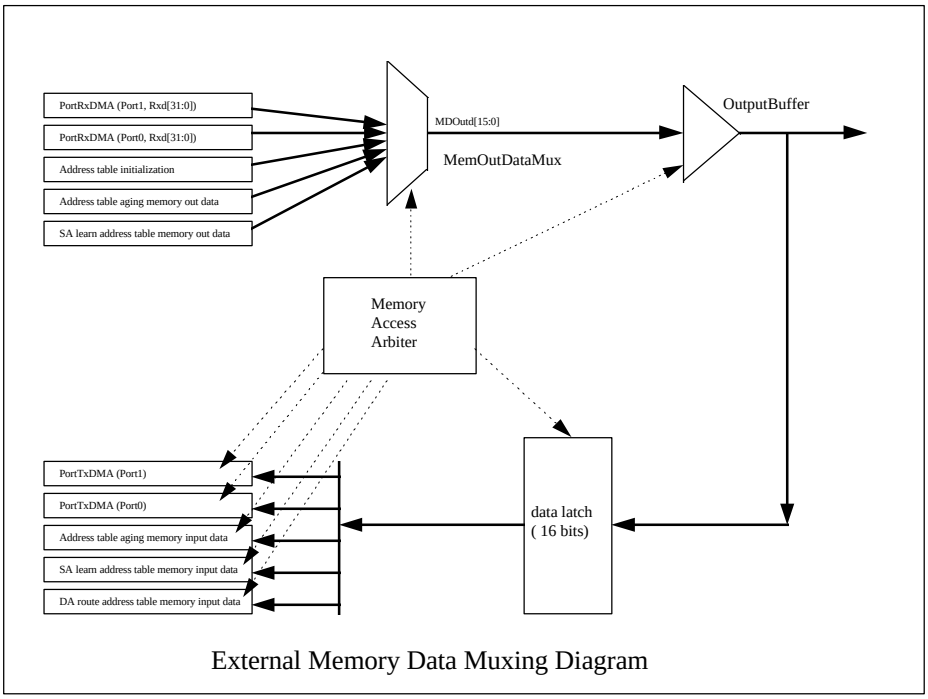
Fig 12

Memory Data Multiplexing

Like the memory addressing operation, all of the data read from or written to the buffer memory will be multiplexed under the control of the memory access arbiter. They determine which state machine can pass its information to next one at the time interval issued by memory access arbiter and manage bus from collision or dead lock. Only the granted memory access request can hold the data bus to access the buffer memory. In the figure 13, the block diagram of the multiplexing operation is shown.

Memory Access Enable

Memory access enable here means W89C871F will issue a set of memory access signals to the buffer memory to synchronize and in-phase the system clock when memory access arbiter and data path is ready. With them, W89C871F can retrieve or store data, routing information etc. on the buffer memory without trouble such as timing error. In W89C871F, The memory access enable cycle is synchronized with the system operating speed. Any read cycle or write cycle will be finished within one system clock pulse. The system operating clock is 25 Mhz and each memory access cycle is limited below 40 ns. The block diagram of the memory access enable is shown below.



External Memory Data Muxing Diagram

Fig. 13

Buffer Manager:

Buffer manager is the center to assign where the packet should be placed or retrieved in the buffer memory. It knows which memory block is occupied or available, and controls the allocation and freeing of the memory block, as well as manages the base address list(buffer ID list) of the packet. Statements below describe the jobs of the Buffer manager and its operation. In the Fig. 15, it shows the its structure and operation flow detailedly.

1) Formatting the data buffer memory (512K / 256K bytes) to be 341 / 170 blocks with 1.5k bytes each, and assigning a number to each block as buffer ID to have the memory access addressing device being able to figure out the correct base address where the packet data in the buffer memory will be accessed. (The buffer IDs 0~21 are reserved for the address table).

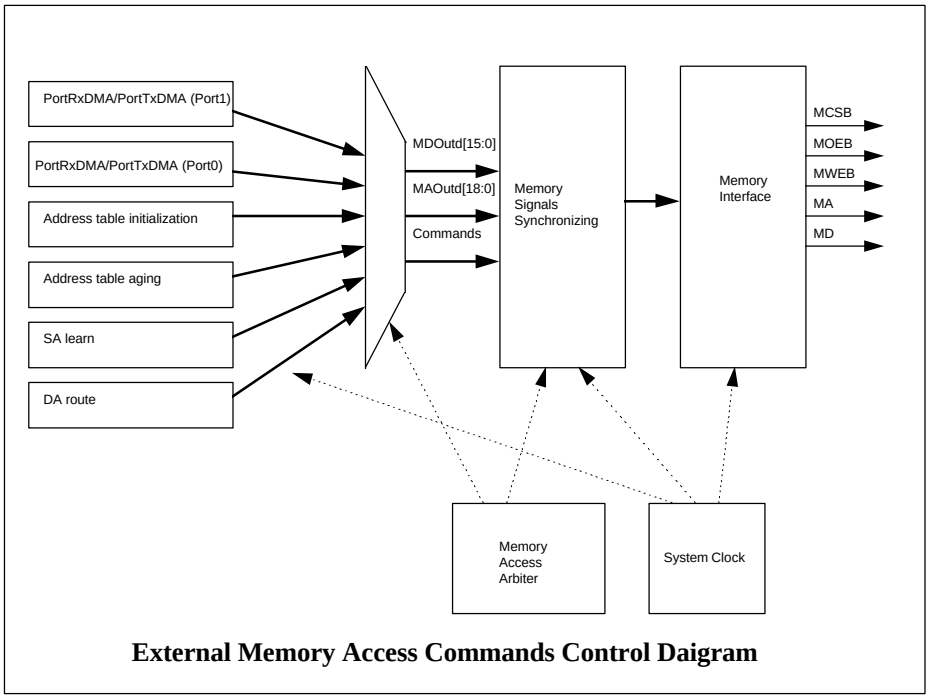
2) maintaining the link list of the buffer IDs, which should be allocated for each forwarding packet dynamically. After a while, the buffer ID is no longer in order, but a random sequence.

3) The buffer manager interfaces to the rx_interface and tx_interface of each port, it allots the free buffer IDs to the rx_interface and recycles the buffer IDs from the tx_interface.

4) A free buffer ID is requested by the rx_interface for a packet receive, and by the tx_interface for the packet transmit. When buffer ID is assigned to a packet, it will be marked in use.

5) The buffer manager also performs the congestion control function : if the incoming packet is much more than the outgoing packets at a time interval, the number

of the free buffer ID is reduced dramatically and may cause the buffer memory full. While a port used up its free buffer IDs, the buffer manager will raise a flow-control alarm signal in order to "back-pressure" the transmitter for avoiding buffer overflow.



External Memory Access Commands Control Daigram

Fig. 14

Buffer Table:

The buffer table is the link lists of the free buffer IDs and the packet buffer IDs and is built in the chip.

Each port of W89C871F has its own packet buffer IDs link list to form the transmitting sequence. And the only one free buffer IDs link is shared by the two ports.

The Buffer Manager Structure:

1. The following diagram shows the structure of the buffer manager.

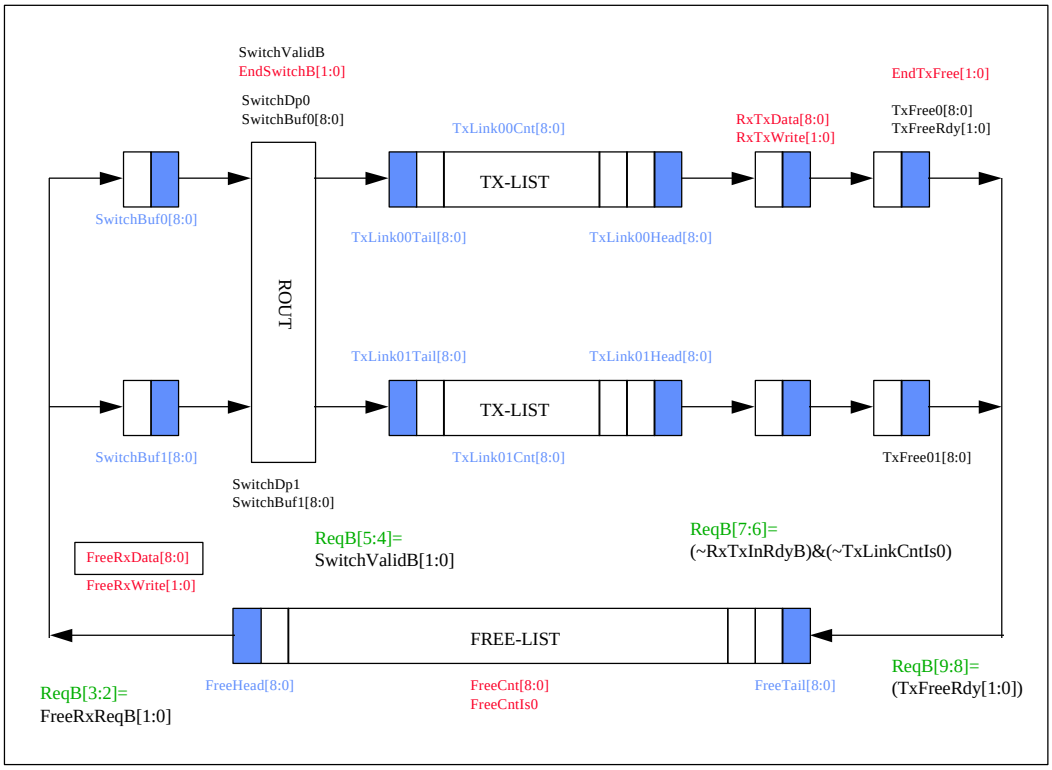


Fig. 15

2. The pool of free buffer ID will be organized as a linked list by buffer manager itself. Like the ring buffer, The buffer manager maintains two pointers for the head ID and the tail ID of the Free-List and the other free buffer IDs are linked one by one between them.

3. While the FreeRxReqB is issued from the rx_interface, the buffer ID which the head pointer points to will be assigned to the rx_interface. FreeRxData and FreeRxWrite represent the buffer ID data and the write signal.

4. While the Filtering/Forwarding process is completed, the buffer manager releases the buffer ID and appends it to the transmit buffer ID link list. And the tail pointer will jump to the new last one in the buffer ID list.

5. While the RxTxInRdyB is issued from the tx_interface, and at that time the respective Tx-List is not empty, the head buffer ID of the Tx-List will be assigned to the tx_interface for transmit. The head pointer will point to the next one.

6. While the packet has finished transmit operation, its associated buffer ID is then marked available and have to be recycled to the tail of the Free-List. If the TxFreeRdy request which is issued from the tx_interface is granted, the operation to free the buffer ID is really completed.

Packet Buffer Congestion Control

The buffer manager implements the congestion control function in half-duplex operation. For each port, the alarm signal raises while the number of the buffer ID reaches the pre-set threshold value. Meanwhile, if a packet arrives at this moment, the TxDMA generates a JAM packet to collide with the incoming packet. This is known as back pressure flow control. This action does not only prevent the buffer overflow but also avoid the packet loss.

W89C871F has two ways to perform back pressure function if enabled by CSB[2]. The first way is enabled by pulling CSB[3] high. In this case, W89C871F will only issue JAM pattern for the packet to be forwarded. It will not take any action for those packets with local destination MAC address. The second way is enabled by floating CSB[3]. In this case, W89C871F will back-pressure each packet received, no matter what they are local or remote packets.

In the very busy network traffic environments, when both 10M segment and 100M segment each other issue packets with wire speed at the same time, the buffer would be full and W89C871F may continuously issue more than 60 times for 100M and 30 times for 10M, respectively. If this happens, then the port of W89C871F connected to that segment will be partitioned, and if the situation lasts, the channel between two segments will be blocked.

To solve this potential issue, W89C871F implements a discontinuous back-pressure function mode capable of being enabled by RPT[7] pin. If enabled, it will continuously back-pressure at most 55 times for 100M port and 23 times respectively and then lost the next coming packet and, again, repeat this algorithm. This keeps the performance between these two different speed network segments.

The maximum pre-set number of the buffer ID depends on each port wire speed : (the first 22 buffer IDs must be reserved for the address table)

(1) for 512K bytes buffer memory configuration

10 Mbps / 10 Mbps : 155 /155

100 Mbps/ 100 Mbps : 155 /155

10 Mbps/100 Mbps : 278/ 32

100 Mbps / 10 Mbps : 32 /278

(2) for 256K bytes buffer memory configuration

10 Mbps / 10 Mbps : 69 /69

100 Mbps/ 100 Mbps : 69/69

10 Mbps/100 Mbps : 122/16

100 Mbps / 10 Mbps : 16/122

To improve the throughput between 10M and 100M segments, no matter what duplex mode they are, W89C871F implements a minimum number of buffers for both MII ports receiving to keep the path with heavy traffic from being blocked.

THE FUNCTIONS OF MEDIA ACCESS CONTROLLER(MAC)

The MAC function of W89C871F consists of two sub functions which complies with the specification of the IEEE 802.3/u section 4.. One is the MAC receive function and the other is the MAC transmit function. Each MAC can transmit and receive simultaneously for its implementing two separated receive/transmit FIFO, and perform the most Ethernet functions such as transmit, receive and error handling operation etc.

Network media speed selection function

The MAC module is specifically designed to perform both 100BASE and 10BASE Ethernet. The speed of transmit and receive depends on the input clock of TXCLK and RXCLK on MII bus,. The MAC block of W89C871F transmits or receives the nibble byte data with the same clock speed of TXCLK and RXCLK respectively. When physical layer device(PHY) changes the speed, W89C871F is able to detect the change and follows it.

In 100BASE mode, The frequency of TXCLK and RXCLK is 25MHz; however, in 10BASE mode, it is 2.5 MHz. The frequency of RXCLK and TXCLK is determined by the physical layer device(PHY) which supports both 10BASE and 100BASE bit rates.

The Receive functions of MAC

The MAC receive functions specified by the IEEE802.3 includes the address recognition function, frame check sequence validation, frame disassembly, framing and collision filtering. However, the address recognition is not implemented in the MAC module of W89C871F, since this function is not necessary for the MAC of the switch. The CRC function is implemented in RXDMA module, but not in MACRX module. The MAC receive portion (MACRX) receives all the packet with both the preamble and the SFD. MACRX does not check the CRC and the destination address of the input packet. However, the input packet with length less than 9 bytes is filtered and the odd nibble at the end of the input packet is also filtered for data byte alignment device. The MACRX operates independently with the MACTX module.

Receiving synchronization control

The receiving synchronization control generates control signals to latch the nibble byte data from MII bus. This operation synchronizes the timing of control and data between PHY and MAC in W89C871F and prevents the data misalignment etc. The receiving clock RXCLK from the MII is synchronized with the transmit clock TXCLK in the MAC transmit module. These clock and control signals, included TXCLK, RXCLK, RXD[0:3] and TXD[0:3] are used by the received data byte aligner for packing the nibble byte data into the byte-formed data.

Received data byte aligner

The Received data byte aligner is used to merge two nibble byte data as a byte data and is shown in Fig. 16. The MAC Receive module(MACRX) will, finally, do the de-

framing to strip the preamble and the SFD before sending the receive data to RXDMA module. The nibble data received from the MII bus is aligned and packed to a byte data by the data byte aligner and then send to RXDMA module. The data in RXDMA module does not includes preamble bits and SFD. The aligner outputs the data RXDATA[7:0], control signal RXCRS and the WRITE for RXDMA operation. RXCRS is the receiving carrier sense signal and WRITE is the clock to latch the RXDATA[7:0] in the RXDMA operation.

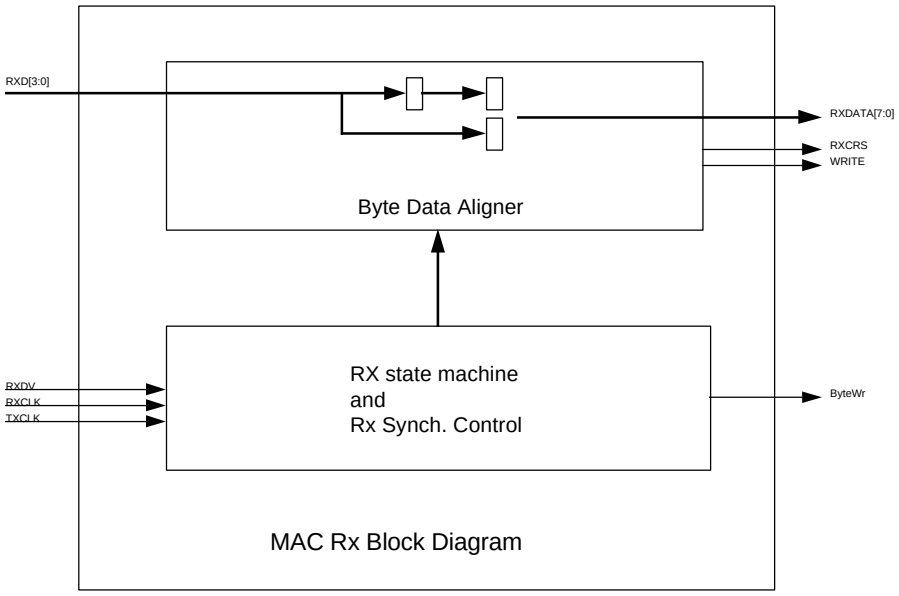


Fig.16

The Transmit Functions of MAC

In Fig 17., MAC transmit function(MACTX) performs the CSMA/CD protocol and transmit data etc., and converts the byte format data from TXDMA device into nibble format and put it on the MII bus. MACTX does not append extra more data except padding the preamble bits and the SFD to the exact 64 bits long.

Defer and back off

The MACTX also perform many other transmission functions specified by the IEEE802.3 including the inter-frame spacing function, collision detection, collision enforcement, collision backoff and re-transmission etc,. The collision backoff delay is an integer multiple of slot time, defined as 512 bit times. The number of slot times to delay between the current attempt to the next attempt is determined by a uniformly distributed random integer specified by the IEEE802.3. The integer, r, is specified as the following

$0 \le r \le 2^k$ where k = min.(n, 10)

MAC has to defer when ready to transmit a frame because the carrier sense signal presented before MAC gets the grant to acquire the network media. When others MAC finishes the transmit and slips 96 bits inter-frame gap time, MAC of W89C871F will transmit the data immediately.

W89C871F also supports an optional function of high prioritized transmit. This helps release buffer from congestion in the case with different speed segments when RPT[6] is pulled high by a 4.7k ohms resistor. In different speed case, this may happens frequently. For releasing the buffer congestion, W89C871F supports such a function to promote network performance, especially in the case that back pressure is enabled.

Duplex mode control

The duplex mode is determined by PHY. W89C871F gets the duplex mode status once PHY has completed the negotiation with others PHY device.

In half duplex mode, Only transmit or receive operation can be performed at a time. In 100M with this mode, MII collision signal, COL, is valid for the MAC module. While MAC is transmitting a packet, an active signal on COL is treated as a transmit collision event occurred on the media. However, in 10M mode, the active COL signal acts as a SQE test signal, not a collision event, in the time duration from the 10th bit to the 16th bit after the packet is transmitted. In 100M mode, this time frame is still treated as a part of collision time.

MII carrier sense signal, CRS, is also a valid signal when the MAC module is set to be half duplex mode. The active signal on CRS will act as a loopback carrier sense signal when the MAC is transmitting a packet. Usually, there should not be carrier sense lost during transmitting.

In full duplex mode, MAC performs the simultaneous transmit and receive operation. In this case, COL and CRS on MII bus are ignored by MAC. There is no collision event, SQE lost and carrier sense lost in the full duplex operation mode. Any activity on COL and CRS will not affect the operation of MAC module.

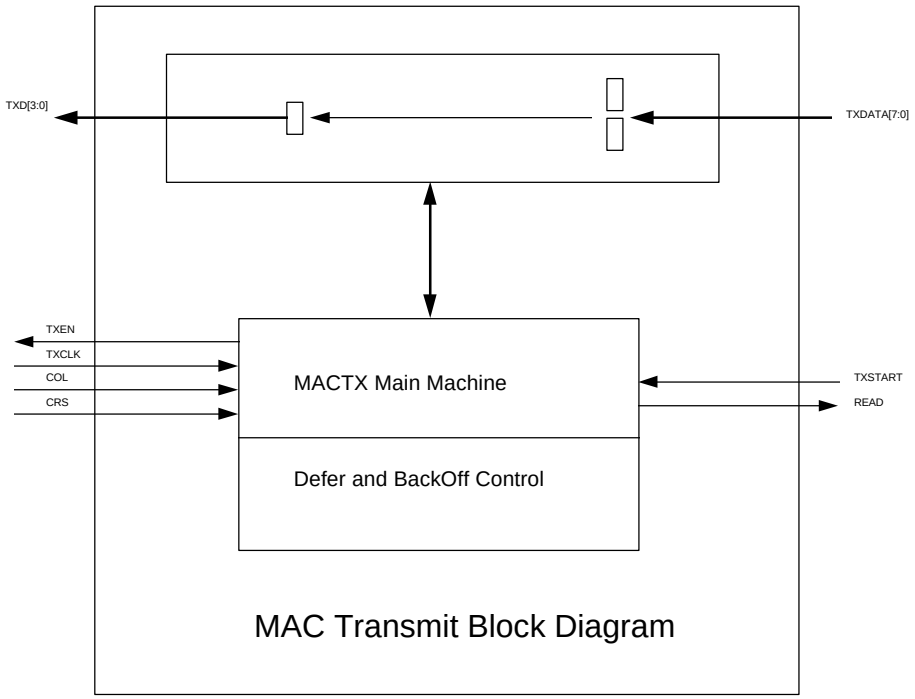


Fig. 17

DMA Functions

The DMA function of W89C871F consists of two sub functions. One is the receive DMA function and the other is the transmit DMA function. DMA function is used to handle the data transfer between the buffer memory and each FIFO receive/transmit port. In fig. 18 and 20, it is clear to show the DMA path.

Receive DMA function

RXDMA receives the packet data from MAC module and packs these byte-aligned data into word-aligned data because the data width of the buffer memory is 16 bits. The RXDMA also generates control signals for the word-aligned data reception and the handshaking with buffer manager. The detail statements are shown in the following paragraph.

Receiving data path

There is an one-stage 16 bits data latch for aligning the byte format data as word format data. The clock for latching the aligned buffer is synchronized with the WRITE pulse of the MAC module, shown in Fig. 18. The aligned 16 bits word data will be written into a 16 bits data FIFO. The write pulse is controlled by the RxSyncCtrl block in RXDMA module. During the data reception, the write pulse is also synchronized with the WRITE pulse of the MAC module.

The FIFO issues a data read request to the memory access control module for storing the received data into the buffer memory. The read pulse for this FIFO is generated by the memory access control module and is synchronized with the global system clock but not the clock of the MAC module. When a packet is received, the RXSyncCtrl block will write a 16 bits packet header information into the FIFO. The packet header is the internal information, included 13 bits received byte count, 1 bits receiving port ID, 1 bits routed port ID and 1 bits received status. It is appended by the received packet data and stores in the buffer memory.

Receiving status control

The receiving status include CRC status, long packet status, runt packet status and the normal received status. In W89C871F, there is a CRC check circuit for performing the CRC check, a packet length check circuit for performing the check of the runt packet or long packet which excesses 1518 bytes. If VLAN function is enabled, the length of packet with 1522 bytes is allowed.

Receiving FIFO overflow detection

In DXDMA module, when the buffer memory is full or FIFO full being unable to transfer its content to the buffer memory, an FIFO overflow will occur. The received packet will be dropped when this error happens.

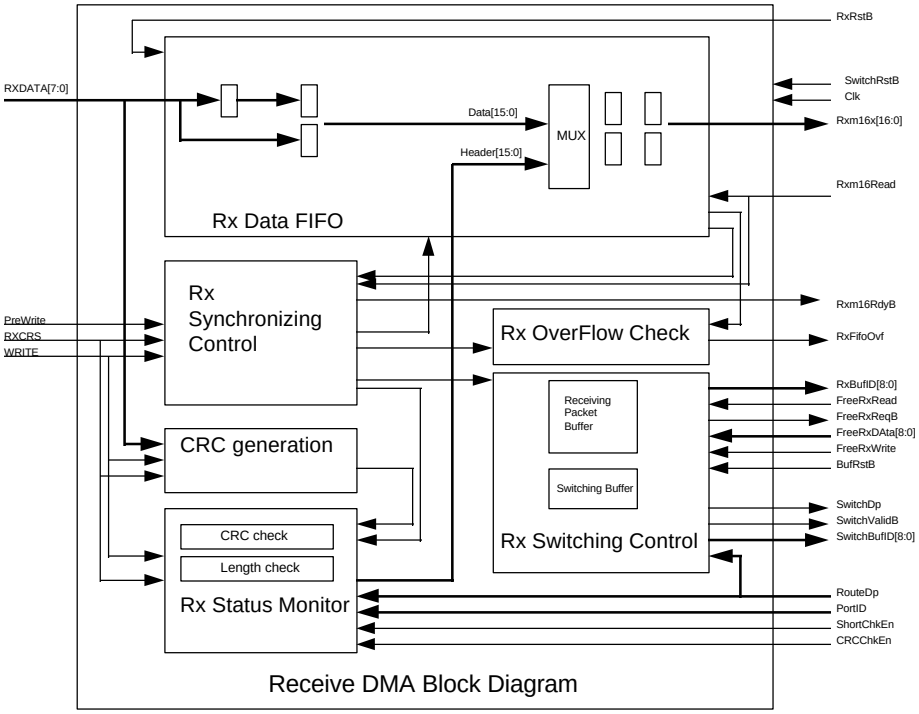
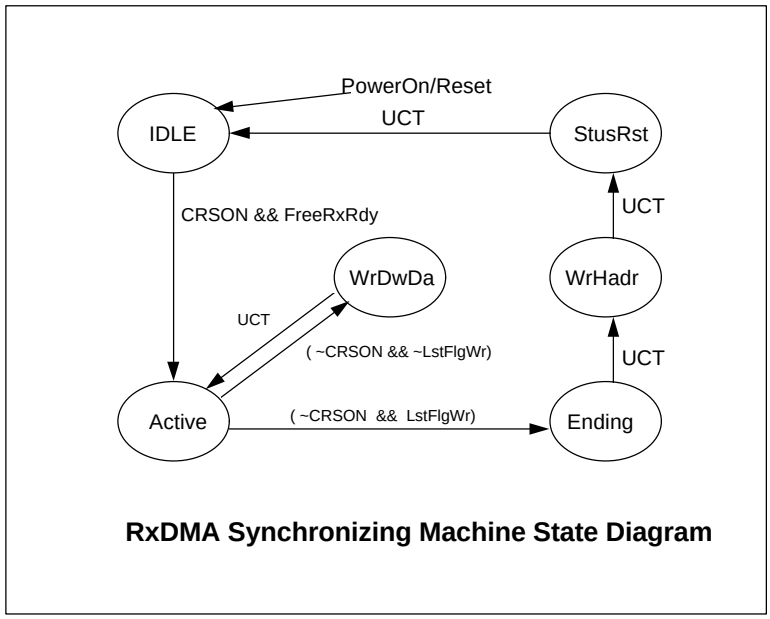


Fig. 18

Receiving synchronization control

Due to the operating clock of the MAC module and the switching core(including DMA, the packet_routing, etc.) is different. Between pre-packing buffer and the FIFO of MAC, there is an asynchronous issue existed. The RxSyncCtrl block performs the synchronization for the data FIFO write in Fig. 18. There are two types of data FIFO write, one is the received word data write and the other is the packet header write. The state diagram of the synchronization control block is shown in the figure 19. The state machine starts when a packet is coming and there is an available packet buffer ID which is able to allocate a block of memory with full packet size. The packet header will be written when the CRS is inactive at the receive operation. The packet header includes 13 bits received byte count, 1 bit routed port ID, 1 bit source port ID and 1 bit receive status.



RxDMA Synchronizing Machine State Diagram

Fig. 19

Receiving switching control

The receiving switching control performs the receiving buffer memory control and the switching status buffering. The receiving buffer is managed by the buffer manager. Each RXDMA allocate two packet buffer IDs for next coming packet. If the current receiving packet has an error occurred, the receiving packet buffer ID for the current receiving packet can be reused and does not have to return it back to the buffer manager.

The switching status includes the routed port ID and the receiving buffer ID used by the current received packet. If there is any switching status error occurred, the received packet will be discarded.

Transmit DMA function

The TXDMA performs the function to fetch the data stored in the buffer memory according to the buffer ID in the buffer id link list and to re-align the word format data into a byte format data. The TXDMA also controls the data transmit to the MAC module and the packet buffer ID recycle.

The block diagram of the TXDMA function is shown as the following figure.

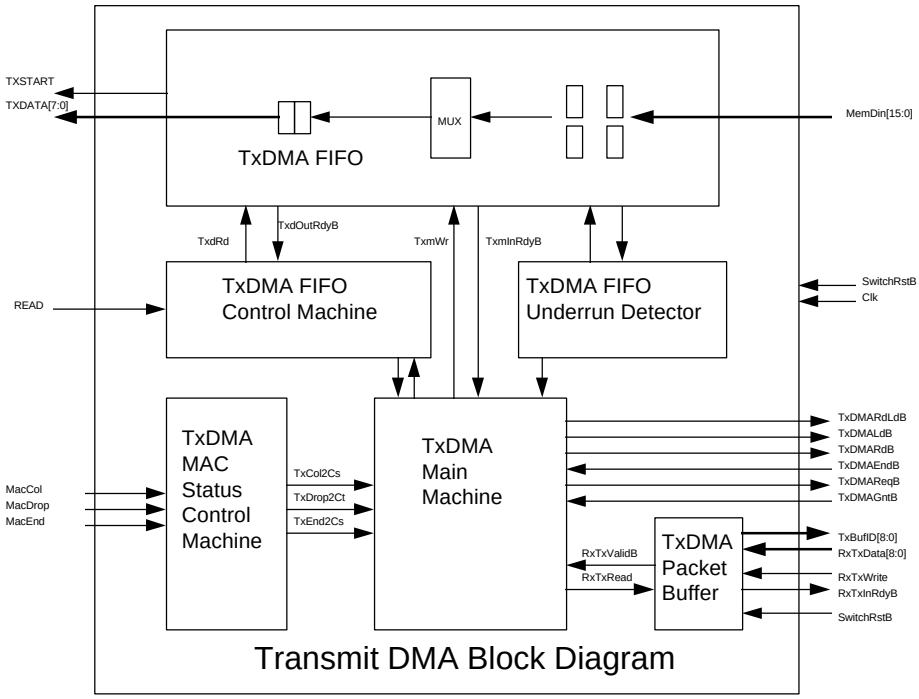


Fig. 20

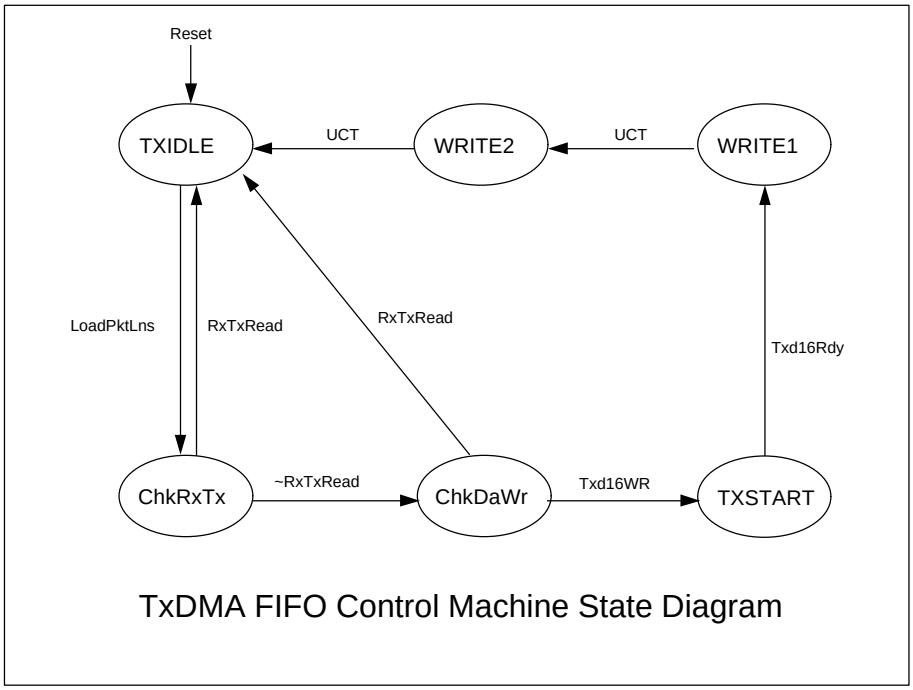
Transmit data path

There are two 8 bits data latcher and two 16 bits data FIFO used for latching and buffering the data to be transmitted. The data fetched from the buffer memory is controlled by TXDMA state machine, and is first latched into a four-stage with 64-bit long FIFO and then written into two stage FIFO with 8-bit long each. The data written to the 8-bit long FIFO is accomplished by both TXDMA FIFO control machine and MAC modules, and next, transferred to the transmit FIFO by MAC. The state diagram of TXDMA FIFO control machine is shown as the following diagram.

TXDMA FIFO control machine will not write data into the two stages byte aligned FIFO until the word data is ready in the two stages 16 bits FIFO. FIFO control state machine will be active when it detects that TXDMA main machine is entering the Load header(LDHDR) state. If the transmitted packet is dropped due to the packet header

error, FIFO control machine will return to the idle state without writing any data into FIFO. It will write, however, first two bytes data into the FIFO by TXDMA when the transmitted packet is good. The remain bytes of the transmitted packet will be written into the FIFO with the READ signal from MAC module.

MAC module will start to transmit the preamble bits when FIFO control machine detects the first word data has been written into the FIFO. It is guaranteed that the packet data will be ready in the FIFO before the preamble is transmitted.



TxDMA FIFO Control Machine State Diagram

Fig. 21

Transmit FIFO under flow detection

The TXDMA builds a FIFO under flow detection circuit. The transmitted packet will be dropped when an under-flow occurred in transmit FIFO. At this time, the buffer ID is not free.

MAC status monitoring

The state diagram of TXDMA MAC status control machine is shown as following diagram. It shows how the MAC status is monitored and handled.

TXDMA MAC status control machine monitors the MAC module state. The control signal Transmit End, Transmit Collision or Transmit Abort is asynchronized with the system clock. The TXDMA main machine, however, is driven by the system clock. The TXDMA MAC status control machine performs synchronization for the signals generated by the MAC module. These re-synchronized signals will be, then, used as inputs of the TXDMA main machine. The MAC status machine also monitors if the output packet blocked status and the FIFO underflow event are consistent with the TXDMA main machine and the TXDMA FIFO control machine.

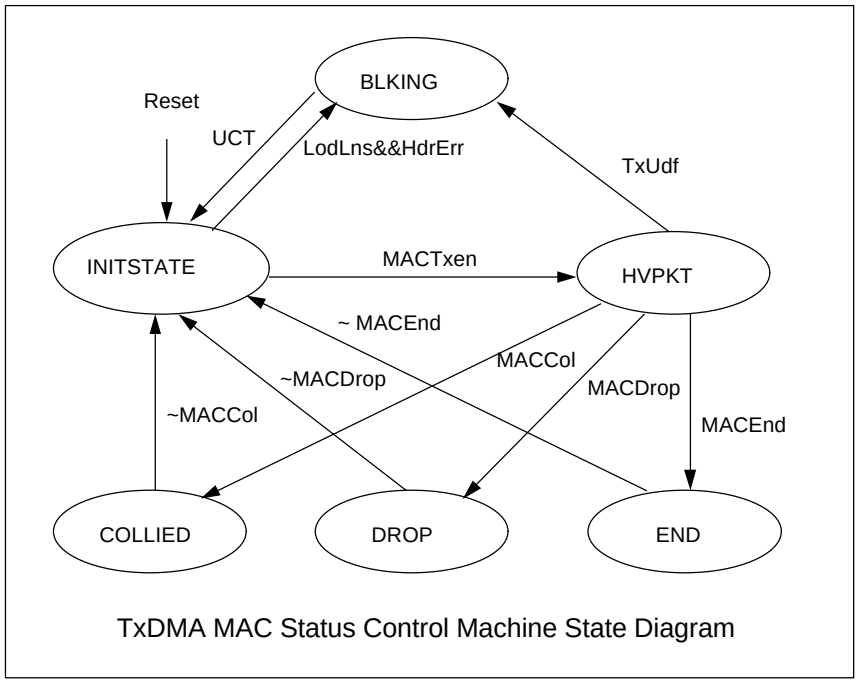


Fig. 22

Transmit packet buffer FIFO

The packet to be transmitted is stored in the buffer memory at the beginning. The buffer manager writes the buffer ID of the packet, in which the associated packet is ready to be transmitted by the TXDMA, into the transmit packet buffer FIFO. The TXDMA main machine will start when it detects a packet buffer ID is written into the buffer FIFO. The buffer manager will read back the packet buffer ID when the packet is transmitted.

TXDMA main machine

TXDMA main machine controls the data fetch function for the operation of the packet transmitted. The TXDMA main machine will be active when it detectes that a packet is to be transmitted. The data ready signal of the FIFO of the packet buffer ID will be active when the buffer manager writes a packet buffer ID into the FIFO. The main machine, then, first fetches the packet header.

If the header is with some kinds of error or the output packet is blocked by the configuration setting of the VLAN, the packet will be dropped. Otherwise, the main machine will continue to fetch the next packet.

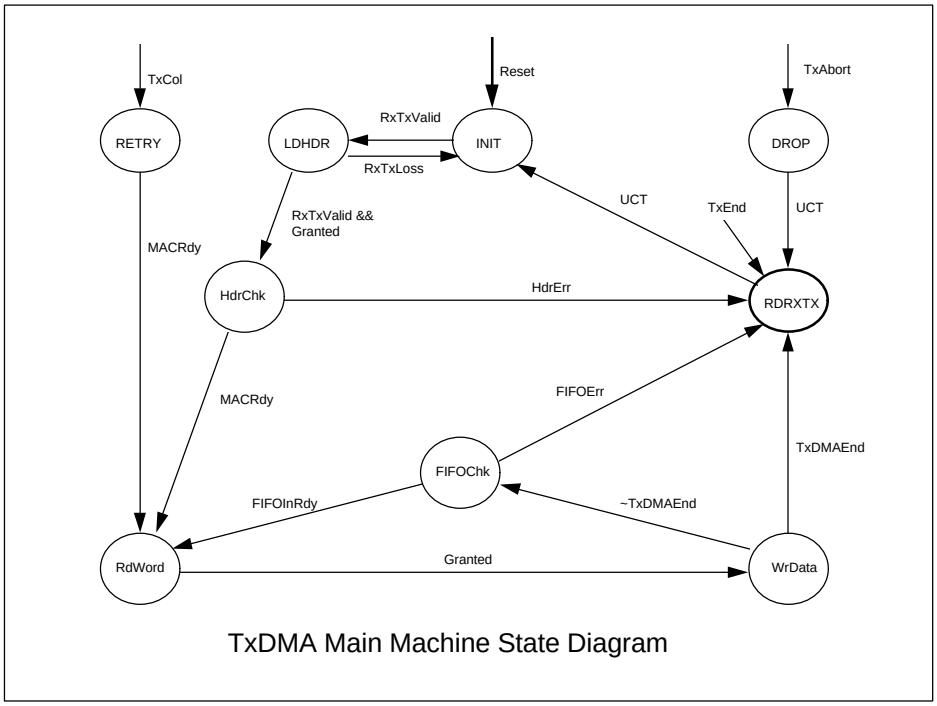
The TXDMA main machine checks the following status to decide whether to fetch next long word data, to wait for the grant to fetch data, to re-fetch the header information or to return to the idle state. These status are Transmit FIFO underflow status, Transmit FIFO Input Ready status and Transmit End status.

When it is already granted to access the external memory by the memory access arbiter, TXDMA main machine fetches the next long word data. In case of Transmit Aborted, Transmit End , Packet Blocked or Transmit FIFO underflow happens, the main machine will enter RDRXTX state and inform the buffer manager to read back the packet

buffer ID. However, the main machine will try to re-fetch the data from the head of the packet in case of re-transmission.

In any case, the main machine will not return to INIT state before the packet buffer ID is read back by the buffer manager. A SwhEnd signal is used to synchronize the TXDMA main machine and the buffer manager.

The block diagram of the TXDMA main machine is shown as the following diagram.



TxDMA Main Machine State Diagram

Fig. 23

MII Management

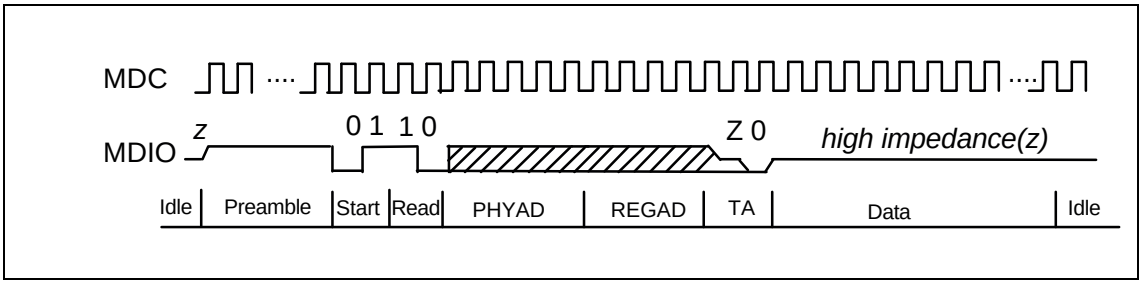
The W89C871F provides a set of configuration registers, accessible through the MDC and MDIO pins on the MII serial management bus. The FastMPR can thus be managed through the MDC and MDIO pins. For the FastMPR to be configured by programming these registers or setting hardware jumpers, an external serial command generator is needed to generate an MII management frame format command (shown in the following table) to drive MDC with a minimum 40 ns clock period so that the data train is latched on the MDIO. The typical read and write timing of the serial interface is shown in the diagram below.

	MII MANAGEMENT PROTOCOL							
	PRE	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1... 1	01	10	AAAAA	RRRRR	Z0	16 bits	Z
Write	1... 1	01	01	AAAAA	RRRRR	10	16 bits	Z

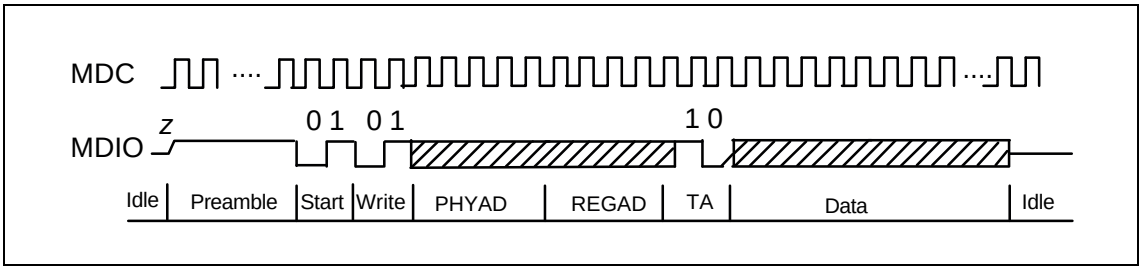
Management Frame Format Table

Note:
PRE: Preamble; ST: Start of Frame; OP: Operation code; PHYAD: PHY address; REGAD: register address.
TA: Turnaround.

TYPICAL MDIO/MDC READ CYCLE



TYPICAL MDIO/MDC WRITE CYCLE



LED Displaying Interface

In W89C871F, LED display interface supports comprehensive network status reports along with the corresponding strobe signals. The following table describes the content shown by LED display selected by the strobe signals.

	RXBW_STB	TXBW_STB	RXFLT_STB	TXCOL_STB	MISC_STB
RPT[0]	RXBW_RPT[0]	TXBW _RPT[0]	RXFLT_RPT[0]	TXCOL_RPT[0]	BFFUL_RPT
RPT[1]	RXBW_RPT[1]	TXBW_RPT[1]	RXFLT_RPT[1]	TXCOL_RPT[1]	TXACT_RPT
RPT[2]	RXBW_RPT[2]	TXBW_RPT[2]	RXFLT_RPT[2]	TXCOL_RPT[2]	RXACT_RPT
RPT[3]	RXBW_RPT[3]	TXBW_RPT[3]	RXFLT_RPT[3]	TXCOL_RPT[3]	SPEED_RPT
RPT[4]	RXBW_RPT[4]	TXBW_RPT[4]	RXFLT_RPT[4]	TXCOL_RPT[4]	UPLX_RPT
RPT[5]	RXBW_RPT[5]	TXBW_RPT[5]	RXFLT_RPT[5]	TXCOL_RPT[5]	COL_RPT
RPT[6]	RXBW_RPT[6]	TXBW_RPT[6]	RXFLT_RPT[6]	TXCOL_RPT[6]	N.A.
RPT[7]	RXBW_RPT[7]	TXBW_RPT[7]	RXFLT_RPT[7]	TXCOL_RPT[7]	N.A.

The following diagram shows the timing of each display mode and the corresponded strobe signal.

The LED displaying data include the

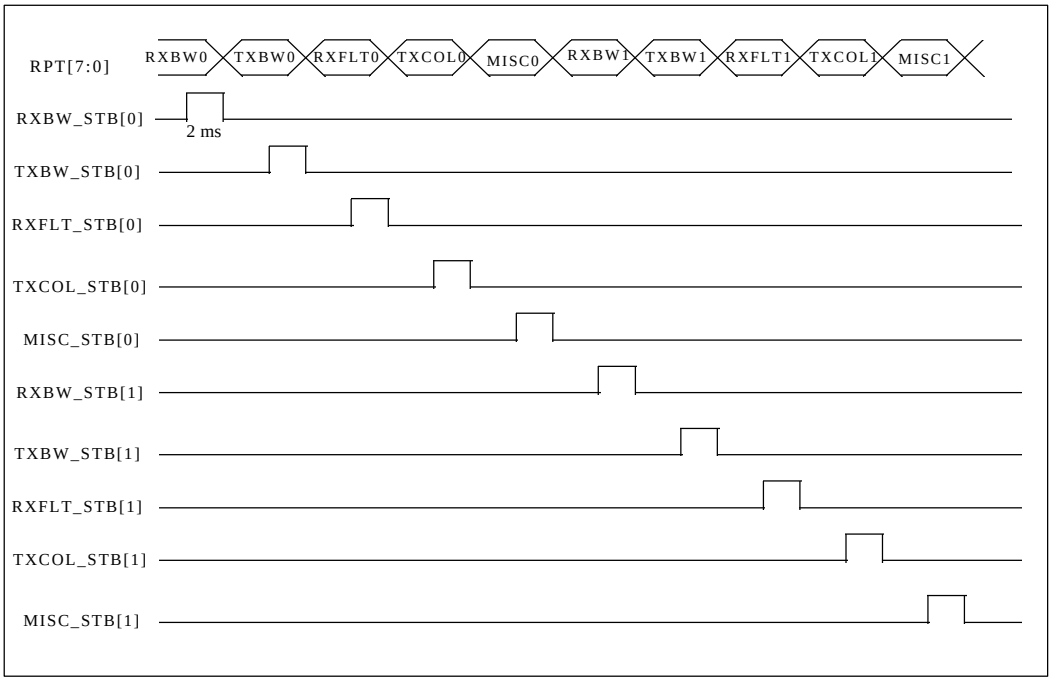
1) Bandwidth percentage of Receiving Activity (%),

2) Bandwidth percentage of Transmitting Activity (%),

3) Bandwidth percentage of Receiving Filter (%),

4) Bandwidth percentage of Transmitting Collision (%)

5) Miscellaneous report.



The displaying data shows the status of each port. All of the status can be latched by individual strobe signal.

For Receiving Bandwidth, Transmitting Bandwidth, Receiving Filter, and Transmitting Collision displaying, the mapping between the data of RPT[7:0] and the activity ratio is shown as the table below.

	>1%	>5%	>10%	>20%	>35%	>50%	>70%	>90%
RPT[0]	0	0	0	0	0	0	0	0
RPT[1]	1	0	0	0	0	0	0	0
RPT[2]	1	1	0	0	0	0	0	0
RPT[3]	1	1	1	0	0	0	0	0
RPT[4]	1	1	1	1	0	0	0	0
RPT[5]	1	1	1	1	1	0	0	0
RPT[6]	1	1	1	1	1	1	0	0
RPT[7]	1	1	1	1	1	1	1	0

Bandwidth percentage of Receiving Activity (%)

This statistics report displays the percentage of each port network utilization compared to the wire speed. For 100 Mbps configuration, we select a calculation window 80 ms, and the $8*10^6$ bits will cause the 100% bandwidth utilization during the calculation window. A receiving bit counter which is enabled by RX_DV is implemented to learn this. The Receiving Bandwidth (%) can be calculated by dividing the $8*10^6$ with the value of the receiving bit counter whenever the calculation window is expired.

Bandwidth percentage of Transmitting Activity (%)

In a similar way, by implementing the transmitting bit counter which is enabled by TX_EN, the Transmitting Bandwidth (%) can be calculated by dividing the $8*10^6$ with the value of the transmitting bit counter whenever the calculation window is expired. The statistic report represents the forwarding bandwidth for each port.

Bandwidth percentage of Receiving Filter (%)

The statistic report indicates the complementary result of the Transmitting Bandwidth (%). For example, if the 35% Transmitting Bandwidth is represented, therefore the 65% Receiving Filter is represented during the calculation window.

Bandwidth percentage of Transmitting Collision (%)

For each port, the statistics report displays the percentage of the collision bandwidth for each port compared to the overall network bandwidth. A collision bit counter which is enabled by COL is implemented. The calculation is done by dividing the $8*10^6$ with the value of collision bit counter whenever the calculation window is expired.

Miscellaneous Report

Buffer Full Report

The buffer full reports are derived from the flow-control alarm signals of the Buffer Manager, which indicate the received packet buffer has reached the threshold value. While the port receive one more packet, the back pressure event occurs.

Transmitting Active Report

The transmitting active reports are derived from the TX_EN signals of the MII interface. Whenever the transmitting packets traverse the ports, the LEDs will blinking light.

Receiving Active Report

The receiving active reports are derived from the RX_DV signals of the MII interface. Whenever the receiving packets traverse the ports, the LEDs will blinking light.

Speed Report

The speed reports are derived from the result of the speed configuration. While the auto-negotiation or the hardware configuration is completed, the reports keep light on or off steadily. Output high means the 10 Mbps speed is configured. (Consistent with N.S. PHYceiver)

Duplex Report

The reports are similar to the speed reports. While the auto-negotiation or the hardware configuration is completed, the reports keep light on or off steadily. Output high means the half duplex is configured. . (Consistent with N.S. PHYceiver)

Collision Report

The collision reports are derived from the COL signals of the MII interface. While the COL signals raise, the LEDs will light on.

External Manager Interface

The External manager interface is implemented only for the test mode of the W89C871F. There are some control registers built in the W89C871F to perform the testing functions. In order to monitor the operation of the W89C871F, the external manager interface provides the channel to access and configure the internal registers. The access procedure for registers follows the MII management protocol defined in IEEE 802.3u.

The following table lists the internal registers and their corresponding address.

Addr.	Symbol	Bw	r/w	Description
0	CTRLR	16	rw	Control register
1	CFGSR	16	ro	Configuration status register
2	EMACR	16	rw	External memory access command register
3	BTACR	16	rw*	Buffer table access command register
4	WDIER	16	rw	Watch dog timer interrupt enable register
5	WDISR	16	ro	Watch dog timer interrupt status register
6	LCTSR	16	ro	Long counter test signature register
7	INTSR	16	ro	Interrupt status register
8	INTER	16	rw	Interrupt enable register
9	FREHR	16	ro	Free head register
A	FRETR	16	ro	Free tail register
B	FRECR	16	ro	Free buffer counter register

C	MEMDR	16	rw	Memory direct access data register
D	MEMAR	16	rw	Memory direct access address register
E	AGTMR	16	rw	Age time register
F	MACCR	16	rw	MAC control register
10	TX0HR	16	ro	Port0 Tx buffer head register
11	TX1HR	16	ro	Port1 Tx buffer head register
12	TX0TR	16	ro	Port0 Tx buffer tail register
13	TX1TR	16	ro	Port1 Tx buffer tail register
14	TX0CR	16	ro	Port0 Tx buffer counter register
15	TX1CR	16	ro	Port1 Tx buffer counter register
16	TXMXR	16	rw**	Tx-list maximum threshold register

Note1* : The command of BTACR is valid only when CTRLR[4] = 1.

Note2**: The TXMXR can be written only when CTRLR[5] = 1, the written value is kept until the CTRLR[5] = 0.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	PARAMETER	MIN	MAX	UNIT
TA	Operating Temperature	0	70	°C
TS	Storage Temperature	-55	150	°C
VDD	Supply Voltage	-0.5	7.0	V
VIN	Input Voltage	VSS-0.5	VDD+0.5	V
VOUT	Output Voltage	VSS-0.5	VDD+0.5	V
TL	Lead Temperature (Soldering 10 seconds maximum)		250	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Power Supply

(VDD = 4.75V, VSS = 0V, TA = 0° C to 70° C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
IDDI	Power Supply Current (idle)	150	150	mA
IDDT	Power Supply Current (transmit)	250	250	mA

DC Characteristics

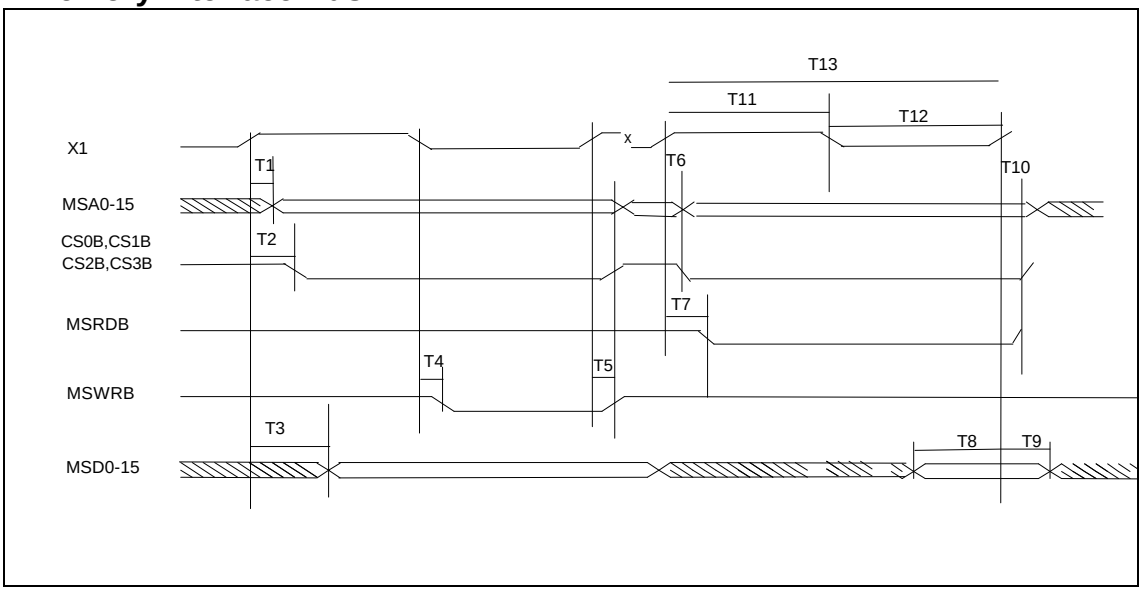
(VDD = 4.75V to 5.25V, VSS = 0V, TA = 0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
VIL	Low Input Voltage	VSS-0.5	0.8	mA
VIH	High Input Voltage	2.0	VDD+0.5	V
VOL	Low Output Voltage (IoL= 4.0mA)		0.4	V
VOH	High Output Voltage (Ioh= -4.0mA)	2.4		V
IIL	Input Leakage Current(Vin=5.25V)		10	μA
IOL	Tristate leakage Current(VDD = 5.25V)		10	μA

AC Characteristics

(VDD = 4.75V to 5.25V, VSS = 0V, TA = 0 °C to 70 °C)

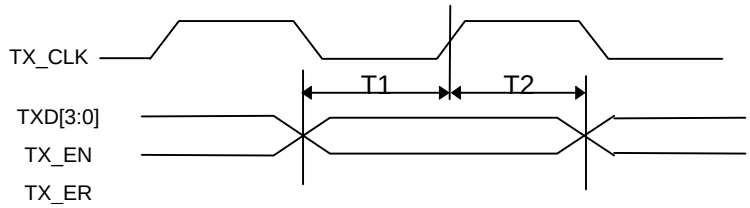
Memory Interface Bus



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	X1 rising to MSA0-15 valid			5	nS
T2	X1 rising to CSB0,1,2,3 valid			5	nS
T3	X1 rising to write data MSD0-15 valid			15	nS
T4	X1 falling to MWRB active low			5	nS
T5	X1 rising to MWRB deassert			5	nS
T6	X1 rising to MSA0-15 and CSB0,1,2,3 valid			5	nS
T7	X1 rising to MRDB active low			15	nS
T8	Read data MSD0-15 set up time to X1 rising			5	nS

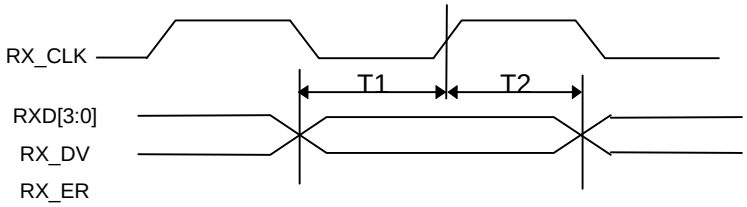
T9	Read data MSD0-15 hold time from X1 rising	5			nS
T10	MRD, MSA0-15 and CSB0,1,2,3 hold time from X1 ringing	5			nS
T11	X1 clock high time (bch)		20		nS
T12	X1 clock low time (bcl)		20		nS
T13	X1 clock cycle time (bcyc)		40		nS

Transmit MII Timing



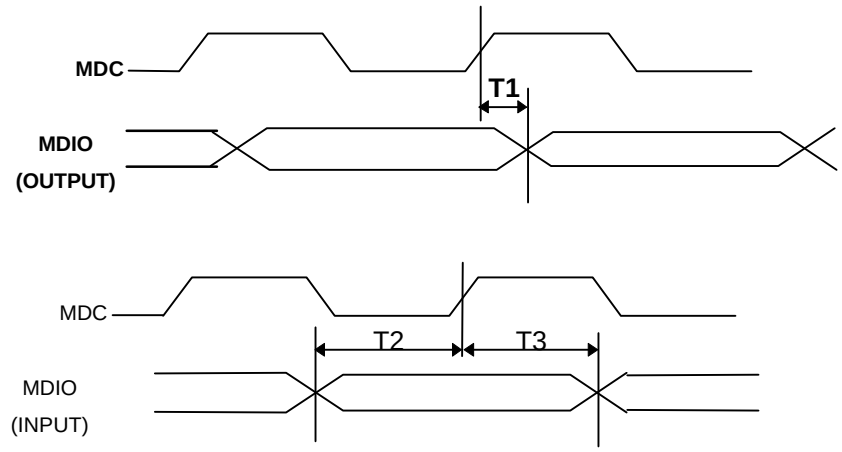
Symbol	Parameters	MIN	TYP	MAX	Unit
T1	TX_CLK to TXD, TX_EN, TX_ER Set_up Time	5			nS
T2	TX_CLK to TXD, TX_EN, TX_ER Hold Time	3			nS

Receive MII Timing



Symbol	Parameters	MIN	TYP	MAX	Unit
T1	RX_CLK to RXD, RX_DV, RX_ER Set_up Time				nS
T2	RX_CLK to RXD, RX_DV, RX_ER Hold Time				nS

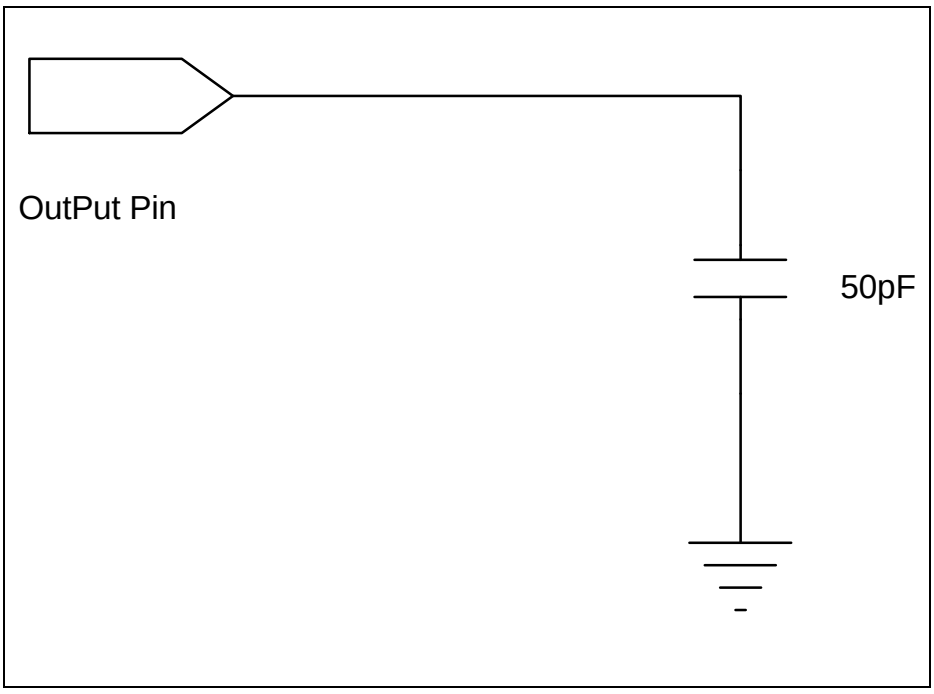
Register Read/Write Timing



Symbol	Parameters	MIN	TYP	MAX	Unit
T1	MDC to MDIO(OUTPUT) Delay Time	0	15	300	nS
T2	MDIO(INPUT) to MDC Set-up Time		25		nS
T3	MDIO(INPUT) to MDC Hold Time		15		nS

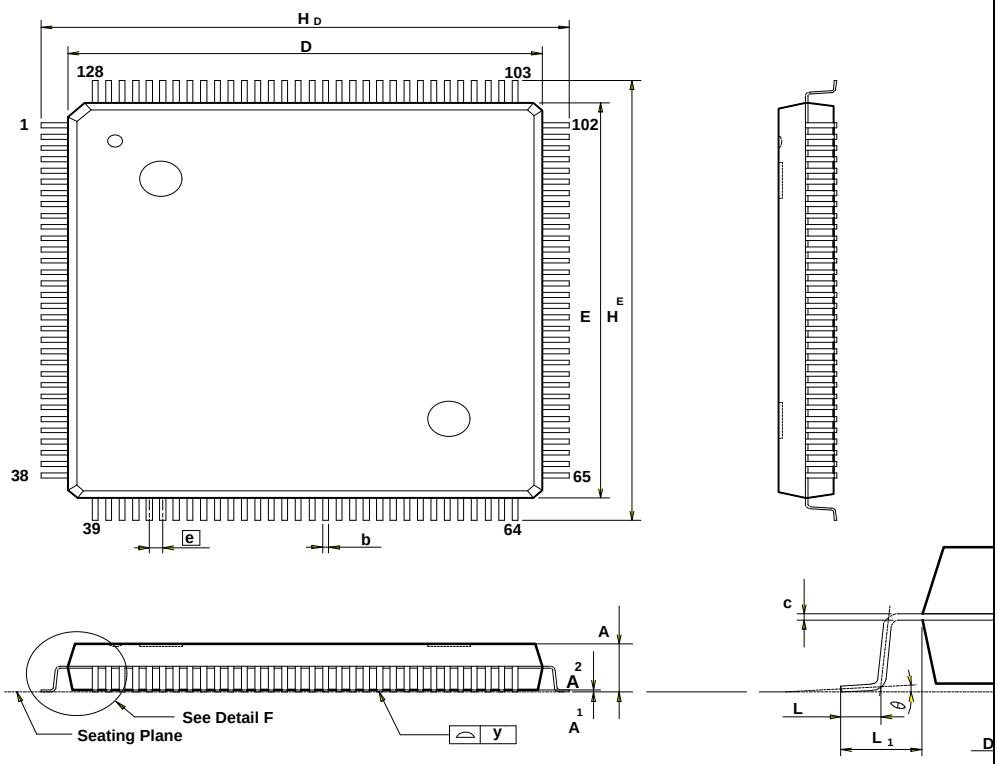
Test Load

Digital Output Switching Test Load



PACKAGE AND DIMENSIONS

(128L QFP 14x20x2.75mm footprint 3.2mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°