Winbond Electronics Corp.

Voice & Melody Controller
(*ViewTalk* ™ Series)

GENERAL DESCRIPTION

The W536XXXP, a member of *ViewTalk*™ family, is a high-performance 4-bit micro-controller (uC) with built-in 8KW uC program. The 4-bit uC core contains dual clock source, 4-bit ALU, two 8-bit timers, one 14 bits divider, maximum 32 pads for input or output, 8 interrupt sources and 8-level nesting for subroutine/interrupt applications. Speech unit, integrated as a single chip with maximum 128 seconds (based on 6.4K sample rate with 5 bits MDPCM) , is capable of expanding to 512 seconds speech addressed by external memory W55XXX with serial bus interface. It can be implemented with Winbond Power Speech using MDPCM algorithm. Melody unit provides dual tone output and can store up to 1k notes. Power reduction mode is also built in to minimize power dissipation. It is ideal for educational toys, remote controllers and other application products which incorporate both melody and speech.

Body	**W536030P**	**W536060P**	**W536090P**	**W536120P**
Voice	30 sec	60 sec	90 sec	120 sec
I/O pad	8I/O, 8I (RA/RB/RC/RD)	8I/O, 8I (RA/RB/RC/RD)	8I/O, 12I, 12O (RA/RB/RC/RD/RE/RF /RG/RH)	8I/O, 12I, 12O (RA/RB/RC/RD/RE/RF /RG/RH)
WDT disable/Enable (Mask Option)	Y	Y	Y	Y
Sub-clock RC/XTAL mode (Mask Option)	Y	Y	Y	Y
Tri-state serial bus (Mask Option)(1)	Y	Y	Y	Y
Cascaded Voice through serial bus (2)	Y	Y	N	Y

(1) Tri-state serial bus mask option can float serial bus while voice playing is no active. Let this mask option is disabled to get minimum power consumption in general.

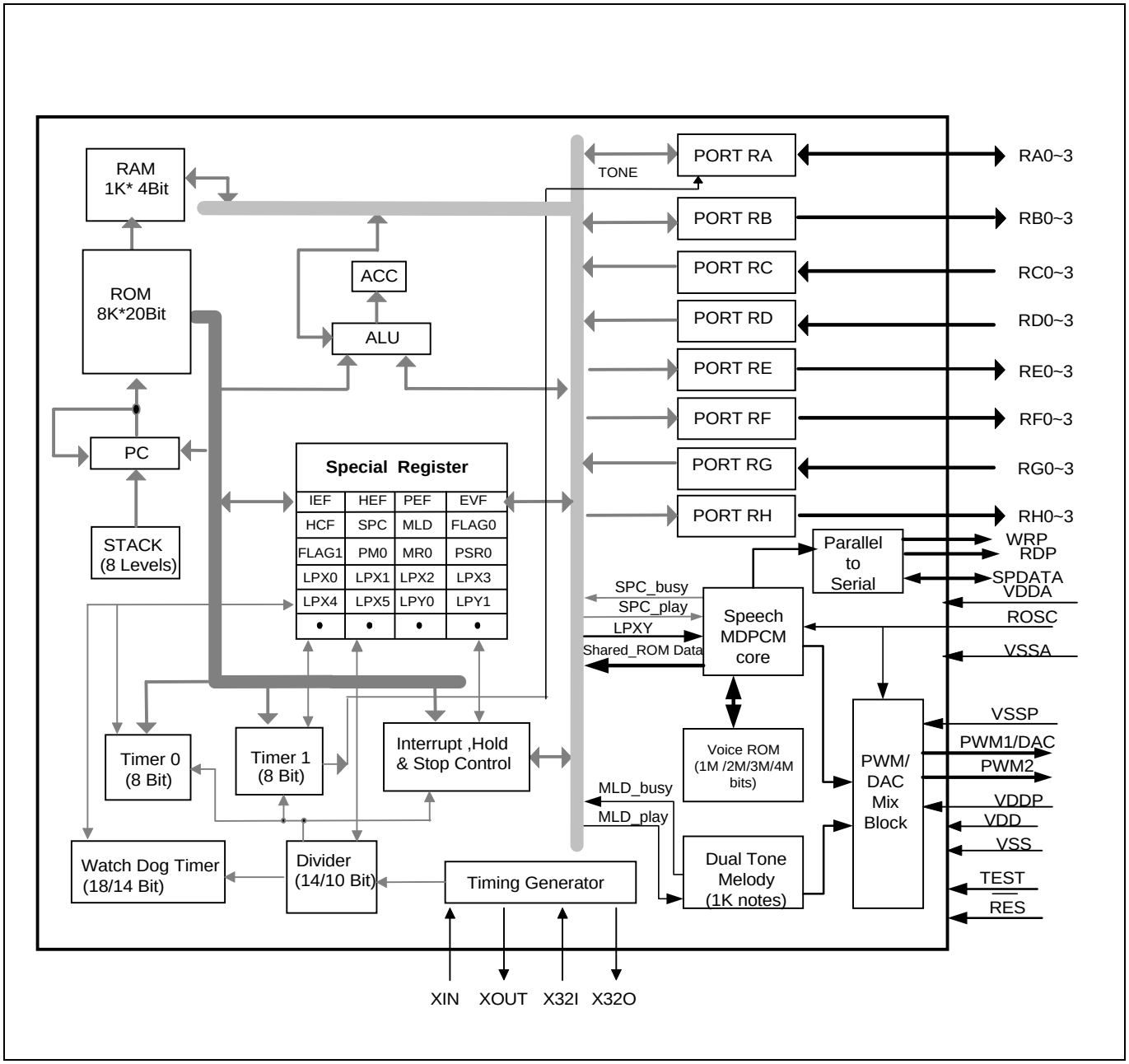
(2) Cascaded Voice ROM user option help to expand voice up to 512 sec through serial bus by W55XXX chip.

FEATURES

- Operating voltage: 2.4 volt ~ 5.5 volt
- Watch dog disabled/enabled by mask option
- Dual clock operating system
  - Main clock with RC/Crystal (400 KHz to 4 MHz)
  - Sub-clock with 32.768 KHz RC/Crystal by mask option
- Memory
  - Program ROM (P-ROM): 8 K × 20 (ROM Bank0)
  - Data RAM (W-RAM): 1K × 4 bit
    (RAM Bank 0 is 512 nibbles from 0:000~0:1FF and 0:380~0:3FF are mapped to special register. RAM Bank F is 512 nibbles from F:200~F:3FF either data RAM or dedicated to script kernel)
- Maximum 32 input/output pads
  - Ports for input only: 12 pads (RC, RD and RG port ; RG for W536090P/120P only)
  - Ports for output only: 12 pads (RE, RF and RH port; RH for W536090P/120P only)
  - Ports for Input/output: 8 pads

- Power-down mode
  - Hold mode (except for 32kHz oscillator)
  - Stop mode (including 32kHz oscillator and release by RD or RC port)
- Eight types of interrupts
  - Five internal interrupts (Divider, Timer 0, Timer 1, Speech, Melody)
  - Three external interrupts (Port RC, RD, RA)
- One built-in 14-bit clock frequency divider circuit
- Two built-in 8-bit programmable countdown timers
  - Timer 0: one of two clock sources (FOSC/4 or FOSC/1024) can be selected
  - Timer 1: built-in auto-reload function includes internal timer, external event counter from RC.0
- Built-in 18/14-bit watchdog timer for system reset.
- Powerful instruction sets.
- 8-level subroutine (including interrupt) nesting
- Speech function
  - Provided 1M / 2M/ 3M/ 4M bits Voice ROM for W536030P/060P/090P/120P based on 5 bits MDPCM algorithm
  - Voice ROM (V-ROM) available for uC data.
  - Maximum 8*256 Label/Interrupt vector (voice section number) available
  - Provide two types of speech busy flag to either each GO or each trigger
  - Maximum up to 16M bits speech address capability interface with external memory W55XXX through serial bus.
- Melody function
  - Provide 1K notes (22bits/note) dedicated melody ROM
  - Provide two types of melody busy flag to uC either each note or each song
  - Provide 6 kinds of beat, 16 kinds of tempo, and pitch range from G3# to C7
  - Tremolo, triple frequency and 3 kinds of percussion available
  - Maximum 31 songs available
- Can mix speech with melody
- Multi-engine controller
- Direct driving speaker/buzzer or DAC output
- Chip On Board available

BLOCK DIAGRAM



PAD DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN/RXIN	I	Input pad for main clock oscillator. It can be connected to crystal when crystal mode is selected (SCR0.2=1), otherwise connect a resistor to VDD to generate main system clock while RC mode is selected (SCR0.2=0 and default). Oscillator can be enabled or stopped by set SCR0.1 to 1 or clear to 0 separately. External capacitor connects to start oscillation while crystal mode
XOUT	O	Output pad for oscillator which is connected to another crystal pad when in crystal mode. External capacitor connects to start oscillation when in crystal mode.
X32I/RSUB1	I	32.768 KHz crystal input pad or external resistor node 1 **by mask option**. External 15~20pF capacitor connects to get more accurate clock when in crystal mode.
X32O/RSUB2	O	32.768 KHz crystal output pad or external resistor node 2 **by mask option.** External 15~20pF capacitor connects to get more accurate clock when in crystal mode.
RA0 ~ RA3/TONE	I/O	General Input/Output port specified by PM1 register. If output mode is selected, PM0 register bit 0 can be used to specify CMOS/NMOS driving capability option. Initial state is input mode. RA3 may be uses as TONE if bit 0 of MR0 special register is set to logic 1. An interrupt source.
RB0 ~ RB3	I/O	General Input/Output port specified by PM2 register. If output mode is selected, PM0 register bit 1 can be used to specify CMOS/NMOS driving capability option. Initial state is input mode.
RC0 ~ RC3	I	4-bit schmitter input with internal pull high option specified by PM3 register bit 2. Each pad has an independent interrupt capability specified by PEFL special register. Interrupt and STOP mode wake up source. RC0 is also the external event counter source of Timer1.
RD0 ~ RD3	I	4-bit schmitter input port with internal pull high option specified by PM3 register bit 3. Each pad has an independent interrupt capability specified by PEFH special register. Interrupt and STOP mode wake up source.
RE0~RE3	O	Output port only. PM3 register bit 0 can be used to specify CMOS/NMOS driving capability option.
RF0~RF3	O	Output port only. PM3 register bit 1 can be used to specify CMOS/NMOS driving capability option.
RG0 ~ RG3	I	Input port with internal pull high option specified by PM6 register bit 0. (W536090P/W536120P only)
RH0 ~ RH3	O	Output port only. PM6 register bit 1 can be used to specify CMOS/NMOS driving capability option. (W536090P/W536120P only)
$\overline{\text{RES}}$	I	System reset pad, active low with internal pull-high resistor.
TEST	I	Test pad. Active high with internal pull low resistor.
ROSC	I	Connect resistor to VDD pad to generate speech or melody playing clock source.
PWM1/DAC	O	While speech or melody is active, PWM1/DAC is speaker direct driving output or DAC output controlled by voice output file.
PWM2	O	While speech or melody is active, PWM2 is another speaker direct driving output.
WRP	O	External serial memory address write clock for voice extension.

RDP	O	External serial memory address read clock for voice extension.
SPDATA	I/O	External serial memory data in/out for voice extension.
VSS	I	Chip ground.
VSSP	I	Chip ground for PWM or DAC playing output.
VSSA (3)	I	Chip ground. (W536090P/120P only)
VDD	I	Power source.
VDDP	I	Power source for PWM or DAC playing output.
VDDA (3)	I	Power source. (W536090P/120P only)

(3) VDDA, VSSA for W536090P/120P only. To sure chip operation properly, please bond all VDD, VDDA, VDDP, VSS, VSSA and VSSP pads, and connect VSS, VSSP form chip external PCB circuit.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(VDD–VSS = 3.0V, F_M = 4 MHz with RC mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Op. Voltage	V_{DD}		2.4		5.5	V
Op. Current (No Load, no Voice, no Melody)	I_{OP1}	Dual clock with crystal	-	400	500	uA
		Dual clock with RC type		400	500	
		Sub-clock only		15	30	
Hold Mode Current	I_{OP2}	Sub-clock active only		4	6	uA
Stop Mode Current	I_{OP3}				1	uA
RDP/WRP Output High Current	I_{OH1}	Vout =2.7V			-0.8	mA
RDP/WRP Output low Current	I_{OL1}	Vout =0.4V			0.8	mA
Input Low Voltage	V_{IL}	-	VSS	-	0.3	VDD
Input High Voltage	V_{IH}	-	0.7	-	1	VDD
Port RA, RB, RE,RF and RH Output Low Voltage	V_{ABL}	IOL = 2.0 mA	-	-	0.4	V
Port RA, RB, RE,RF and RH Output High Voltage	V_{ABH}	IOH = -2.0 mA	2.4	-	-	V

Pull-up Resistor	RCD	Port RC, RD, RG	200	300	400	KΩ
RES Pull-up Resistor	RRES	-	50	100	200	KΩ
PWM1/2 Source Current (4) (R_{LOAD} =8Ω between PWM1 And PWM2)	ISPH	Volume Option =00		-20		mA
		Volume Option =01		-70		
		Volume Option =10		-110		
		Volume Option =11		-135		
PWM1/2 Sink Current (4) (R_{LOAD} =8Ω between PWM1 And PWM2)	ISPL	Volume Option =00		20		mA
		Volume Option =01		70		
		Volume Option =10		110		
		Volume Option =11		135		
DAC output Current	IDAC	VDD=3v, RL=100ohm	-4	-5	-6	mA

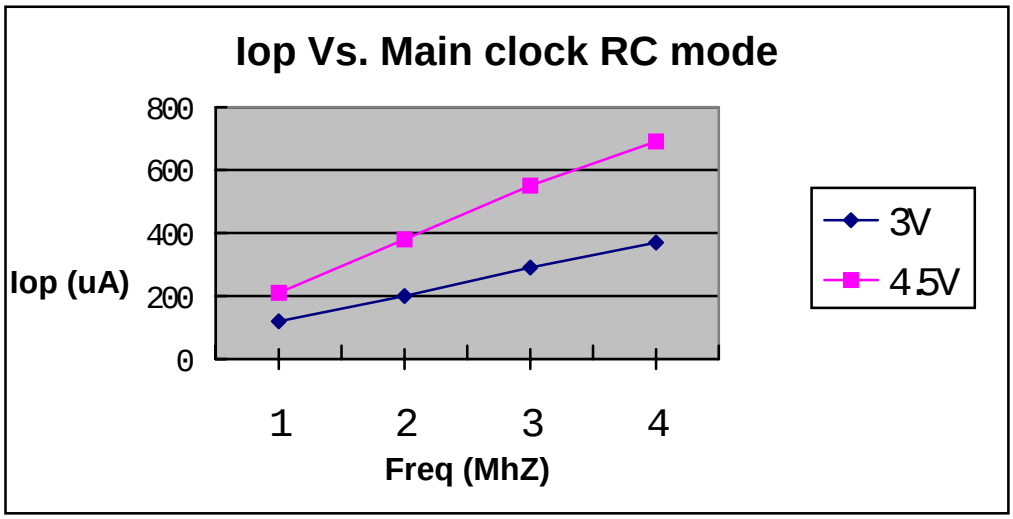
(4) PWM current deviation will be ±20%.

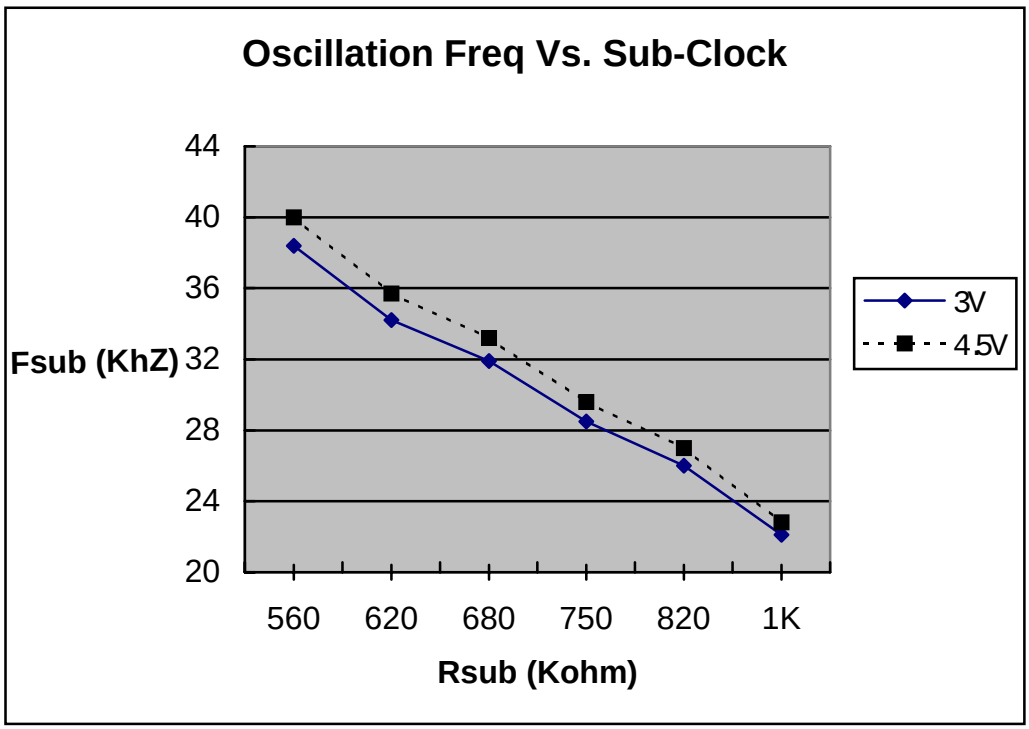
AC CHARATERISTICS

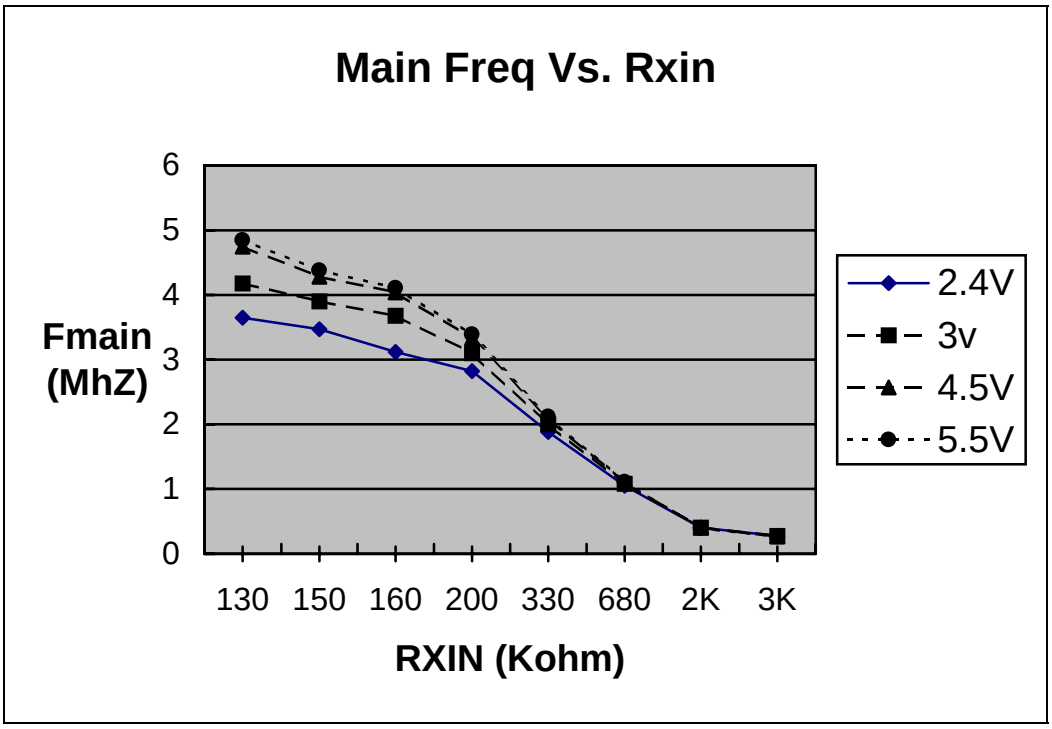
(VDD–VSS = 3.0V, FM = 4 MHz with RC mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C unless otherwise specified)

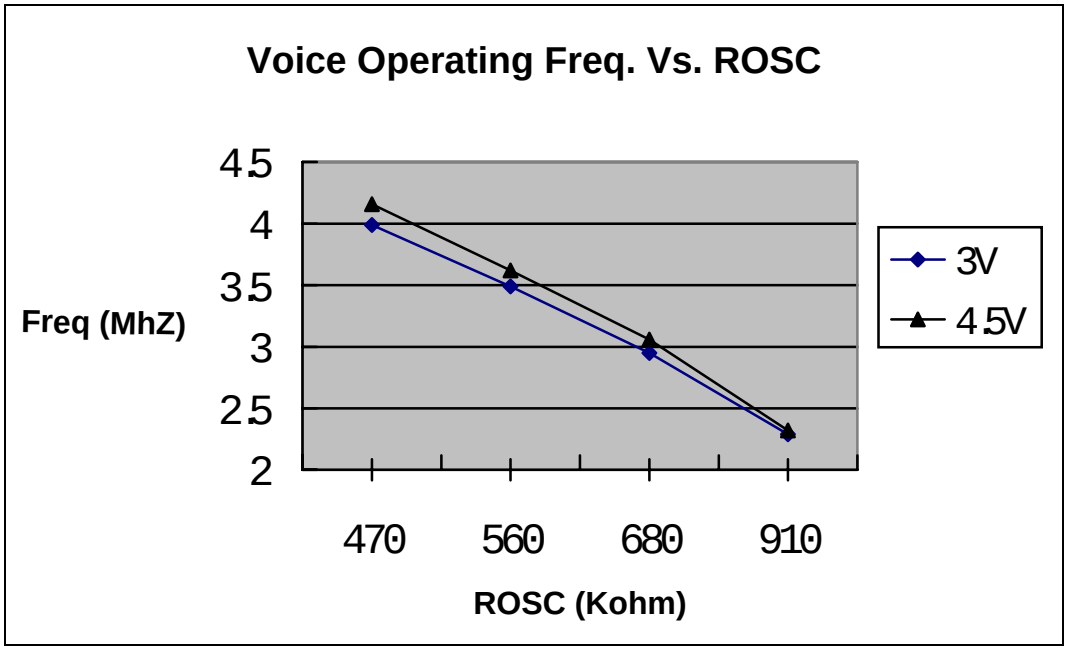
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	FSUB	Crystal type and X32IN and X32O with 17pF external cap.		32768		Hz
Main-clock Frequency	FM	RC type/Crystal type	400K	-	4M	Hz
Chip Operation Frequency	FOSC	SCR0.0=1,FSYS= FSUB		32768		Hz
		SCR0.0=0;FSYS= FMAIN	400K	-	4M	
Instruction Cycle Time	TCYC	One machine cycle	-	4/FOSC	-	S
Reset Active Width	TRAW	FOSC = 32.768 KHz	1	-	-	µS
Interrupt Active Width	TIAW	FOSC = 32.768 KHz	1	-	-	µS
Main clock RC frequency	FRXIN	RXIN =680KΩ		1M		Hz
		RXIN =330K Ω		2M		
		RXIN =200KΩ		3M		
		RXIN =130KΩ		4M		
Sub-Clock Ring Oscillator	FRSUB	RSUB=680KΩ		32		KHz
Sub-Clock Oscillation Stable Time @ Cold Start	FSTOP	RSUB=680KΩ	0.8		1	S
Frequency Deviation of main-clock FRXIN ≤ 2 MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			10	%
Frequency Deviation of main-clock FRXIN = 3 MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			15	%
Frequency Deviation of main-clock FRXIN = 4 MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			20	%
ROSC Frequency	FROSC	ROSC=680KΩ		3		MHz
Frequency Deviation of FROSC = 3MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			7.5	%

(5) The deviation will be +20% while VDD drops from 5.5V to 2.4V based on same resistor

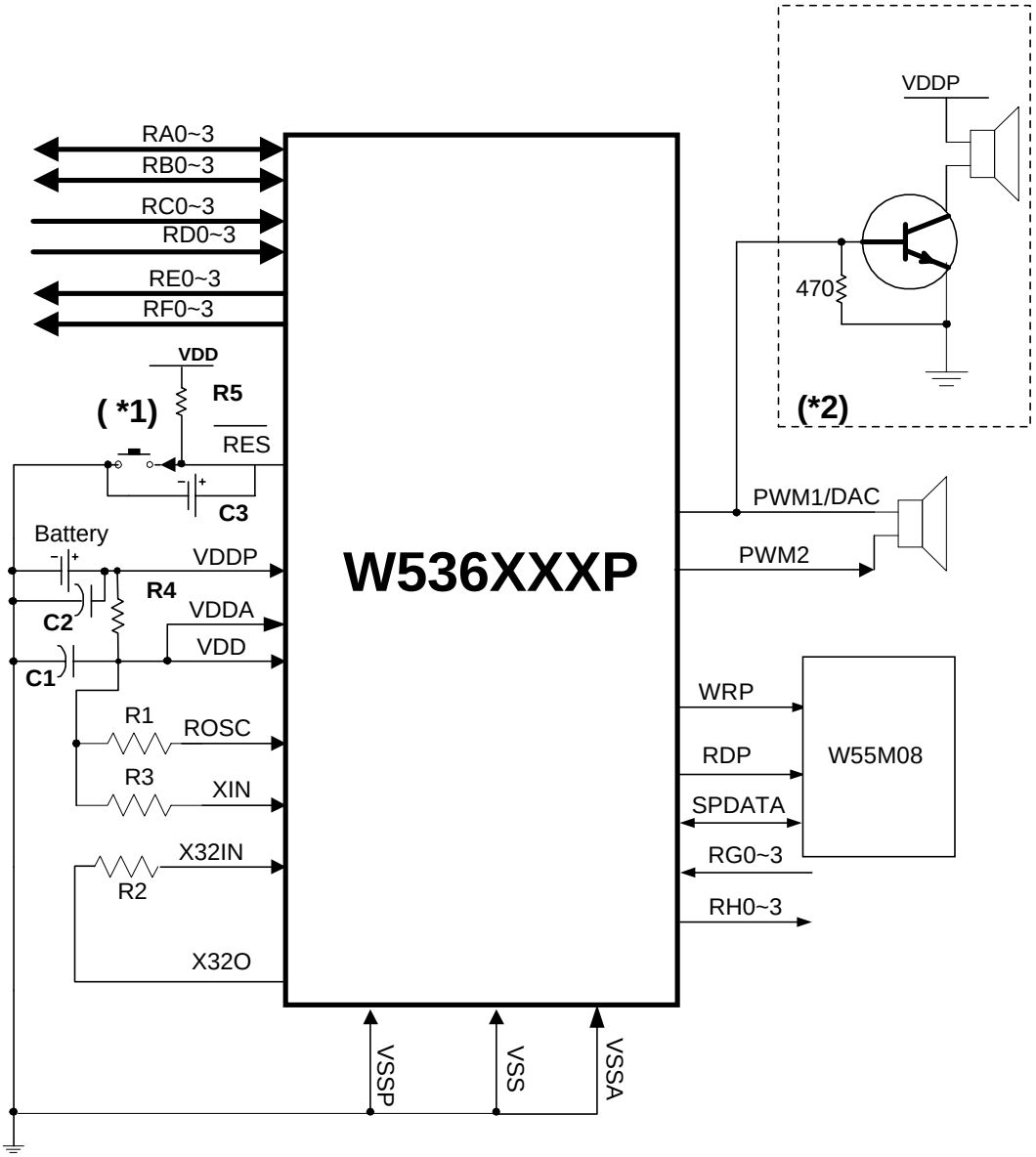

Iop Vs. Main clock RC mode
800
600
400
200
0
Iop (uA)
1
2
3
4
Freq (MhZ)
3V
4.5V


Oscillation Freq Vs. Sub-Clock
44
40
36
32
28
24
20
Fsub (KhZ)
560
620
680
750
820
1K
Rsub (Kohm)
3V
4.5V


Main Freq Vs. Rxin
Fmain (MhZ)
6
5
4
3
2
1
0
130
150
160
200
330
680
2K
3K
RXIN (Kohm)
2.4V
3v
4.5V
5.5V


Voice Operating Freq. Vs. ROSC
Freq (MhZ)
4.5
4
3.5
3
2.5
2
470
560
680
910
ROSC (Kohm)
3V
4.5V

APPLICATION CIRCUIT--1: Sub clock with RC mode



Component	C1	C2	C3	R1	R2	R3	R4
Value	0.1uF	4.7uF	0.1uF	680K	680K	680Kohm/1Mhz 330Kohm/2Mhz 200Kohm/3Mhz 130Kohm/4Mhz	100

Note:

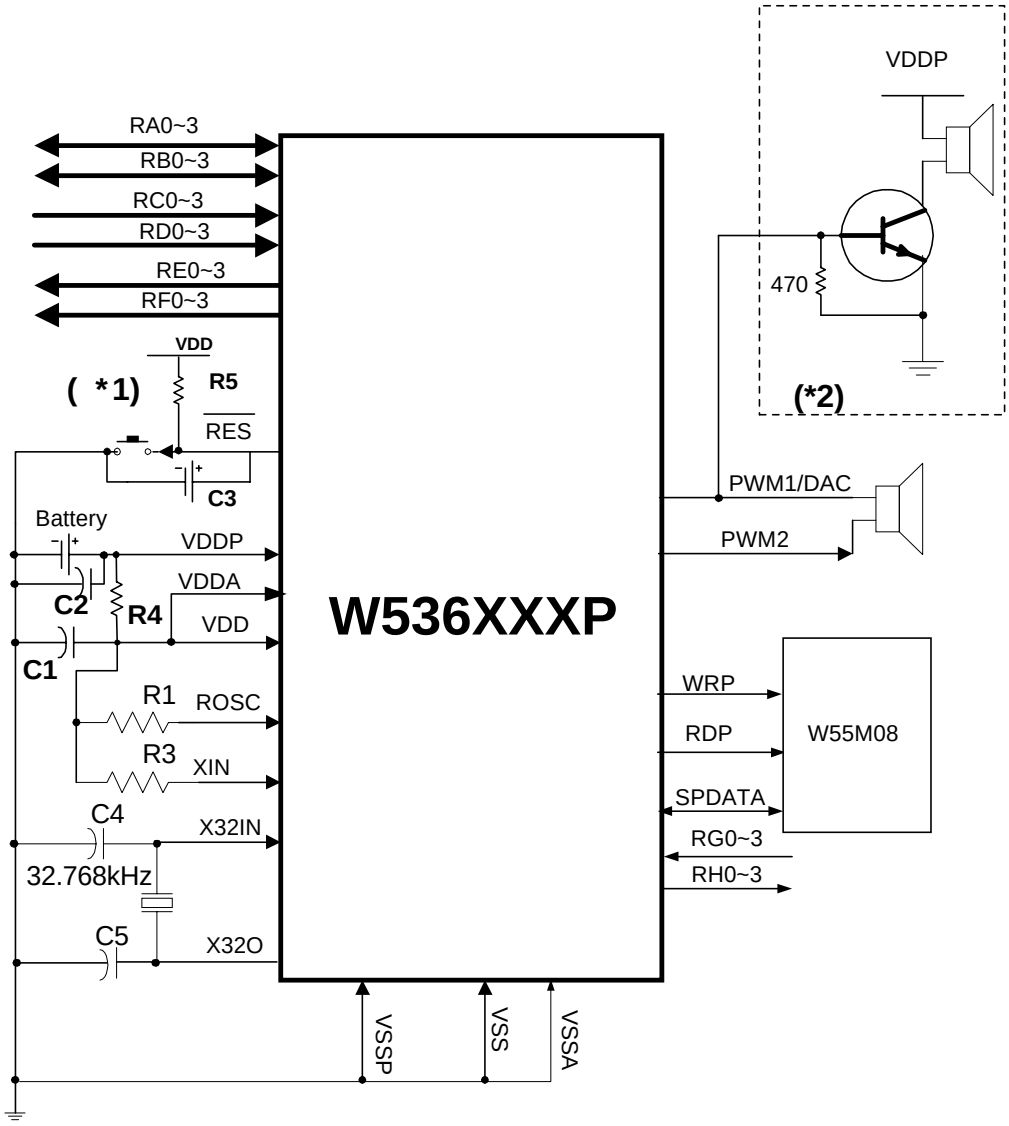
(1) Option R5 equals to 100Ω if high noise immunity is needed.

(2) For DAC option application

(3) To sure chip operation properly, please bond all VDDP, VDD, VDDA, VSSP, VSSA and VSS

(4) VDDA, VSSA are only for W536090P/120P.

APPLICATION CIRCUIT--2: Sub clock with Xtal mode



Component	C1	C2	C3	C4~C5	R1	R3	R4
Value	0.1uF	4.7uF	0.1uF	17pF~20pF	680K	680Kohm/1Mhz 330Kohm/2Mhz 200Kohm/3Mhz 130Kohm/4Mhz	100

Note:

(1) Option R5 equals to 100Ω if high noise immunity is needed.

(2) For DAC option application.

(3) To sure chip operation properly, please bond all VDDP, VDD, VDDA, VSSP , VSSA and VSS .

(4) VDDA and VSSA are only for W536090P/120P.