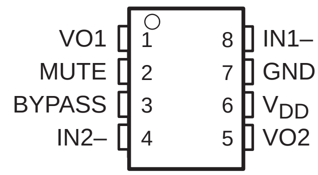
SLOS210 – JUNE 1998

- High-Fidelity Line-Out/HP Driver
- 75-mW Stereo Output
- PC Power Supply Compatible
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface Mount Packaging
- Pin Compatible with TPA302

**D PACKAGE
(TOP VIEW)**



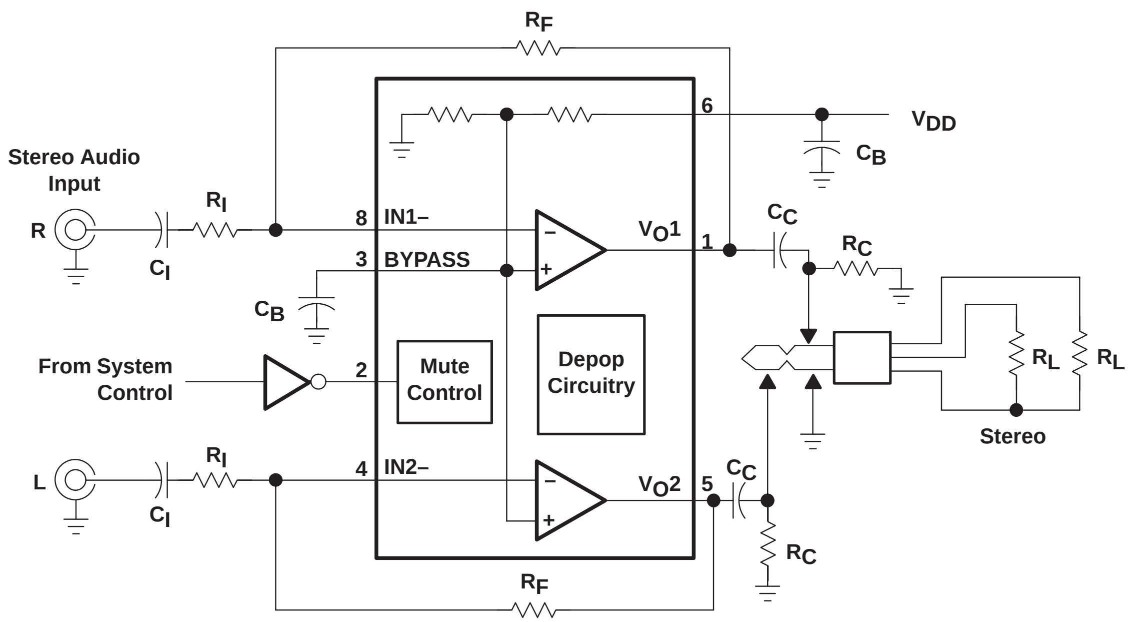
description

The TPA152 is a stereo audio power amplifier capable of less than 0.1% THD+N at 1 kHz when delivering 75 mW per channel into a 32-Ω load. THD+N is less than 0.2% across the audio band of 20 to 20 kHz. For 10 kΩ loads, the THD+N performance is better than 0.005% at 1 kHz, and less than 0.01% across the audio band of 20 to 20 kHz.

The TPA152 is ideal for use as an output buffer for the audio CODEC in PC systems. It is also excellent for use where a high-performance head phone/line-out amplifier is needed. Depop circuitry is integrated to reduce transients during power up, power down, and mute mode.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10. The TPA152 is packaged in the 8-pin SOIC (D) package that reduces board space and facilitates automated assembly.

typical application circuit



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE
–40°C to 85°C	TPA152D†

† The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA152DR)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	3		BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
GND	7		GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
MUTE	2	I	A logic high puts the device into MUTE mode.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
VO1	1	O	VO1 is the audio output for channel 1.
VO2	5	O	VO2 is the audio output for channel 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} . . . . . . 6 V
Input voltage , V_I . . . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . . Internally Limited (See Dissipation Rating Table)
Operating junction temperature range, T_J . . . . . . –40°C to 150° C
Operating case temperature range, T_C . . . . . . –40°C to 125° C
Storage temperature range, T_{stg} . . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	724 mW	5.8 mW/°C	464 mW	376 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	4.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{IO}\|$	Input offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		81		dB
I_{DD}	Supply current	See Figure 13		5.5	14	mA
$I_{DD(MUTE)}$	Supply current in MUTE			5.5	14	mA
Z_I	Input impedance			>1		MΩ

ac operating characteristics V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.03%,	Gain = 1,	See Figure 1		75†		mW
THD+N	Total harmonic distortion plus noise	P_O = 75 mW, See Figure 2	20 Hz–20 kHz,	Gain = 1,		0.2%		
B_{OM}	Maximum output power bandwidth	G = 5,	THD <0.6%,	See Figure 2		>20		kHz
	Phase margin	Open loop,	See Figure 16			80°		
k_{SVR}	Supply voltage rejection ratio	1 kHz,	C_B = 1 µF,	See Figure 12		65		dB
	Mute attenuation	See Figure 15				110		dB
	Ch/Ch output separation	See Figure 13				102		dB
	Signal-to-Noise ratio	V_O = 1 $V_{(rms)}$,	Gain = 1	See Figure 11		104		dB
v_n	Noise output voltage	See Figure 10				6		µV(rms)

† Measured at 1 kHz.

NOTES: 1. The dc output voltage is approximately V_{DD}/2.
2. Output power is measured at the output pins of the IC at 1 kHz.

ac operating characteristics V_{DD} = 5 V, T_A = 25°C, R_L = 10 kΩ

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion plus noise	V_I = 1 $V_{(rms)}$, See Figure 6	20 Hz–20 kHz, Gain = 1,			0.005%		
		$V_{O(PP)}$ = 4 V, See Figure 8	20 Hz–20 kHz, Gain = 1,			0.005%		
B_{OM}	Maximum output power bandwidth	G = 5,	THD <0.02%,	See Figure 6		>20		kHz
	Phase margin	Open loop,	See Figure 16			80°		
k_{SVR}	Supply voltage rejection ratio	1 kHz,	C_B = 1 µF,	See Figure 12		65		dB
	Mute attenuation	See Figure 15				110		dB
	Ch/Ch output separation	See Figure 13				102		dB
	Signal-to-Noise ratio	V_O = 1 $V_{(rms)}$,	Gain = 1,	See Figure 11		104		dB
v_n	Noise output voltage	See Figure 10				6		µV(rms)

† Measured at 1 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4
THD+N	Total harmonic distortion plus noise	vs Frequency	2, 3, 6, 8, 9
THD+N	Total harmonic distortion plus noise	vs Output voltage	5, 7
V_n	Output noise voltage	vs Frequency	10
SNR	Signal-to-noise ratio	vs Gain	11
PSRR	Power supply rejection ratio	vs Frequency	12
	Crosstalk	vs Frequency	13, 14
	Mute Attenuation	vs Frequency	15
	Open-loop gain	vs Frequency	16, 17
	Closed-loop gain	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
P_O	Output power	vs Load resistance	20
P_D	Power dissipation	vs Output power	21

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

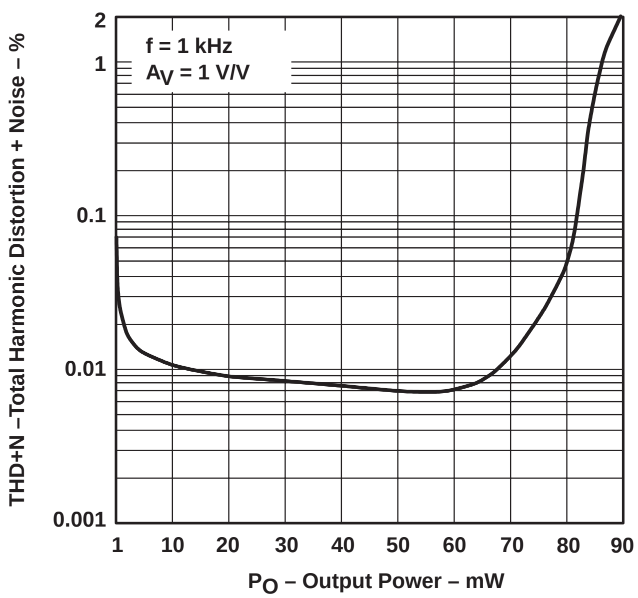


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

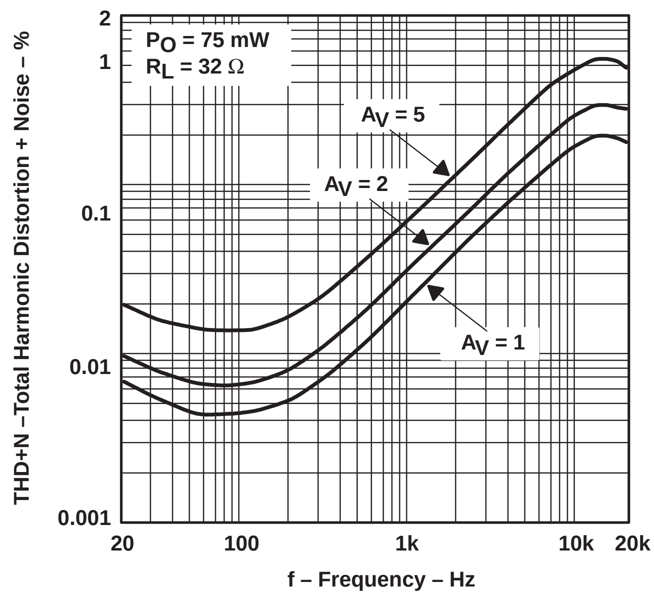


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

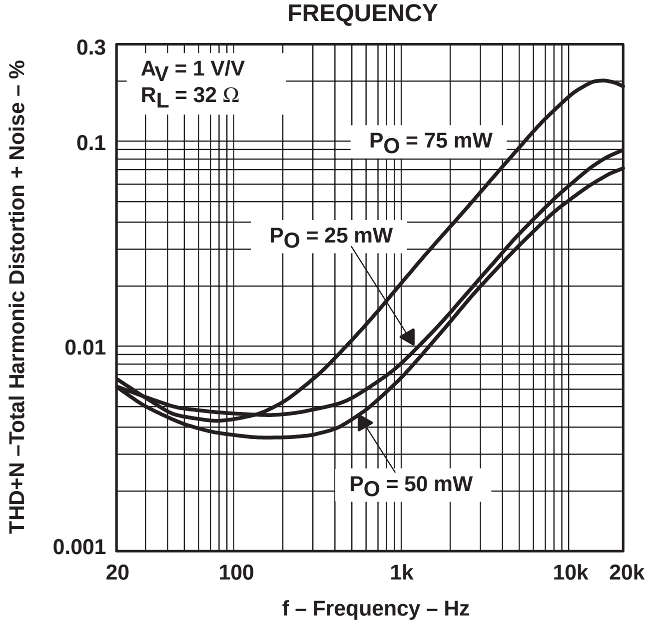


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

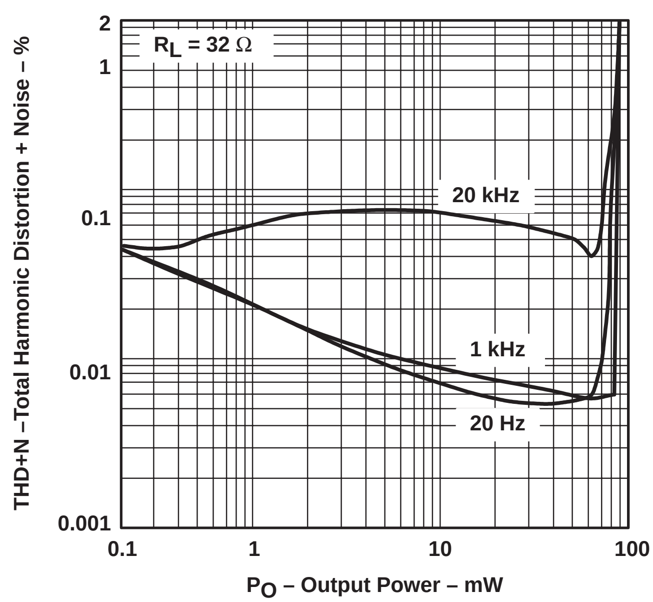


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

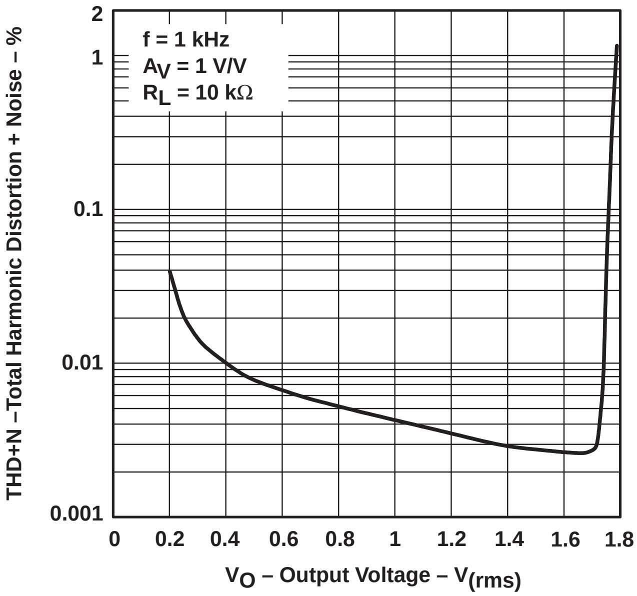


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

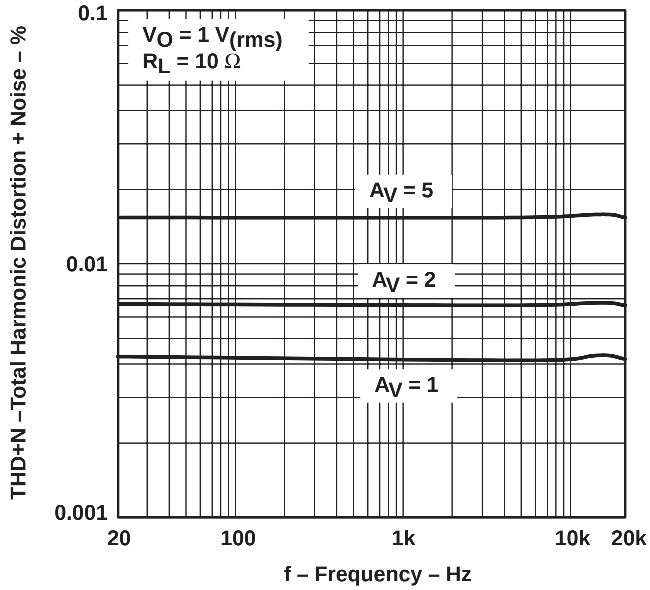


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT VOLTAGE

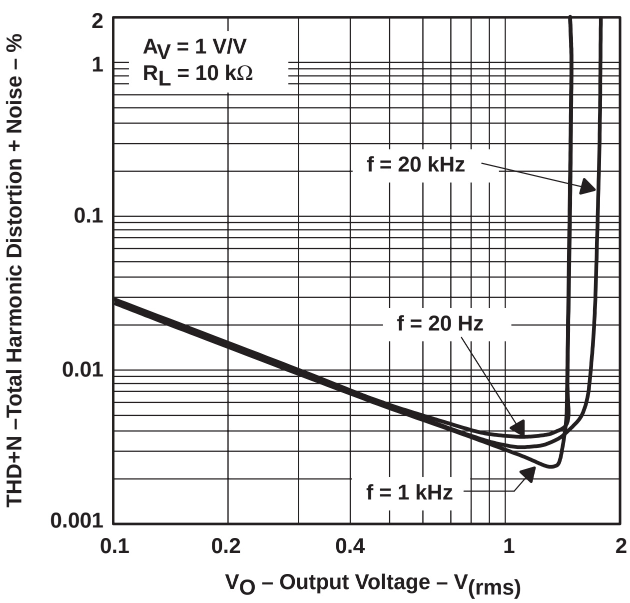


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

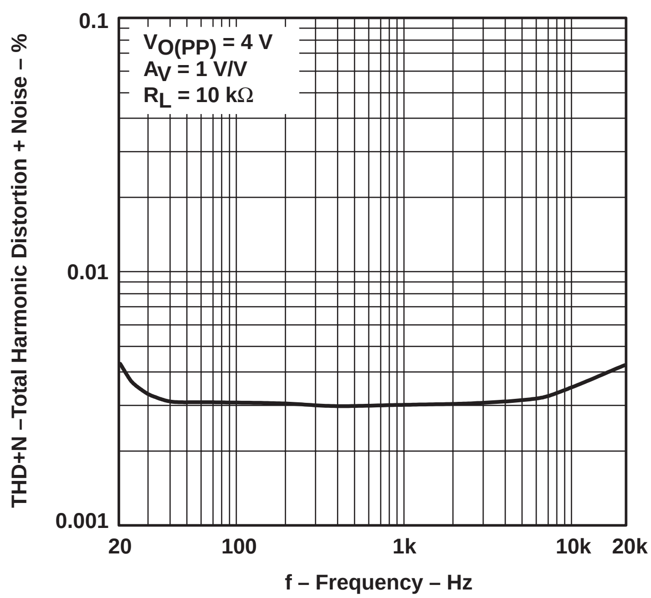


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

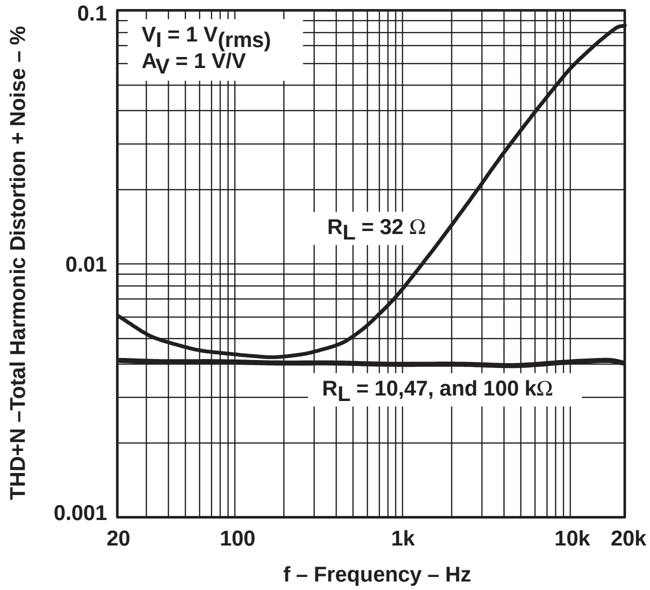


Figure 9

OUTPUT NOISE VOLTAGE vs FREQUENCY

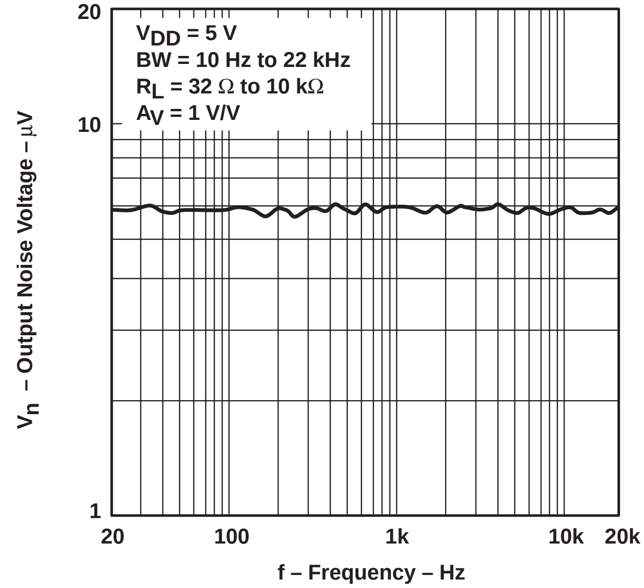


Figure 10

SIGNAL-TO-NOISE RATIO vs GAIN

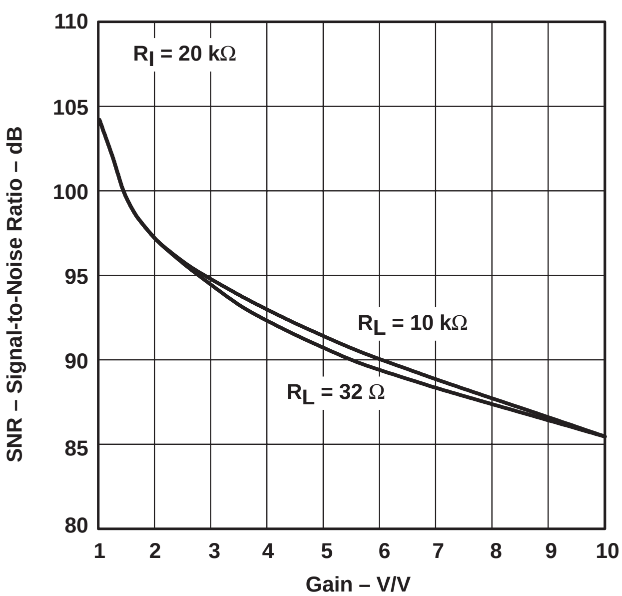


Figure 11

POWER SUPPLY REJECTION RATIO vs FREQUENCY

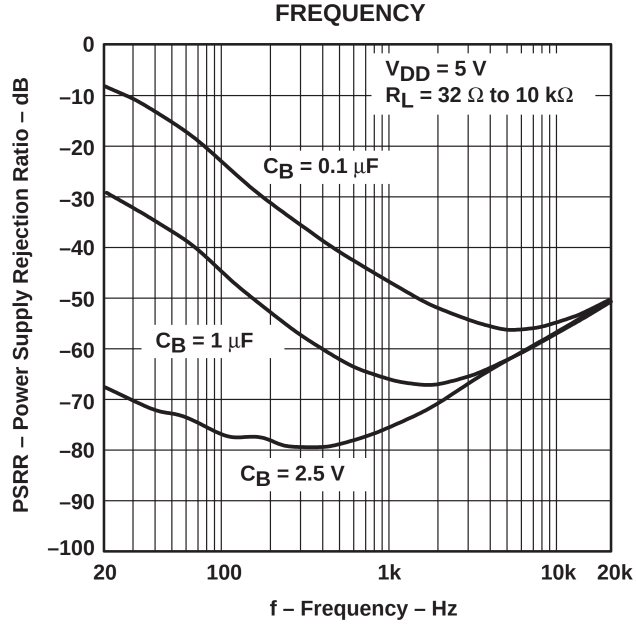


Figure 12

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

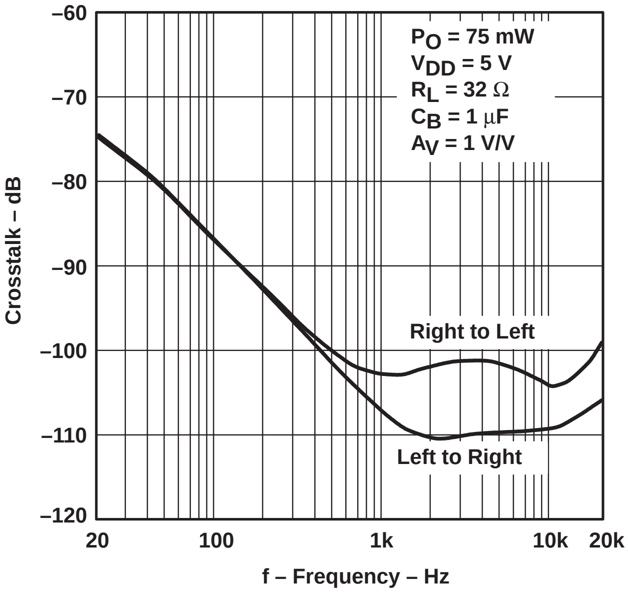


Figure 13

CROSSTALK
vs
FREQUENCY

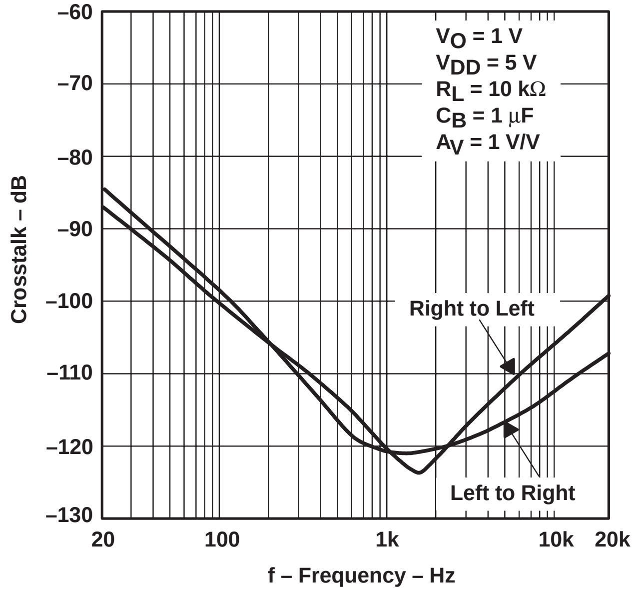


Figure 14

MUTE ATTENUATION
vs
FREQUENCY

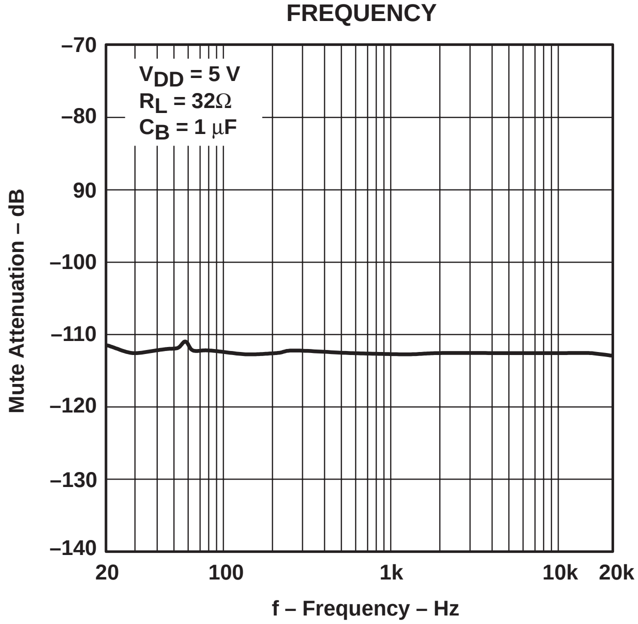


Figure 15

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

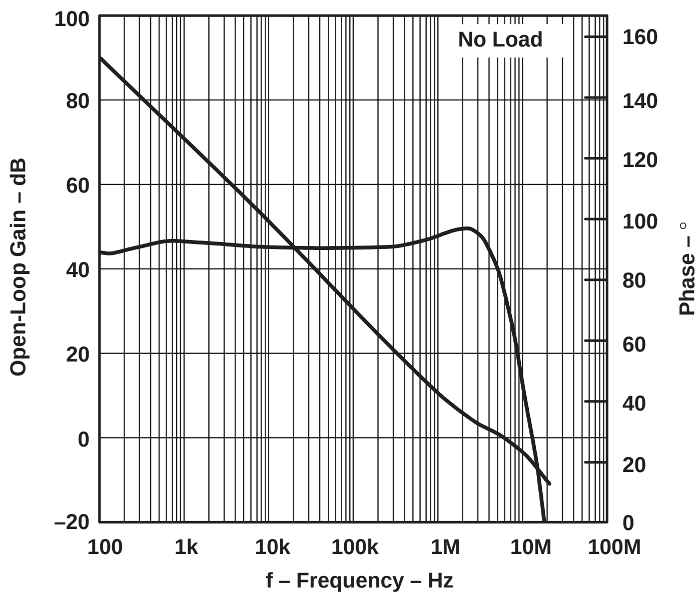


Figure 16

**CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY**

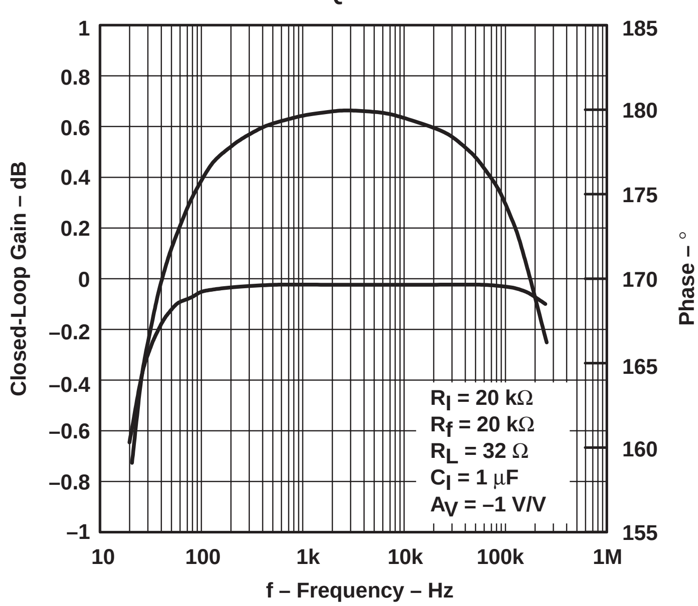


Figure 17

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

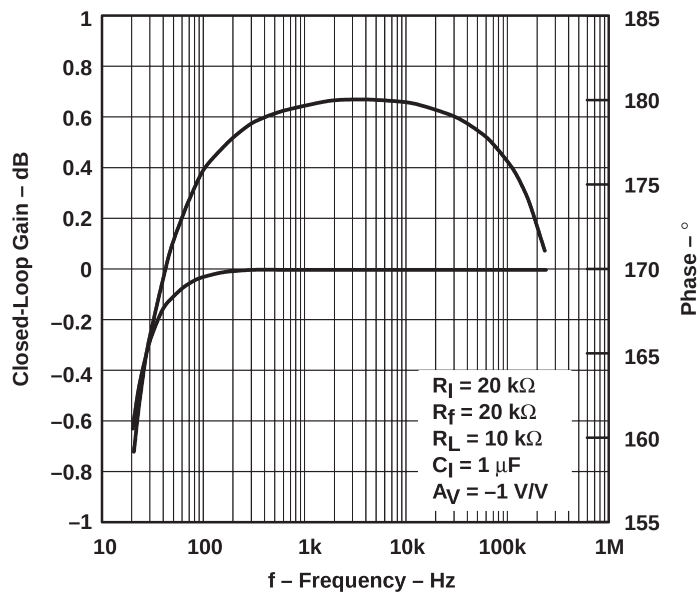


Figure 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

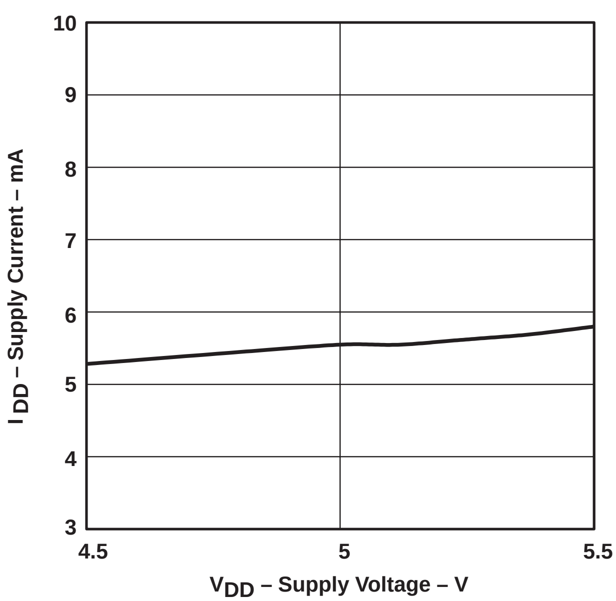


Figure 19

OUTPUT POWER vs LOAD RESISTANCE

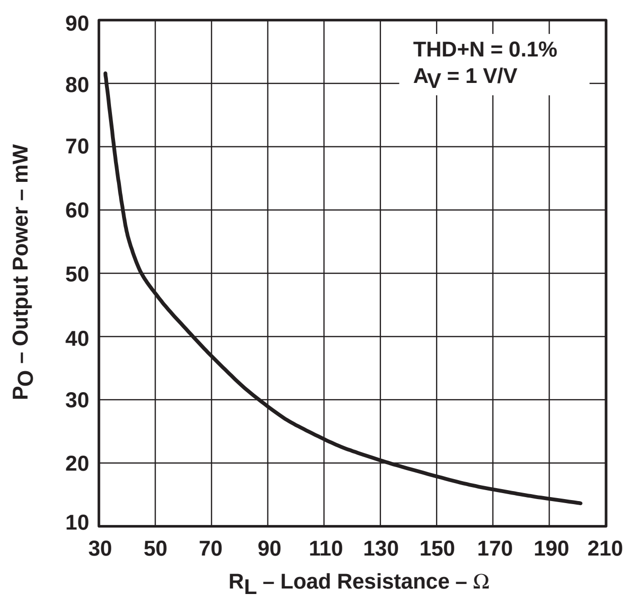


Figure 20

TYPICAL CHARACTERISTICS

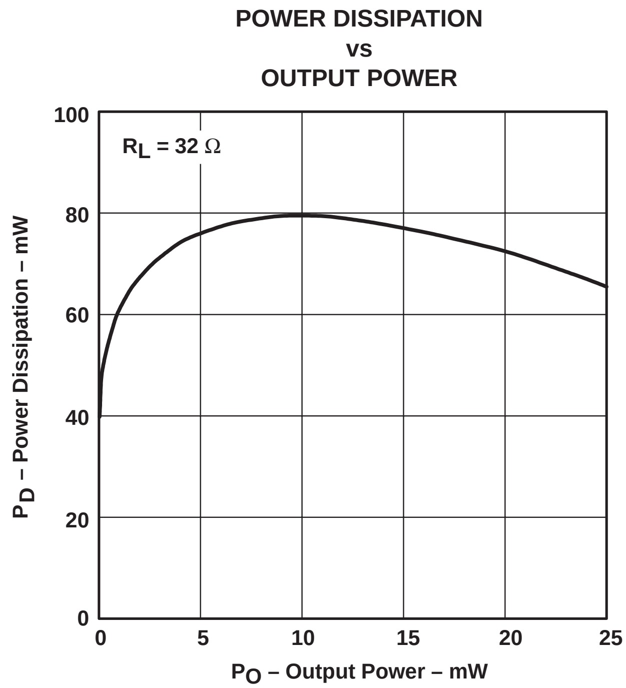
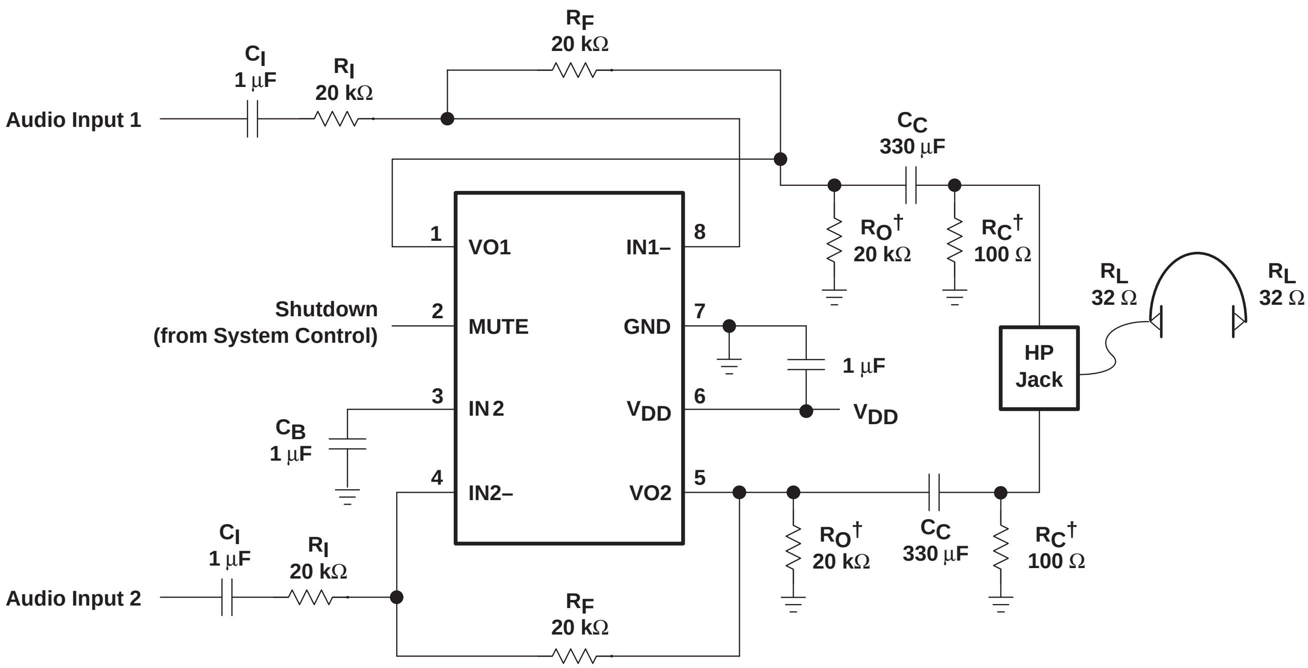


Figure 21

APPLICATION INFORMATION

selection of components

Figure 22 is a schematic diagram of a typical application circuit.



† These resistor are optional. Adding these resistors improves the depop performance of the TPA152.

Figure 22. TPA152 Typical Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA152 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA152 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example if R_F is 100 kΩ and C_F is 5 pF then $f_{co(lowpass)}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{co(highpass)}} \quad (5)$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA152 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 160\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \qquad (6)$$

As an example, consider a circuit where C_B is 1 μF, C_I is 1 μF and R_I is 20 kΩ. Inserting these values into the equation 9 results in:

$$6.25 \leq 50$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_{(\text{out high})} = \frac{1}{2\pi R_L C_C} \qquad (7)$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 160\ k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \qquad (8)$$

output pull-down resistor, $R_C + R_O$

Placing a 100-Ω resistor, R_C, from the output side of the coupling capacitor to ground insures the coupling capacitor, C_C, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones.

Placing a 20-kΩ resistor, R_O, from the output of the IC to ground insures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10-kΩ loads.

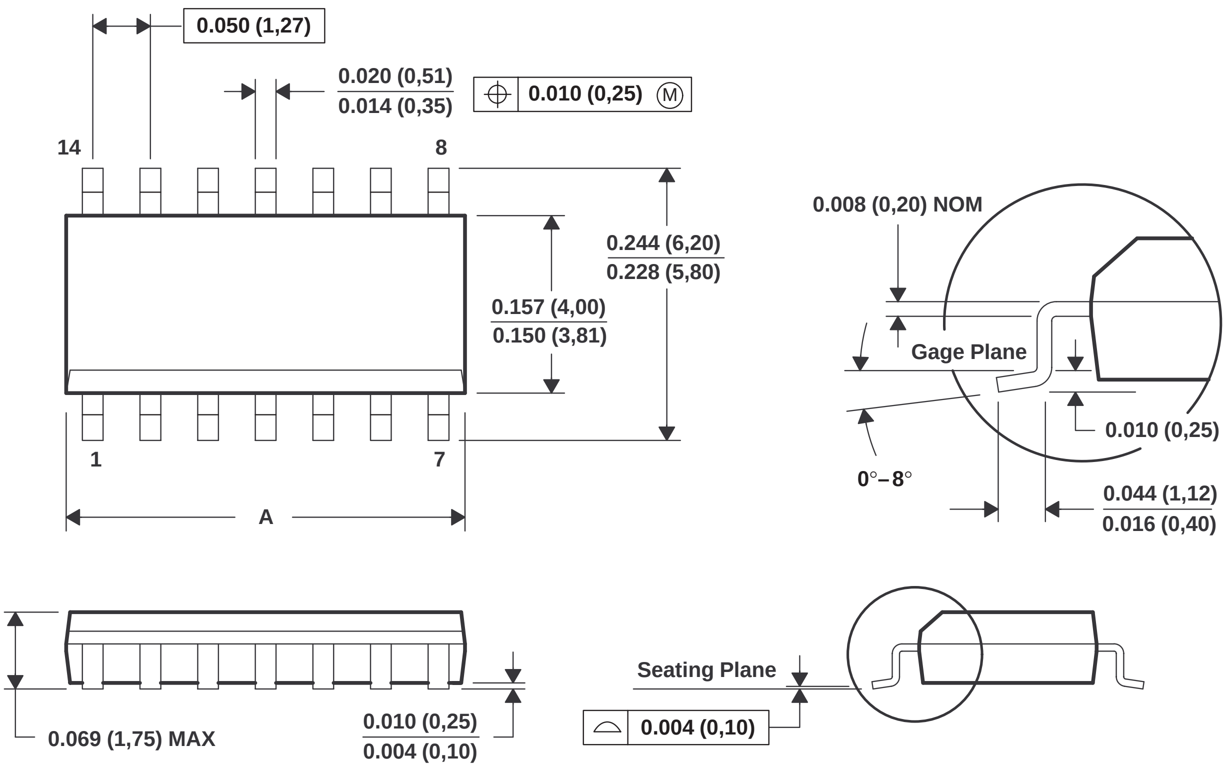
using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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