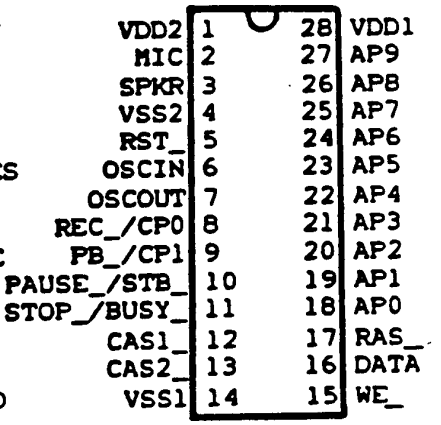
TMS3477
CVSD VOICE RECORDER

January 1988

- SINGLE CHIP VOICE RECORDER/PLAYER
  - 28 PIN SHRINK(400 MIL) DIP
  - CMOS Si-GATE PROCESS
  - SINGLE +5V POWER SUPPLY
- FULL DIGITAL CVSD WITH HIGH FIDELITY
  - THREE POINTS BASE DATA SAMPLING CLOCK SELECTION (16K,32K AND 64KHz)
  - 10 BIT D/A CONVERTOR OUTPUT WITH TYPICAL 64KHz OVER-SAMPLING CLOCK
  - CARRIER SUPPRESSION ALGORITHM REDUCES OVER-SAMPLING CARRIER NOISE
- USING DRAMs AS ENCODED DTATA STORAGE
  - DRAM REFRESH COUNTER ON CHIP
  - DIRECT INTERFACE WITH TMS4164, TMS4256 OR TMS4C1024
  - 1-PHRASE/1-DRAM OR 1-PHRASE/2-DRAMs CONFIGURATION WITH VARIABLE OR FIXED PHRASE SIZE
  - INTERFACING WITH UP TO 6 DRAMs
- SIMPLE OPERATION WITH HIGH FLEXIBILITY
  - ONE TIME OPERATION FOR "RECORDING", "PLAY-BACK","PAUSE" AND "STOP" IN KEY-INTERFACE MODE
  - SIMPLE COMMAND PORT INTERFACE WITH BUSY_ SIGNAL IN CPU-INTERFACE MODE
  - CYCLIC RECORDING, RECORDING MONITOR AND DATA COMPRESSION MODE ARE AVAILABLE

TMS3477
28 PIN SHRINK DIP
(TOP VIEW)



ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

TEXAS INSTRUMENTS JAPAN LIMITED

TERMINAL FUNCTIONS

VDD1	+5V POWER SUPPLY FOR DIGITAL LOGIC
VDD2	+5V POWER SUPPLY FOR ANALOG LOGIC
VSS1	GROUND FOR DIGITAL LOGIC
VSS2	GROUND FOR ANALOG LOGIC
RST_ (INPUT)	SYSTEM RESET. ACTIVE LOW INPUT.
OSCIN (INPUT)	SCHMITT TYPE OSCILLATOR INPUT.
OSCOUT (OUTPUT)	OSCILLATOR OUTPUT
MIC (INPUT)	ANALOG SIGNAL INPUT FOR RECORDING. BIASED IN 1/2 VDD LEVEL INTERNALLY. PEAK TO PEAK VOLTAGE LEVEL OF ANALOG INPUT SIGNAL MUST BE WITHIN 1/2 VDD RANGE WITH COUPLING CONDENSER.
SPKR (OUTPUT)	10 BIT D/A OUTPUT FOR PLAY-BACK. BIASED IN 1/2 VDD LEVEL INTERNALLY. PEAK TO PEAK OUTPUT VOLTAGE IS VDD MAX. COUPLING CONDENSER IS REQUIRED EXTERNALLY.
PB_/ (INPUT) CP1	PB COMMAND INPUT WITH ACTIVE ON-CHIP PULL-UP RESISTOR IN KEY-INTERFACE MODE. COMMAND PORT-1 WITH INACTIVE ON-CHIP PULL-UP RESISTORS IN CPU-INTERFACE MODE.
REC_/ (INPUT) CP0	REC COMMAND INPUT WITH ACTIVE ON-CHIP PULL-UP RESISTOR IN KEY-INTERFACE MODE. COMMAND PORT-0 WITH INACTIVE ON-CHIP PULL-UP RESISTOR IN CPU-INTERFACE MODE.
PAUSE_/ (INPUT) STB_	PAUSE COMMAND INPUT WITH ACTIVE ON-CHIP PULL-UP RESISTOR IN KEY-INTERFACE MODE. COMMAND STROBE INPUT WITH INACTIVE ON-CHIP PULL-UP RESISTOR IN CPU-INTERFACE MODE.
STOP_/ (I/O) BUSY_	STOP COMMAND INPUT WITH ACTIVE ON-CHIP PULL-UP RESISTOR IN KEY-INTERFACE MODE. BUSY_ SIGNAL OUTPUT WITH INACTIVE ON-CHIP PULL-UP RESISTOR IN CPU-INTERFACE MODE.
CAS1_ (OUTPUT)	COLUMN ADDRESS SELECT SIGNAL OUTPUT FOR UPPER PHRASE.
CAS2_ (OUTPUT)	COLUMN ADDRESS SELECT SIGNAL OUTPUT FOR LOWER PHRASE.
RAS_ (OUTPUT)	ROW ADDRESS SELECT SIGNAL OUTPUT.
WE_ (OUTPUT)	WRITE ENABLE SIGNAL OUTPUT.
DATA (I/O)	ENCODED DATA I/O PIN.
AP0-AP9 (I/O)	OUTPUT: ROW AND COLUMN ADDRESS OUTPUT WITH INACTIVE ON-CHIP PULL-UP RESISTORS. INPUT: EXECUTION MODE INPUT WITH ACTIVE ON-CHIP PULL-UP RESISTORS.

DESCRIPTION

TMS3477 is a single chip voice recording/play-back controller using Continuously Variable Slope Delta-modulation (CVSD). There are five commands to control the TMS3477 via Key-interface or CPU-interface mode. REC command to start/restart recording, PB command to start/restart playing-back, PAUSE command to pause recording/playing-back and STOP command to cancel the all of command execution. TMS3477 stores encoded bit stream into external DRAMs via DATA pin in recording operation. TMS3477 has a refresh counter on chip, and directly interfaces with TMS4164, TMS4256 or TMS4C1024. Each encoded bit is addressed by the address counter. When recording is finished by the STOP command or detecting End of Memory, the stop address is latched into the stop address register. The stop address is used to stop the data decoding in play-back operation. The mode register defines the TMS3477 execution mode, and programmed by external pull-down resistors tied to AP0-AP9 pins. The CVSD designed on TMS3477 is based on full digital logic which has high fidelity. Analog signal input on MIC pin is compared with output level of the 10 bit D/A converter at point of data sampling period. Series of data output from the comparater is stored into external DRAMs. Output of the D/A converter is produced by the estimate integrator and sillabic integrator based on the previous sampling data value. The TMS3477 produces speech signal with high fidelity by adapting the step voltage level of wave form, using 64 KHz typical over-sampling clock and suppressing the over-sampling carrier noise.

COMMAND

Four kind of command are available to controll the TMS3477.
Each command are transferred to the TMS3477 by switching to stable 32 ms "L" level at least with external switches connected to REC_, PB_, PAUSE_ and STOP_ pins directly in Key-interface mode. TMS3477 exhibits on-chip pull-up resistors on REC_, PB_, PAUSE_ and STOP_ pins in Key-interface mode.
In CPU-interface mode, CP1 and CP0 are assigned as command ports for four command bit pattern which is transferred to the TMS3477 with active low level strobe input on STB_ pin. BUSY_ signal with active low level is output on BUSY_ pin during TMS3477 is in busy state. TMS3477 inhibits on-chip pull-up resistors on CP1, CP0, STB_ AND BUSY_ pin in CPU-interface mode.

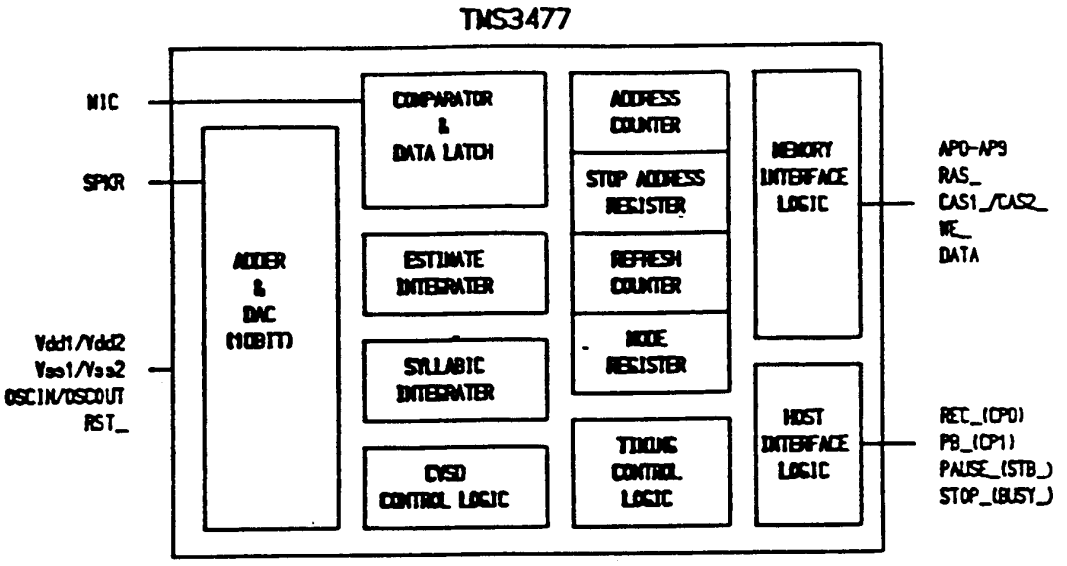


FIG-1 TMS3477 INTERNAL BLOCK DIAGRAM

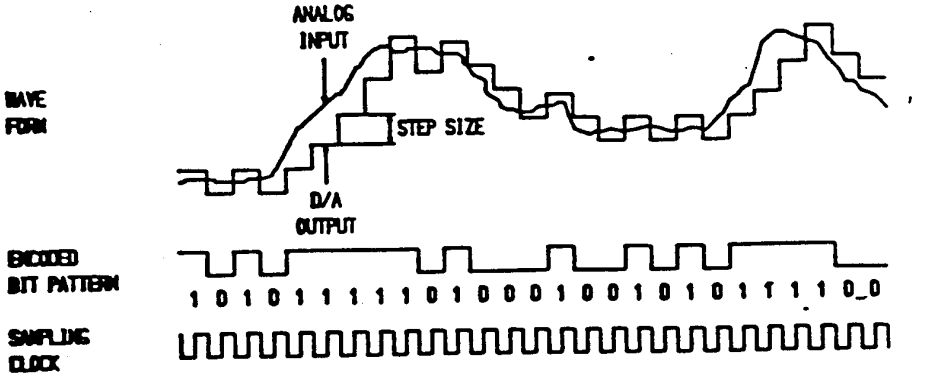


FIG-2 Continuously Variable Slope Delta-modulation (CVSD)

TABLE-1 Command

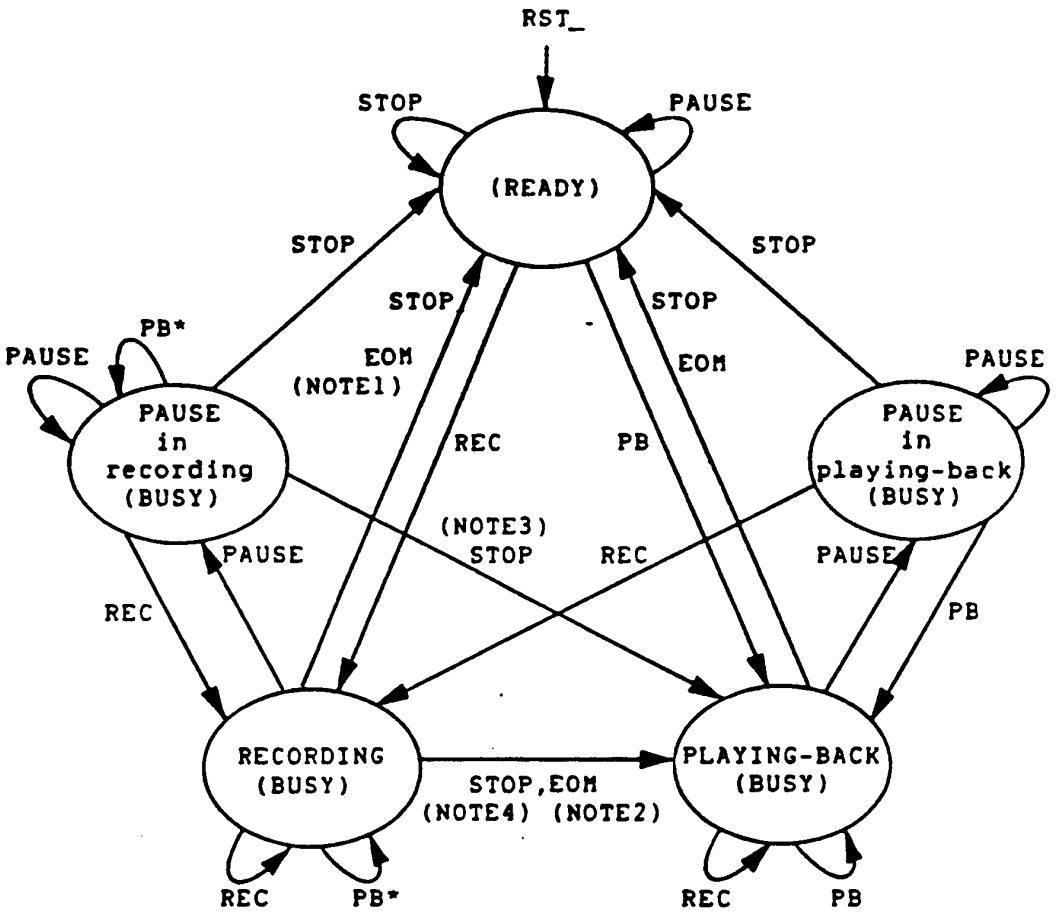
COMMAND	DESCRIPTION
REC COMMAND	Start or restart(in pausing) recording. Recording is stopped by STOP command or detecting End of Memory.
PB COMMAND	Start or restart(in pausing) playing_back. Playing-back is finished by STOP command, detecting stop address or End of Memory.
PAUSE COMMAND	Pause recording or playing-back. Pausing is cancelled by REC, PB and STOP command.
STOP COMMAND	Stop recording, playing-back and pausing.

TABLE-2 Command transfer in Key-interface mode

TERMINAL	INPUT	COMMAND
PAUSE_/STB_	LOW LEVEL	PAUSE COMMAND
PB_/CP1	LOW LEVEL	PB COMMAND
REC_/CP0	LOW LEVEL STROBE	REC COMMAND
STOP_/BUSY_	LOW LEVEL	STOP COMMAND

TABLE-3 Command transfer in CPU-interface mode

TERMINAL INPUT			
PB_/CP1	REC_/CP0	PAUSE_/STB_	COMMAND
LOW	LOW	LOW LEVEL STROBE	PAUSE COMMAND
LOW	HIGH	LOW LEVEL STROBE	PB COMMAND
HIGH	LOW	LOW LEVEL STROBE	REC COMMAND
HIGH	HIGH	LOW LEVEL STROBE	STOP COMMAND



REC: REC command
PB: PB command
PAUSE: PAUSE command
STOP: STOP command
EOM: End of Memory
RST_: Reset

(NOTE1): Ineffective in cyclic recording.
(NOTE2): Ineffective in cyclic recording.
Effective when PB* is already transferred.
(NOTE3): Effective when PB* is already transferred.
(NOTE4): Effective when PB* is already transferred.

FIG-3 TMS3477 STATE DIAGRAM

EXECUTION MODE

The mode register, which defines the TMS3477 execution mode, is programmed via AP0-AP9 input. TMS3477 has pull-up resistors on chip tied to AP0-AP9 pins, so the all "1" inputs are the default value of the mode register. AP0-AP9 turn to input mode and the on-chip pull-up resistors become effective after the period of reset completion, REC command transfer and PB command transfer, then TMS3477 loads the AP0-AP9 input into mode register. Therefore the external pull-down resistors tied to AP0-AP9 pins define the TMS3477 execution mode shown in TABLE-4.

DATA SAMPLING CLOCK

CVSD logic encodes into "0" or "1" at point of data sampling clock period (Fds). Therefore the speech data compress ratio, speech quality and recording time depend on the data sampling clock which is taken by following expression.

$$Fds = (Fosc \times Fbds) / 320,000$$

Fds: Data sampling clock (Hz)
Fosc: TMS3477 oscillator frequency (Hz)
Fbds: Base data sampling clock defined by AP6-AP7 input (Hz)

PHRASE FORMAT

A phrase can be in one DRAM or two DRAMs with variable phrase size or fixed phrase size. CAS1_ output is used in 1-phrase/1-DRAM system. CAS1_ selects upper half phrase and CAS2_ select lower half phrase in 1-phrase/2-DRAM system. For the variable phrase size, TMS3477 loads the stop address into stop address register in recording operation, and refers to the stop address register in play-back operation to stop the playing back at the end of phrase. The variable phrase is not available in TMS4164 interface mode.

CYCLIC RECORDING

TMS3477 cyclically records the encoded data into external DRAMs in cyclic recording mode. The cyclic recording finishes by receiving STOP command, and the over-laid data in DRAMs are sequentially decoded and played back by the PB command. In the cyclic recording, the latest speech data are always buffered in the DRAMs.

IMAGE UNAVAILABLE

DATA COMPRESSION

TMS3477 has a 10 bit D/A register which value is decoded and output by the D/A converter via SPKR pin. In the data compression mode, the contents of 10 bit D/A register is compressed into 8 bits which is shifted left two bit. Upper eight bits are the compressed data and lower two bits are filled with zeros. The compression mode is effective to emphasize the small signal in play-back operation, therefore do not use this mode in recording operation.

RECORDING MONITOR

When the recording monitor mode is selected by the AP9 input, TMS3477 plays back by using encoded bit in recording operation in real time.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

Supply voltage (NOTE1)	———	-0.3 V to 7 V
All input voltages (NOTE2)	———	-0.3 V to Vdd+0.3 V
Storage temperature range	———	-55 deg-C to +150 deg-C
Continuous power dissipation	———	300 mW

(NOTE1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposuer to absolute-maximum-rated conditions for extended periods may affect device reliability.

(NOTE2) Unless otherwise noted, all voltages are with respect to Vss.

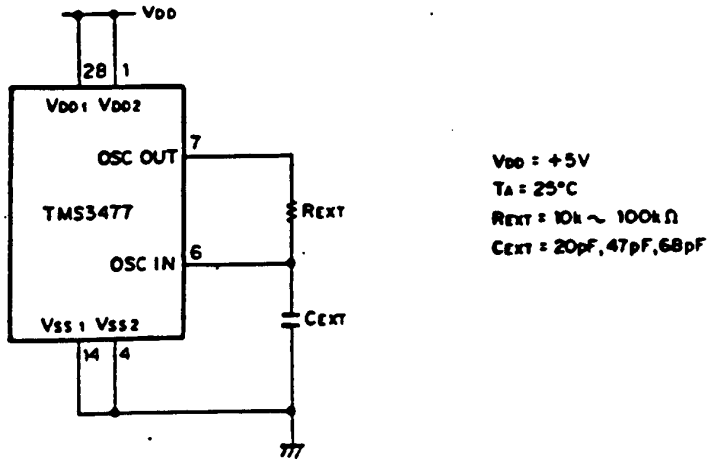
RECOMMENDED OPERATIONG CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	Vdd		4.5		5.5	V
High-level input voltage	Vih	DATA pin	2.2			V
		OSCIN,RST_ pin	0.85Vdd			V
		Except above pins and MIC pin	3.5			V
Low-level input voltage	Vil	Except MIC pin			0.8	V
Input voltage range	Vin	MIC pin	0.25Vdd		0.75Vdd	V
Oscillator frequency	Fosc	OSCIN pin	250	328	492	KHz
Operating free-air temp	Ta		-10		80	deg-C

ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Hi-level output voltage	Voh	Ioh=-1.0mA	2.4			V
Low-level output voltage	Vol	Iol=1.0mA			0.6	V
High-level input current	Iih	Vih=Vdd			10	uA
Low-level input current	Iil	Inactive pull-up resistor on chip Vil=Vss			-10	uA
	Iilr	Active pull-up resistor on chip Vil=Vss			-80	uA
Input impedance	Zi	MIC pin Input freq = 1KHz	20	40		K Ohm
Output impedance	Zo	SPKR pin Output freq = 1KHz		3	10	K Ohm
Peak output voltage range	Vout	SPKR pin			Vdd	Vp-p
Input capacitance	Ci				10	pF
Output capacitance	Co				10	pF
R/C oscillator frequency	Fosc	Cext=47pF Rext=33K Ohm	280		380	KHz
Supply current	Idd	All outputs open			5.0	mA
	Idd	All outputs open Vdd=5V Fosc=492KHz		2.2		mA

IMAGE UNAVAILABLE



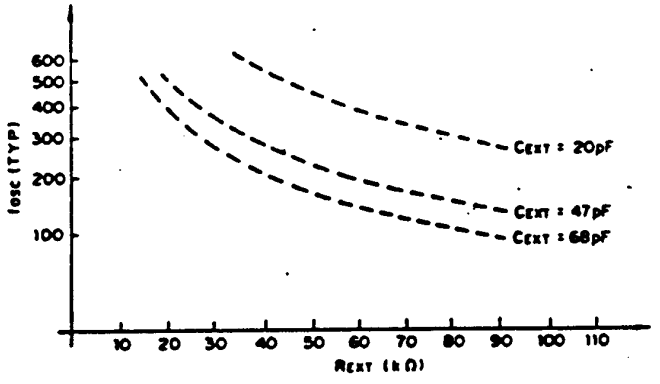
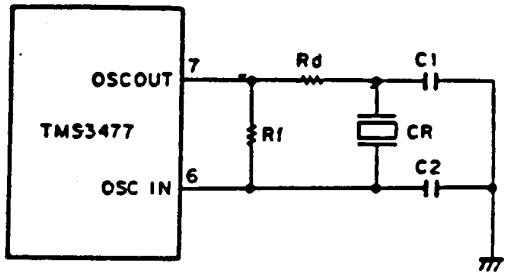


FIG-4 OSCILLATION WITH R/C



CR = CSB320D
Rf = 1M ohm
Rd = 680 ohm
C1 = 330 pF
C2 = 330 pF

FIG-5 OSCILLATION WITH CERAMIC RESONATOR

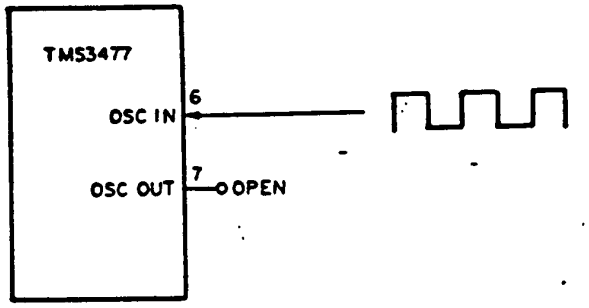


FIG-6 EXTERNAL CLOCK INPUT

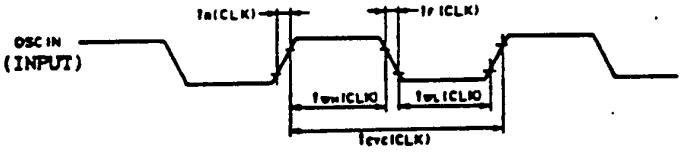


FIG-7 EXTERNAL CLOCK INPUT TIMING

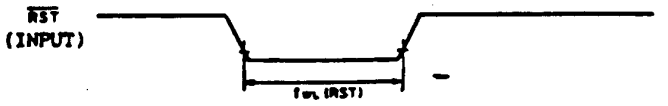
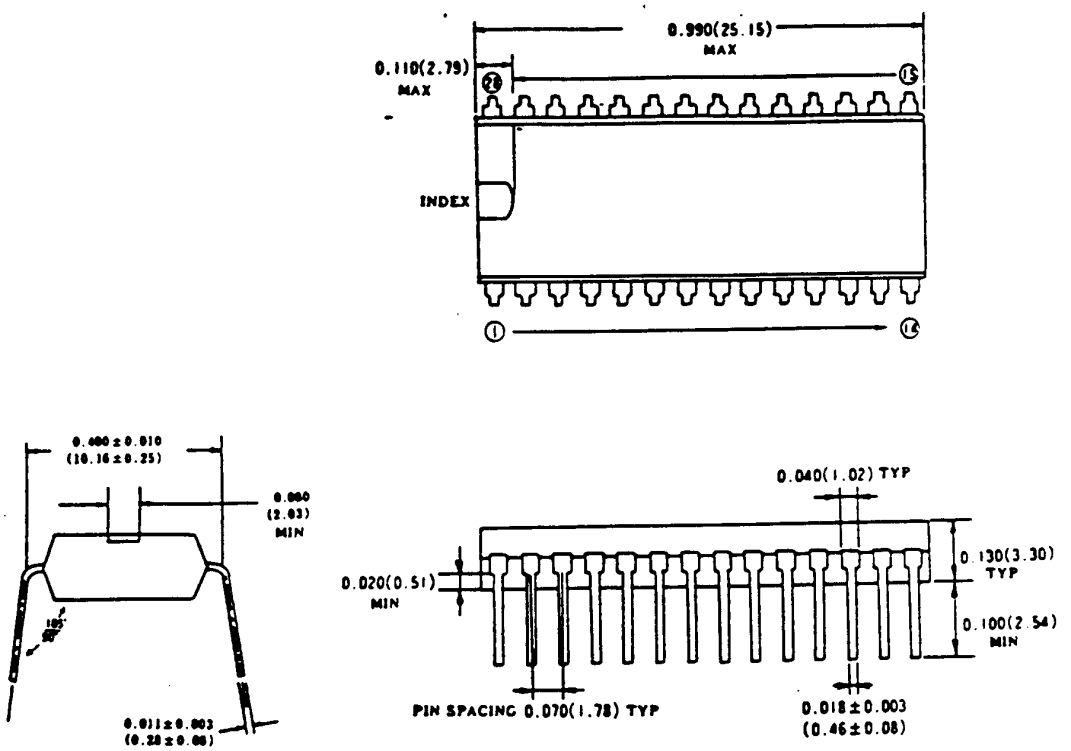


FIG-8 RESET TIMING

IMAGE UNAVAILABLE

MECHANICAL DATA



NOTE: All dimensions are in inches
and parenthetically in millimeters.

FIG-11 TMS3477 PACKAGING (28-PIN SHRINK TYPE DIP)