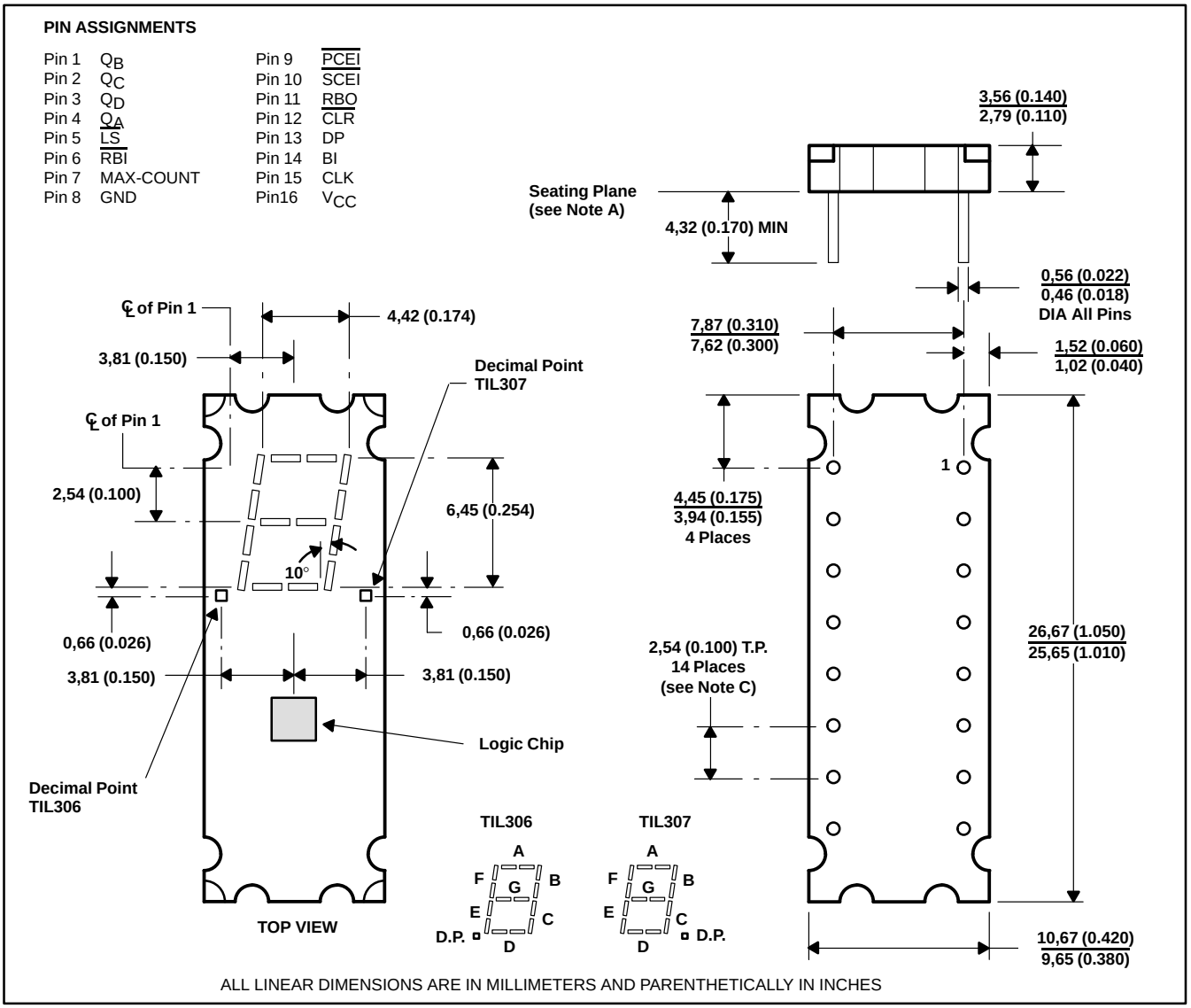
SLBS001 – D1034, JUNE 1982 – REVISED SEPTEMBER 1992

## SOLID-STATE DISPLAYS WITH INTEGRAL TTL MSI CIRCUIT CHIP FOR USE IN ALL SYSTEMS WHERE THE DATA TO BE DISPLAYED IS THE PULSE COUNT

- **6,9-mm (0.270-Inch) Character Height**
- **High Luminous Intensity**
- **TIL306 Has Left Decimal**
- **TIL307 Has Right Decimal**
- **Easy System Interface**
- **Wide Viewing Angle**
- **Internal TTL MSI Chip and Counter, Latch, Decoder, and Driver**
- **Constant-Current Drive for Light-Emitting Diodes**

### mechanical data

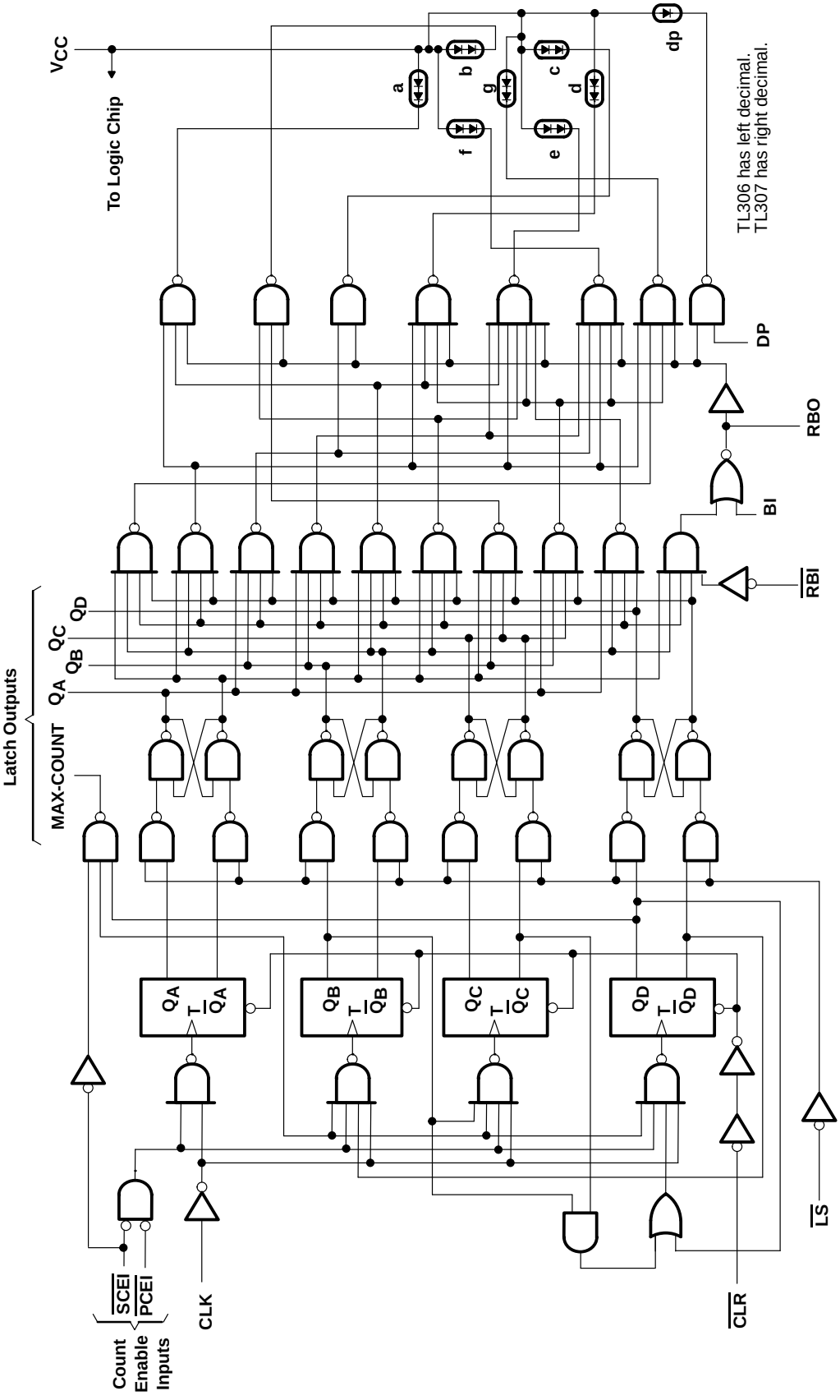
These assemblies consist of display chips and a TTL MSI chip mounted on a header with a red molded plastic body. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Lead dimensions are not controlled above the seating plane.
B. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.
C. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located with 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 16.

## logic diagram




Synchronous BCD counter, 4-bit latch, decoder/driver, seven-segment LED display with decimal point

## description

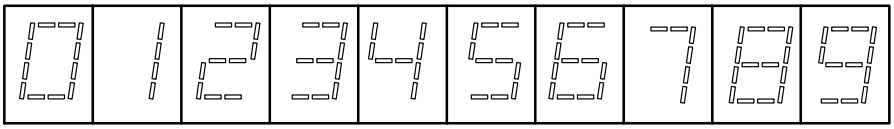
These internally-driven seven-segment light-emitting-diode (LED) displays contain a BCD counter, a four-bit latch, and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices are in the terminal function table.

The TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-carry input, actually two internal loads, is rated as one standard series 54/74 load.

The logic outputs, except RBO, are active pullup, and the latch outputs $Q_A$, $Q_B$, $Q_C$, and $Q_D$ are each capable of driving three standard Series 54/74 loads at a low logic level or six loads at a high logic level while the maximum-count output is capable of driving five Series 54/74 loads at a low logic level or ten loads at a high logic level. The RBO node with passive pull-up serves as a ripple-blanking output with the capability to drive three Series 54/74 loads.

The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately 7 mA through each LED segment and decimal point. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 MHz and power dissipation is typically 600 mW with all segments on.

The display format is as follows:



The displays may be interconnected to produce an n-digit display with the following features:

- Ripple-blanking input and output for blanking leading or trailing zeroes
- Floating-decimal-point logic capability
- Overriding blanking for suppressing entire display or pulse modulation of LED brightness
- Dual count-enable inputs for parallel lookahead and serial ripple logic to build high-speed fully synchronous, multidigit counter systems with no external logic, minimizing total propagation delay from the clock to the last latch output
- Provision for ripple-count cascading between packages
- Positive-edge-triggered synchronous BCD counter
- Parallel BCD data outputs available to drive logic processors or remote slaved displays simultaneously with data being displayed
- Latch strobe input allows counter to operate while a previous data point is displayed
- Reset-to-zero capability with clear input.

**Terminal Functions**

| PIN NAME | PIN NO. | DESCRIPTION |
|---|---|---|
| BLANKING Input (BI) | 14 | When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display. |
| CLEAR Input ($\overline{CLR}$) | 12 | When low, resets and holds counter at 0. Must be high for normal counting. |
| CLOCK Input (CLK) | 15 | Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high). |
| DECIMAL POINT Input (DP) | 13 | Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked. |
| LATCH Outputs ($Q_A$, $Q_B$, $Q_C$, $Q_D$) | 4, 1, 2, 3 | The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A$ = 1, $Q_B$ = 2, $Q_C$ = 4, $Q_D$ = 8. |
| LATCH STROBE Input ($\overline{LS}$) | 5 | When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently. |
| MAX-COUNT Output | 7 | Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high. |
| PARALLEL Count Enable Input ($\overline{PCEI}$) | 9 | Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low. |
| RIPPLE-BLANKING Input ($\overline{RBI}$) | 6 | When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0. |
| RIPPLE-BLANKING Output (RBO) | 11 | Supplies ripple-blanking information for the ripple-blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches is BCD 0; otherwise, this output is high. This pin has a resistive pullup circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low, the entire display will be blanked; therefore, this pin may be used as an active-low blanking input. |
| SERIAL Count Enable Input ($\overline{SCEI}$) | 10 | Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low. |

## absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1): Continuous . . . . . 5.5 V
Nonrepetitive peak, $t_w \leq 100$ ms . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating case temperature range, $T_C$ (see Note 2) . . . . . 0°C to 85°C
Storage temperature range . . . . . –25°C to 85°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | 4.75 | 5 | 5.25 | V |
| Normalilzed fan-out from each output, N (to Series 54/74 integrated circuits) | Low logic level | $Q_A$, $Q_B$, $Q_C$, $Q_D$, RBO | | | 3 | |
| | | MAX-COUNT Output | | | 5 | |
| | High logic level | RBO | | | 3 | |
| | | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 6 | |
| | | MAX-COUNT Output | | | 10 | |
| Clock pulse duration, $t_{w(clock)}$ | | High logic level | 25 | | | ns |
| | | Low logic level | 55 | | | |
| Clear pulse duration, $t_{w(clear)}$ | | | 25 | | | ns |
| Latch strobe pulse duration, $t_{w(latch\ strobe)}$ | | | 45 | | | ns |
| Setup time, $t_{su}$ | PCEI/SCEI↑ before CLOCK↑ | | 30 | | | ns |
| | CLEAR↑ before CLOCK↑ | | 60 | | | |
| Operating case temperature, $T_C$ | | | 0 | | 70 | °C |

## electrical characteristics at 25°C case temperature

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.75 V, | $I_I$ = –12 mA | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | RBO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –120 µA | 2.4 | | | V |
| | | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –240 µA | | | | |
| | | MAX-COUNT Output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –400 µA | | | | |
| $V_{OL}$ | Low-level output voltage (see Note 3) | $Q_A$, $Q_B$, $Q_C$, $Q_D$, RBO | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 4.8 mA | | | 0.4 | V |
| | | MAX-COUNT Output | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 8 mA | | | | |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | SCEI | $V_{CC}$ = 5.25 V, | $V_I$ = 2.4 V | | | 40 | µA |
| | | RBO node | | | –0.12 | –0.5 | | mA |
| | | Other inputs | | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | SCEI | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | | –1.6 | mA |
| | | RBO node | | | | –1.5 | –2.4 | |
| | | Other inputs | | | | | –0.8 | |
| $I_{OS}$ | Short-circuit output current | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | $V_{CC}$ = 5.25 V | | –9 | | –27.5 | mA |
| | | MAX-COUNT Output | | | –15 | | –55 | |
| $I_{CC}$ | Supply current | | $V_{CC}$ = 5.25 V, | See Note 4 | | 120 | 200 | mA |
| $I_v$ | Luminous intensity (see Note 5) | Figure 8 | $V_{CC}$ = 5 V | | 700 | 1200 | | µcd |
| | | DP Input | | | 40 | 70 | | µcd |
| $\lambda_p$ | Wavelength at peak emission | | $V_{CC}$ = 5 V, | See Note 4 | | 660 | | nm |
| $\Delta\lambda$ | Spectral bandwidth | | $V_{CC}$ = 5 V, | See Note 4 | | 20 | | nm |

† All typical values are at $V_{CC}$ = 5 V.

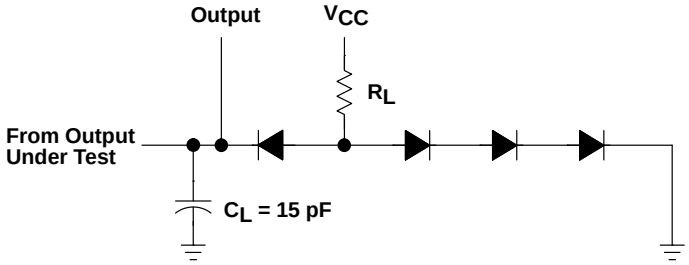
NOTES: 3. This parameter is measured with the display blanked (BI = 5 V).
4. These parameters are measured with all LED segments and the decimal point on.
5. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.

## switching characteristics, $V_{CC}$ = 5 V, $T_C$ = 25°C

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | | 12 | 18 | | MHz |
| $t_{PLH}$ | SERIAL lookahead | MAX-COUNT Output | $C_L$ = 15 pF, $R_L$ = 560 Ω, See Figure 1 | | 12 | | ns |
| $t_{PHL}$ | | | | | 23 | | |
| $t_{PLH}$ | CLK Input | MAX-COUNT Output | | | 26 | | ns |
| $t_{PHL}$ | | | | | 29 | | |
| $t_{PLH}$ | CLK Input | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | $C_L$ = 15 pF, $R_L$ = 1.2 kΩ, See Figure 1 | | 28 | | ns |
| $t_{PHL}$ | | | | | 38 | | |
| $t_{PHL}$ | $\overline{CLR}$ Input | $Q_A$, $Q_B$, $Q_C$, $Q_D$ | | | 57 | | ns |

† $f_{max}$ ≡ Maximum clock frequency
$t_{PLH}$ ≡ Propagation delay time, low-to-high-level output
$t_{PHL}$ ≡ Propagation delay time, high-to-low-level output

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064.

**Figure 1. Load Circuit**

## TYPICAL CHARACTERISTICS

**RELATIVE SPECTRAL CHARACTERISTICS**

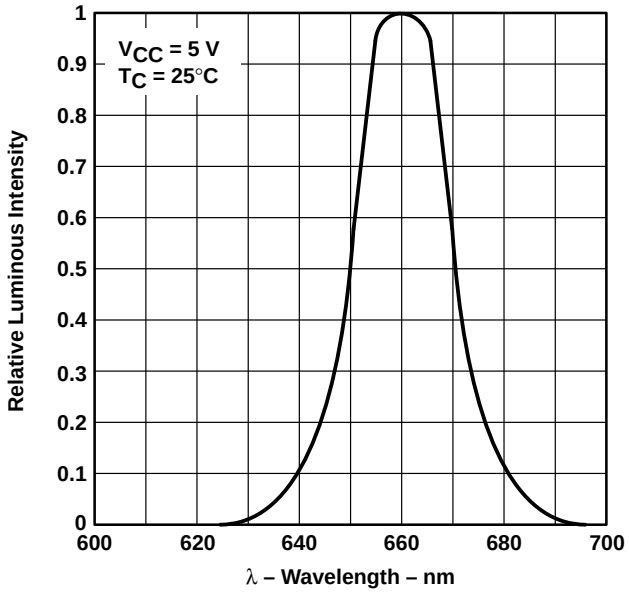



**Figure 2**

**RELATIVE LUMINOUS INTENSITY vs CASE TEMPERATURE**

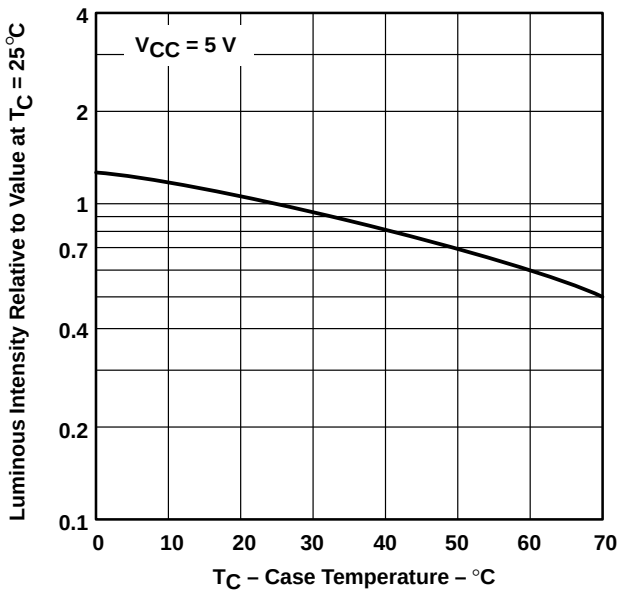



**Figure 3**

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.