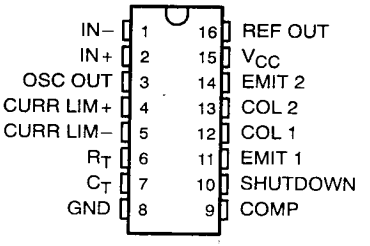
D2294, APRIL 1977–REVISED DECEMBER 1991

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Silicon General SG2524 and SG3524**

**N PACKAGE**
**(TOP VIEW)**

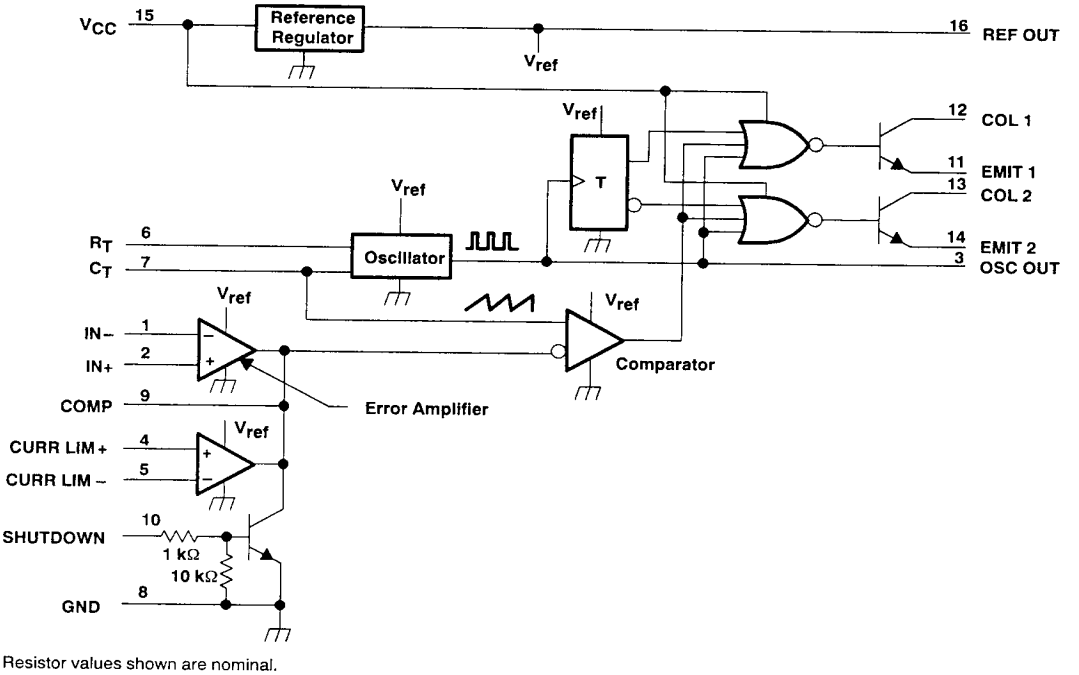



## description

The SG2524 and SG3524 incorporate on single monolithic chips all the functions required in the construction of a regulating power supply, inverter, or switching regulator. They can also be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

The SG2524 is characterized for operation from −25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

## functional block diagram




Resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Notes 1 and 2) ..... 40 V
Collector output current ..... 100 mA
Reference output current ..... 50 mA
Current through $C_T$ terminal ..... −5 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SG2524 ..... −25°C to 85°C
SG3524 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the $V_{CC}$ and reference output pins both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR | DERATE ABOVE $T_A$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|---|
| N | 1000 mW | 9.2 mW/ °C | 41°C | 736 mW | 598 mW |

## recommended operating conditions

| | SG2524 | | SG3524 | | UNIT |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| Supply voltage, $V_{CC}$ | 8 | 40 | 8 | 40 | V |
| Reference output current | 0 | 50 | 0 | 50 | mA |
| Current through $C_T$ terminal | −0.03 | −2 | −0.03 | −2 | mA |
| Timing resistor, $R_T$ | 1.8 | 100 | 1.8 | 100 | kΩ |
| Timing capacitor, $C_T$ | 0.001 | 0.1 | 0.001 | 0.1 | μF |
| Operating free-air temperature | −25 | 85 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 20 V (unless otherwise noted)

### reference section

| PARAMETER | TEST CONDITIONS† | SG2524 | | | SG3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| Output voltage | | 4.8 | 5 | 5.2 | 4.6 | 5 | 5.4 | V |
| Input regulation | $V_{CC}$ = 8 V to 40 V | | 10 | 20 | | 10 | 30 | mV |
| Ripple rejection | f = 120 Hz | | 66 | | | 66 | | dB |
| Output regulation | $I_O$ = 0 mA to 20 mA | | 20 | 50 | | 20 | 50 | mV |
| Output voltage change with temperature | $T_A$ = MIN to MAX | | 0.3% | 1% | | 0.3% | 1% | |
| Short-circuit output current§ | $V_{ref}$ = 0 | | 100 | | | 100 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except output voltage change with temperature, are at $T_A$ = 25°C.
§ Duration of the short circuit should not exceed one second.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 20 V, f = 20 kHz (unless otherwise noted)

### oscillator section

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator frequency | $C_T$ = 0.001 μF, | $R_T$ = 2 kΩ | | 450 | | kHz |
| | Standard deviation of frequency§ | All values of voltage, temperature, resistance, and capacitance constant | | | 5% | | |
| $\Delta f_{osc}$ | Frequency change with voltage | $V_{CC}$ = 8 V to 40 V, | $T_A$ = 25°C | | | 1% | |
| $\Delta f_{osc}$ | Frequency change with temperature | $T_A$ = MIN to MAX | | | | 2% | |
| | Output amplitude at OSC OUT | $T_A$ = 25°C | | | 3.5 | | V |
| $t_w$ | Output pulse duration (width) at OSC OUT | $C_T$ = 0.01 μF, | $T_A$ = 25°C | | 0.5 | | μs |

### error amplifier section

| PARAMETER | | TEST CONDITIONS† | SG2524 | | | SG3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = 2.5 V | | 0.5 | 5 | | 2 | 10 | mV |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | | 2 | 10 | | 2 | 10 | μA |
| | Open-loop voltage amplification | | 72 | 80 | | 60 | 80 | | dB |
| $V_{ICR}$ | Common-mode input voltage range | $T_A$ = 25°C | 1.8 to 3.4 | | | 1.8 to 3.4 | | | V |
| CMMR | Common-mode rejection ratio | | | 70 | | | 70 | | dB |
| $B_1$ | Unity-gain bandwidth | | | 3 | | | 3 | | MHz |
| | Output swing | $T_A$ = 25°C | 0.5 | | 3.8 | 0.5 | | 3.8 | V |

### output section

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(BR)CE}$ | Collector-emitter breakdown voltage | | | 40 | | | V |
| | Collector off-state current | $V_{CE}$ = 40 V | | | 0.01 | 50 | μA |
| $V_{sat}$ | Collector-emitter saturation voltage | $I_C$ = 50 mA | | | 1 | 2 | V |
| $V_O$ | Emitter output voltage | $V_C$ = 20 V, | $I_E$ = −250 μA | 17 | 18 | | V |
| $t_r$ | Turn-off voltage rise time | $R_C$ = 2 kΩ | | | 0.2 | | μs |
| $t_f$ | Turn-on voltage fall time | $R_C$ = 2 kΩ | | | 0.1 | | μs |

### comparator section

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Maximum duty cycle, each output | | 45% | | | |
| $V_T$ | Input threshold voltage at COMP | Zero duty cycle | | 1 | | V |
| | | Maximum duty cycle | | 3.5 | | |
| $I_{IB}$ | Input bias current | | | −1 | | μA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$$

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 20 V, f = 20 kHz (unless otherwise noted)

### current limiting section

| PARAMETER | | TEST CONDITIONS | SG2524 | | | SG3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_I$ | Input voltage range (either input) | | −1 to 1 | | | −1 to 1 | | | V |
| $V_{(sense)}$ | Sense voltage at $T_A$ = 25°C | $V_{(IN+)} - V_{(IN-)} \geq 50$ mV, | 190 | 200 | 210 | 180 | 200 | 220 | mV |
| | Temperature coefficient of sense voltage | $V_{(COMP)}$ = 2 V | | 0.2 | | | 0.2 | | mV/°C |

### total device

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{st}$ | Standby current | $V_{CC}$ = 40 V, IN+ at 2 V, | IN−, CURR LIM+, $C_T$, GND, COMP, EMIT 1, EMIT 2 grounded<br>All other inputs and outputs open | | 8 | 10 | mA |

† All typical values, except for temperature coefficients, are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION

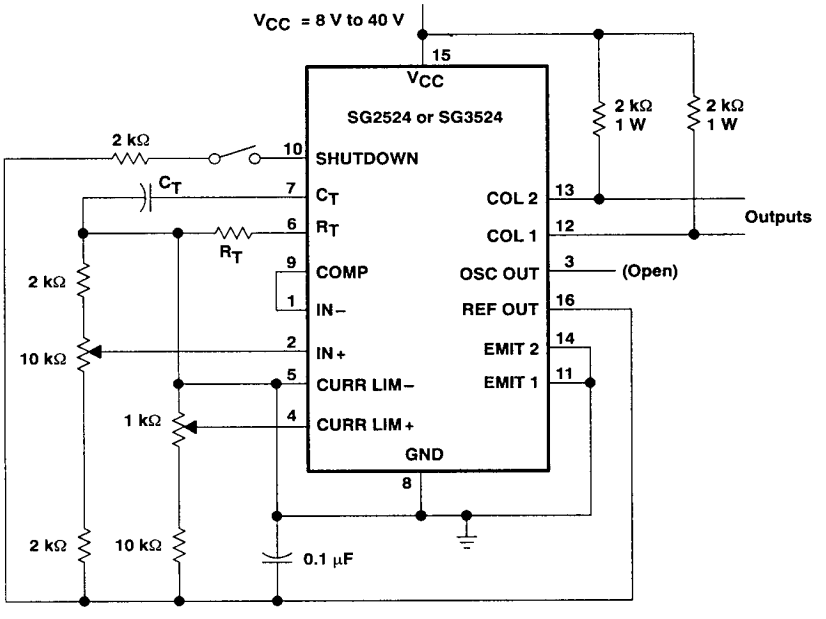



Figure 1. General Test Circuit

## PARAMETER MEASUREMENT INFORMATION

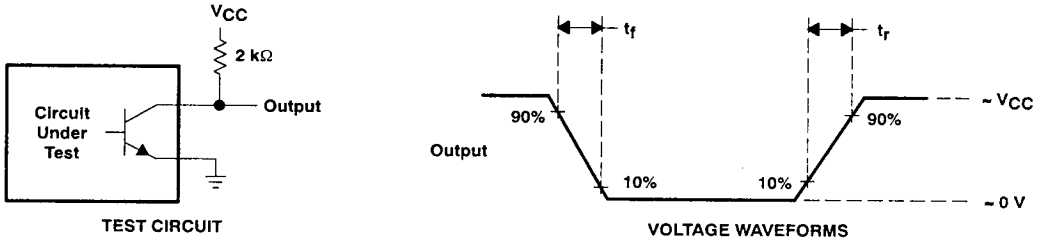



Figure 2. Switching Times

## TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION OF ERROR AMPLIFIER vs FREQUENCY

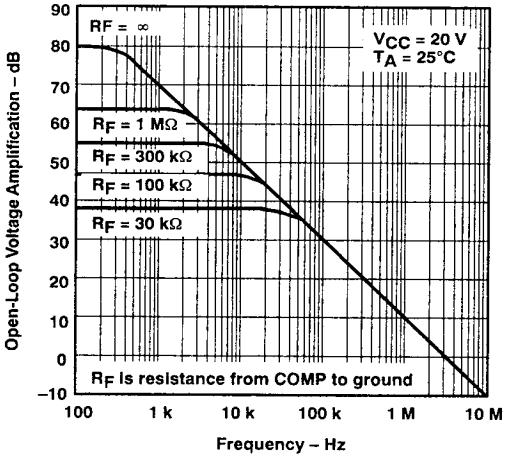



Figure 3

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

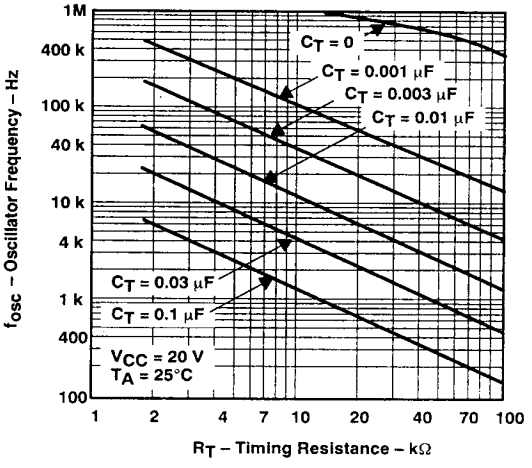



Figure 4

## TYPICAL CHARACTERISTICS

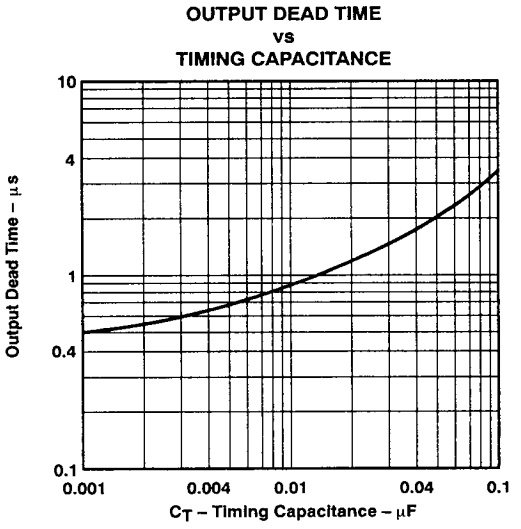



Figure 5

## PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor $R_T$ and one timing capacitor $C_T$. $R_T$ establishes a constant charging current for $C_T$. This results in a linear voltage ramp at $C_T$, which is fed to the comparator providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an on-board 5-V regulator that serves as a reference as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference may be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at $C_T$. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of $C_T$. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, to compensate the error amplifier, or to provide additional control to the regulator.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### oscillator

The oscillator controls the frequency of the SG2524 and is programmed by $R_T$ and $C_T$ as shown in Figure 4.

$$f \approx \frac{1.30}{R_T\ C_T}$$

where $R_T$ is in kΩ
$C_T$ is in μF
f is in kHz

Practical values of $C_T$ fall between 0.001 and 0.1 μF. Practical values of $R_T$ fall between 1.8 and 100 kΩ. This results in a frequency range typically from 140 Hz to 500 kHz.

### blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of $C_T$ as shown in Figure 5. If small values of $C_T$ are required, the oscillator output pulse duration may still be maintained by applying a shunt capacitance from OSC OUT to ground.

### synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, $R_T$ $C_T$ must be selected for a clock period slightly greater than that of the external clock.

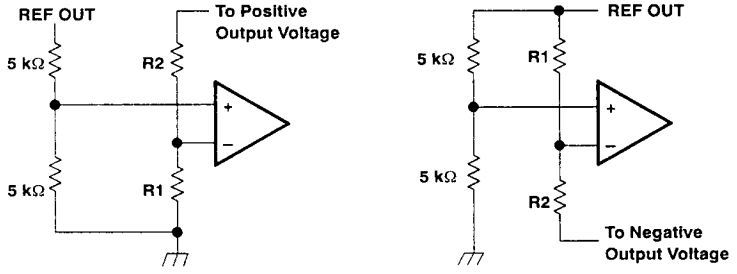
If two or more SG2524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other SG2524s operate. In this application, the $C_T$ $R_T$ values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, $C_T$ (master) = 2 $C_T$ (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and will subsequently reset the slave regulators.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### voltage reference

The 5-V internal reference may be employed by use of an external resistor divider network to establish a reference within the error amplifiers common-mode voltage range (1.8 V to 3.4 V) as shown in Figure 6, or an external reference may be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference may be bypassed by applying the input voltage to both the $V_{CC}$ and $V_{REF}$ terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.




$$V_O = 2.5\ V \frac{R1 + R2}{R1} \qquad \frac{R1\ R2}{R1 + R2} = 2.5\ k\Omega$$

**Figure 6. Error Amplifier Bias Circuits**

### error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node ($R_L$ = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

### compensation

COMP, as discussed above, is made available for compensation. Since most output filters will introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 μF. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

### shut-down circuitry

COMP can also be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and thus disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM– may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM– may also be grounded to convert CURR LIM+ into an additional shut-down terminal.

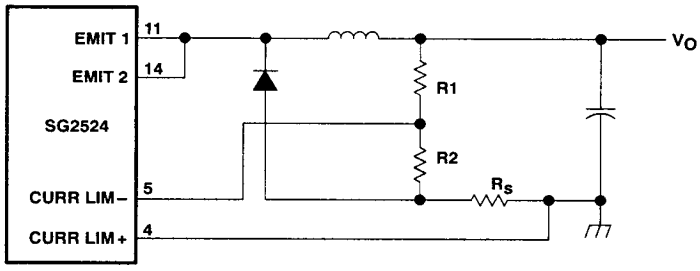
† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV and must be applied in the ground line since the voltage range of the inputs is limited to +1 V to −1 V. Caution should be taken to ensure the −1 V limit is not exceeded by either input, otherwise damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.




$$I_{O(max)} = \frac{1}{R_S}\left( V_{(sense)} + \frac{V_O\ R2}{R1 + R2} \right)$$

$$I_{OS} = \frac{V_{(sense)}}{R_S} \text{ where } V_{(sense)} = 20 \text{ mV}$$

**Figure 7. Foldback Current Limiting for Shorted Output Conditions**

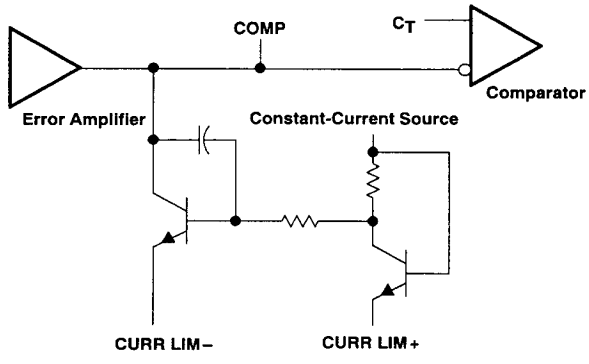



**Figure 8. Current-Limit Schematic**

### output circuitry

The SG2524 contains two identical n-p-n transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

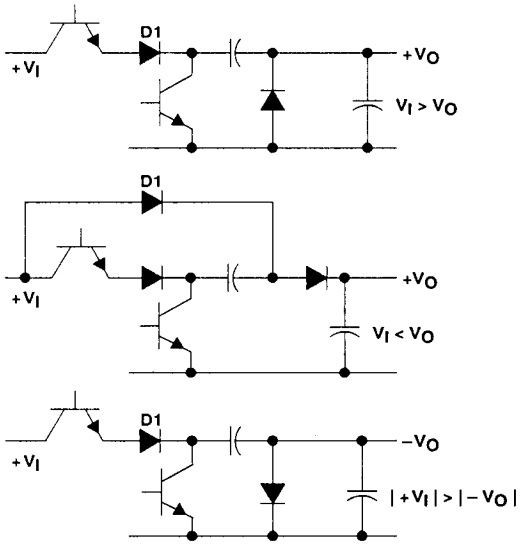



**Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages**

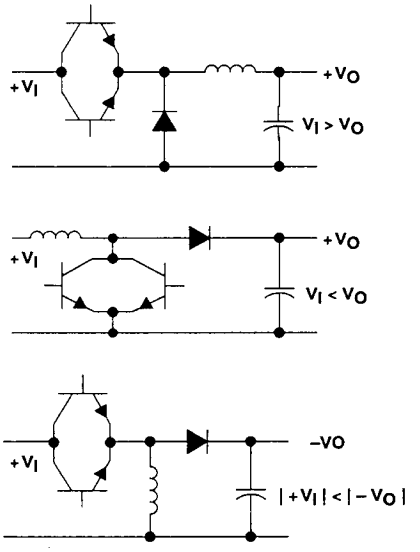



**Figure 10. Single-Ended Inductor Circuit**

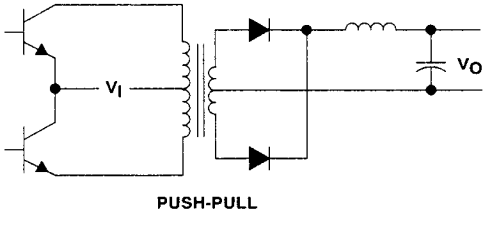



**Figure 11. Transformer-Coupled Outputs**

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

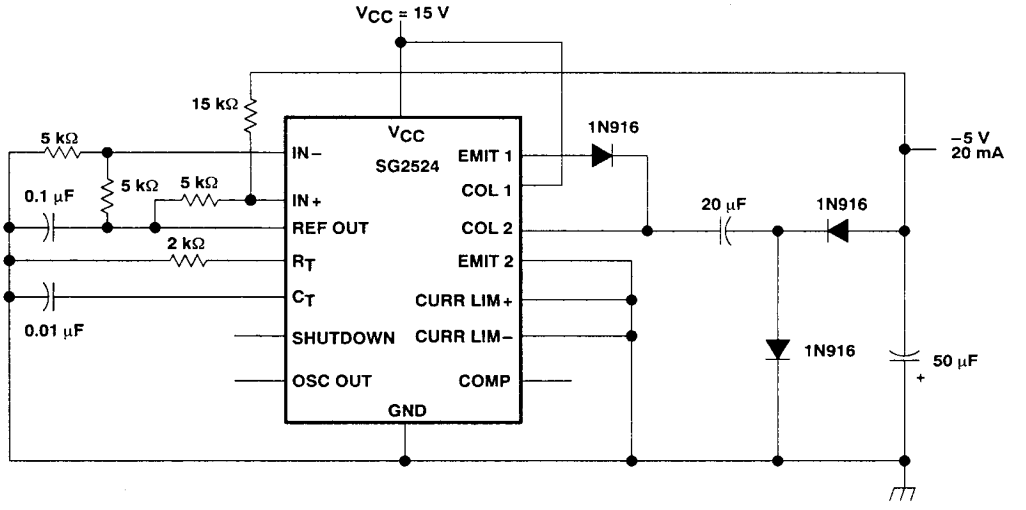



**Figure 12. Capacitor-Diode Output Circuit**

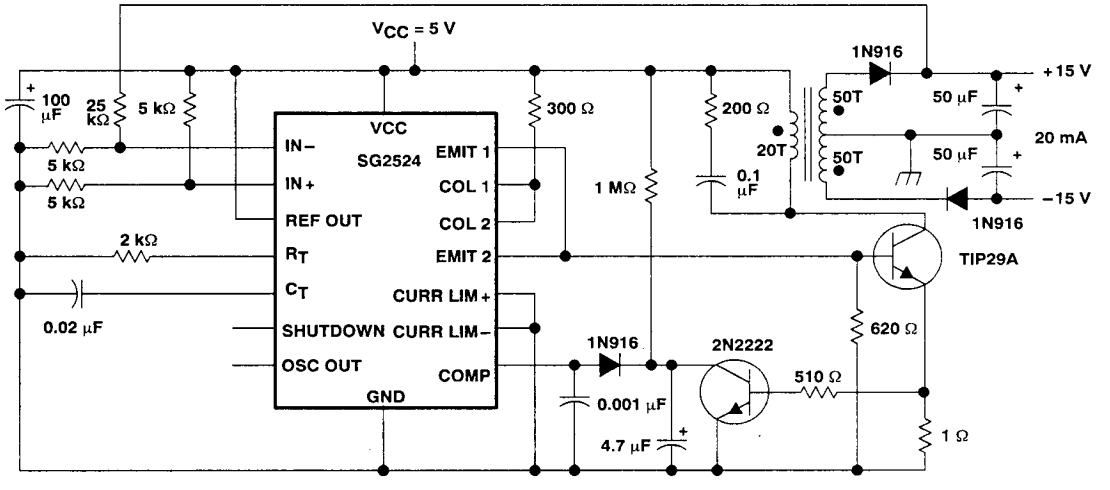



**Figure 13. Flyback Converter Circuit**

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

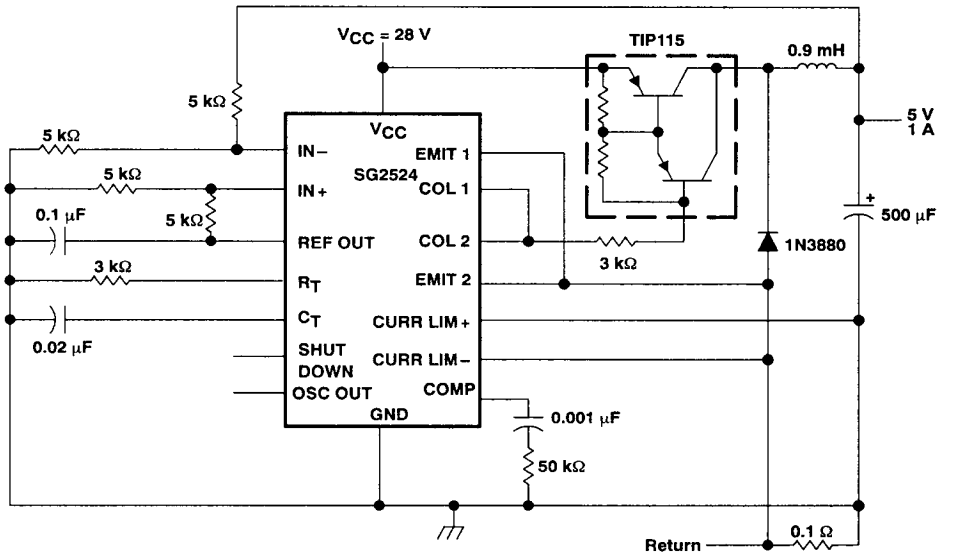



**Figure 14. Single-Ended LC Circuit**

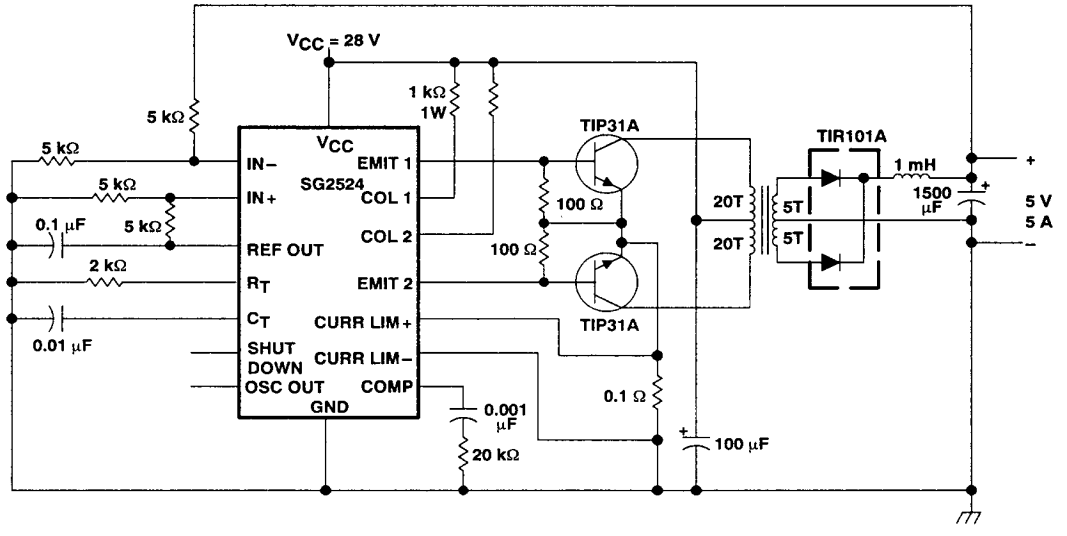



**Figure 15. Push-Pull Transformer-Coupled Circuit**

† Throughout these discussions, references to the SG2524 apply also to the SG3524.