

# ***Interface Circuits for TIA/EIA-485***

## *Design Notes*

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# Contents

<b>The Need for Balanced Transmission-Line Standards</b> .....	<b>1</b>
<b>Process-Control Design Example</b> .....	<b>2</b>
<b>Line Loading</b> .....	<b>3</b>
Signal Attenuation .....	5
Fault Protection and Fail-Safe Operation .....	6
Galvanic Isolation .....	11
<b>Eye Patterns</b> .....	<b>14</b>
Setting Up the Eye Pattern .....	14
Taking Measurements from Eye Patterns .....	16

## List of Figures

1 485 Specification Highlights .....	2
2 Process-Control Design Example .....	3
3 The Unit Load Concept .....	4
4 Signal Attenuation .....	5
5 485 Signal Distortion vs Signaling Rate .....	6
6 Input Protection for Noisy Environments .....	6
7 Integrated Transient Voltage Protection for Noisy Environments .....	7
8 External 485 Fail-Safe Circuits .....	9
9 Short-/Open-Circuit Fail Safe .....	10
10 Isolated 485 Node With the SN75LBC176 .....	13
11 Signal Distortions Using Eye Patterns .....	14
12 Eye Pattern Oscilloscope Trace .....	15
13 NRZ Random Code Generator .....	15
14 Measuring Signal Transmission Quality .....	16



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# ***Interface Circuits for TIA/EIA-485***

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## **ABSTRACT**

This design note provides information concerning the design of TIA/EIA-485 interface circuits. The document discusses the need for balanced transmission-line standards and gives an example for a process-control design. Line loading is discussed with subtopics of signal attenuation, fault protection, and galvanic isolation. Finally, setting up and measuring using eye patterns is documented. Eye patterns are used to measure the effects of signal distortion, noise, signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system.

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## **The Need for Balanced Transmission-Line Standards**

This document focuses on the industry's most widely used balanced transmission-line standard, the ANSI/TIA/EIA-485-A (referred to hereafter as 485). After reviewing some key aspects of the 485 standard you are introduced to the practicalities of implementing a differential transmission configuration based on a factory automation example. Finally, new additions to TI's 485 product line are discussed along with their application, where appropriate.

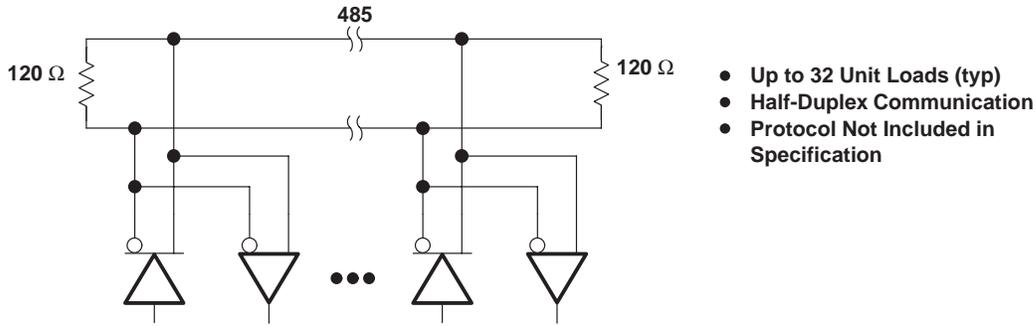
Data transmission between computer-system components and peripherals over long distances and under high-noise conditions usually proves to be very difficult, if not impossible, with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long-line system requirements.

The 485 is a balanced (differential) digital transmission line interface developed to incorporate and improve upon the advantages of the current-loop configuration and improvements to 232 limitations. The advantages are:

- Signaling rate – up to 50 Mbit/s
- Longer line length – up to 1200 meters
- Differential transmission – fewer noise emissions
- Multiple drivers and receivers

Data transmission circuits employing 485 drivers, receivers, or transceivers are used in practically any application requiring an economical, rugged inter-connection between two or more computing devices. A typical application could be using 485 signaling between point-of-sales terminals and a central computer for automatic stock debiting. The low-noise coupling of balanced signaling with twisted-pair cabling and the wide common-mode voltage range of 485 allow data exchange at data signaling rates up to 50 Mbit/s or to distances of several kilometers at lower rates.

As a result of its versatility, an increasing number of standards committees are embracing the 485 standard as the physical layer specification of their communications standard. Examples include the ANSI (American National Standards Institute) small computer systems interface (SCSI) that is featured in the *Interface Circuits for SCSI Applications Report* (Literature Number SLLA035), the Profibus standard, and the DIN Measurement Bus.



KEY PARAMETERS	SPECIFICATION LIMITS
Maximum common-mode voltage	-7 V to 12 V
Receiver input resistance	12 kΩ minimum
Receiver sensitivity	±200 mV
Driver load	60 Ω
Driver output short-circuit limit	250 mA to -7 V to 12 V

**Figure 1. 485 Specification Highlights**

The balanced transmission-line standard 485 was developed in 1983 to interface a host computer's data, timing, or control lines to its peripherals. The standard specifies the physical layer only. Protocols, timing, serial or parallel data, and connector choice are all left to be defined by the designer.

The 485 originally was defined as an upgrade to and a more flexible version of 422. Where 422 facilitates simplex communication only, 485 allows for multiple drivers and receivers on a single line, facilitating half-duplex communication. Like 422 the maximum line length is not specified, but is based on 24-AWG cable; it is nominally around 1.2 km. Maximum signaling rate is unlimited and is set by the ratio of rise time to bit time, similar to 232. In many cases it is the length of the cable that limits the signaling rate more than the drivers, due to transmission line effects and noise.

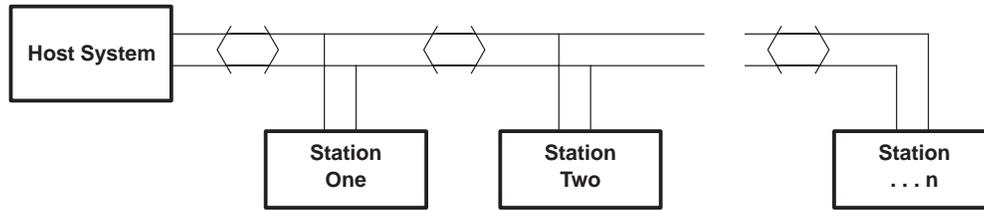
The differences between 485 and 422 lie primarily in the driver features that allow reliable multipoint communications.

## Process-Control Design Example

To gain more knowledge in the design of a 485 system it may be beneficial to take a look at a specific example. In this case, consider a factory automation system with a host controller and several out-stations. Each out-station is capable of transmitting as well as receiving data.

The system has the following features, and a general system specification is shown in Figure 2.

- Furthest out-station is 500 m from the host controller.
- Requires up to 31 out-stations on the line (with the host controller, a total of 32 stations).
- System signaling rate is 500 kbit/s.
- Only one signal pair is used for data transmission operating in half-duplex mode.



- |   |          |  |
|---|----------|--|
| <p><b>Considerations:</b></p> <ul style="list-style-type: none"> <li>• Signal Attenuation</li> <li>• Line Loading</li> <li>• Cable Choice</li> <li>• Fault Protection</li> <li>• Stub Lengths</li> <li>• Termination</li> </ul> | <p>→</p> | <p><b>System Specifications:</b></p> <ul style="list-style-type: none"> <li>• 500 m Furthest Station</li> <li>• 32 Stations</li> <li>• 500 kbit/s</li> <li>• Asynchronous Half-Duplex Communication</li> </ul> |
|---|----------|--|

**Figure 2. Process-Control Design Example**

## Line Loading

The 485 takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether or not to terminate the line is system dependent and is affected by the choice of the maximum line length and signaling rate.

**Line Termination** — The test for whether a transmission line is to be considered as a distributed parameter model or a lumped parameter model is dependent upon the relationship of signal transition time,  $t_t$ , at the driver output and the propagation time,  $t_{pd}$ , of the signal down the cable.

If the relationship  $2t_{pd} \leq 5/t_t$  is true, then the transmission line must be treated as a distributed parameter model and terminated accordingly.

If the opposite is true, then

$$2t_{pd} \geq \frac{t_t}{5} \text{ is true and}$$

the transmission line can be treated as a lumped-parameter model and termination is not necessary.

To transmit data at the design goal of 500 kbit/s and comply with 485, the input transition time can be no more than 0.3 times the unit interval (UI). This establishes an upper limit on the transition time of:

$$t_t \leq 0.3 \times \text{UI}$$

$$t_t \leq 0.3 \left( \frac{1}{500 \times 10^3} \right)$$

$$t_t \leq 60 \times 10^{-9} \text{ s}$$

If a cable with a phase velocity equal to that of the speed of light in a vacuum could be obtained, the propagation delay of the cable would be 3.33 ns/m multiplied by 500 m or 1,665 ns. Using the criteria for determining that there is a transmission line:

$$2t_{pd} \geq \frac{t_t}{5}$$

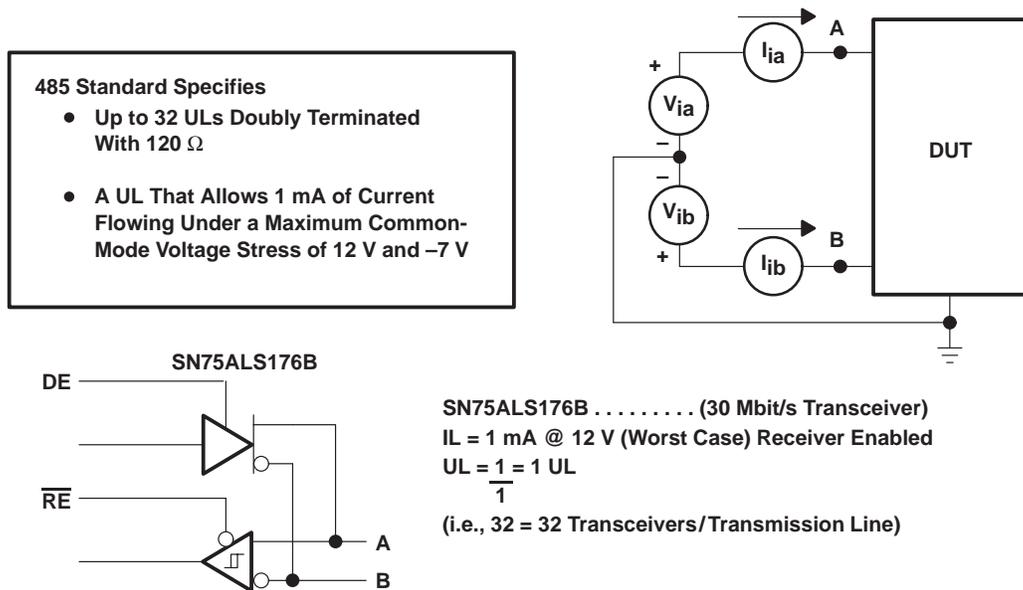
$$3,333 \geq 12$$

With the slowest possible signal transition and the fastest phase velocity, there is a transmission line. Using real-world components would only substantiate the fact that our 500-m half-duplex transmission line must be terminated at both ends.

**The Unit Load Concept** — The maximum number of drivers and receivers that can be placed on a single 485 communication bus depends upon their loading characteristics relative to the definition of a unit load (UL). The 485 standard recommends a maximum of 32 ULs per line.

One UL (at worst case) is defined as a load allowing 1 mA of current under a maximum common-mode voltage stress of 12 V or 0.8 mA at -7 V. ULs may consist of drivers and/or receivers and fail-safe resistors, but they do not include the ac termination resistors.

The example in Figure 3 shows a UL calculation for the SN75ALS176B. Since this device is connected internally as a transceiver (i.e., driver output and receiver input connected to the same bus) it is difficult to obtain separate driver leakage and receiver input currents. For this calculation, reference is made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 UL, which allows up to 32 devices to be connected to the line.

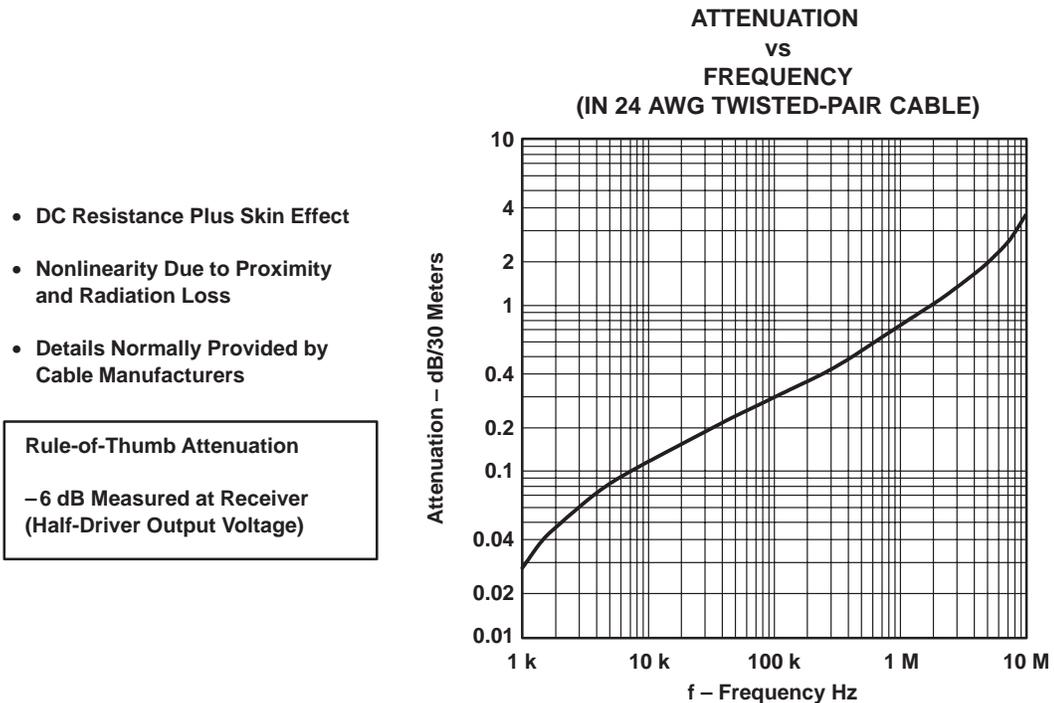


**Figure 3. The Unit Load Concept**

As long as (all) the receiver's input resistance is greater than the 12 kΩ, thus preventing loading of the line, it is possible to connect more than 32 receivers.

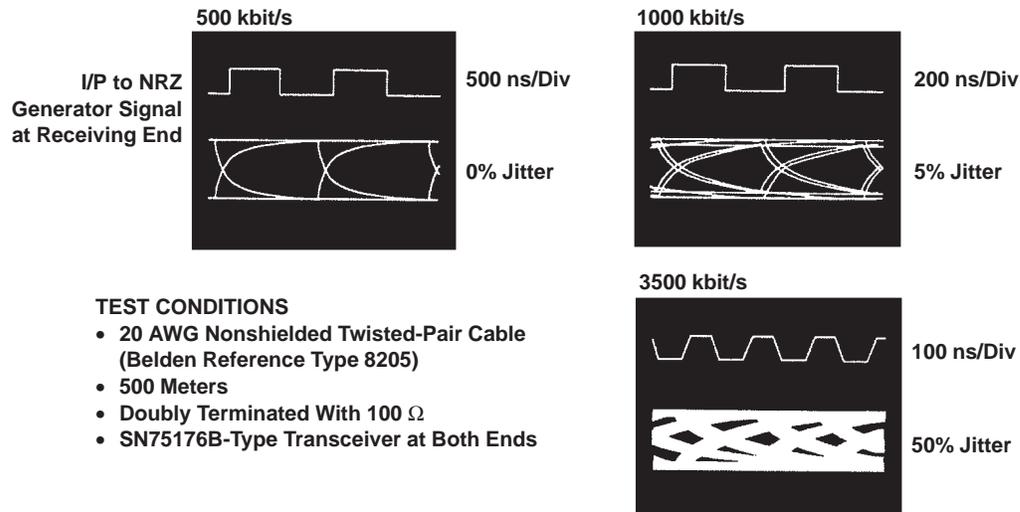
## Signal Attenuation

A rule of thumb for allowable attenuation is  $-6$  dB at the maximum signaling rate in Hz. Although the fundamental frequency of a 500 kbit/s signaling rate is 250 kHz, the attenuation is chosen at 500 kHz to include the high-frequency components of the signal. Attenuation figures usually are supplied by cable manufacturers. The curve in Figure 4 shows the attenuation change versus frequency for a 24-AWG cable. For 500 meters of cable and using 6-dB rule, the maximum attenuation that can be tolerated is 0.36 dB/30 meters. As shown in the graph on Figure 4, the attenuation is a little over 0.5 dB/30m, exceeding the design constraint by 0.14 dB/30m. This is acceptable, operating at slightly less noise margin than the conservative rule of thumb provides.



**Figure 4. Signal Attenuation**

The simplest way to determine the effects of random noise, jitter, attenuation, and dispersion is with the use of eye patterns. For information on how to set up eye patterns, refer to section *Eye Patterns* in this document. Figure 5 shows the distortion of the signal at the receiving end of 500 meters of 20 AWG twisted-pair cable at different signaling rates. When the signaling rate is increased further, the effects of jitter then become noticeable. In this case, at 1 Mbit/s, there is a 5% jitter. At 3.5 Mbit/s the signal begins to be lost completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system is generally held to less than 5%.

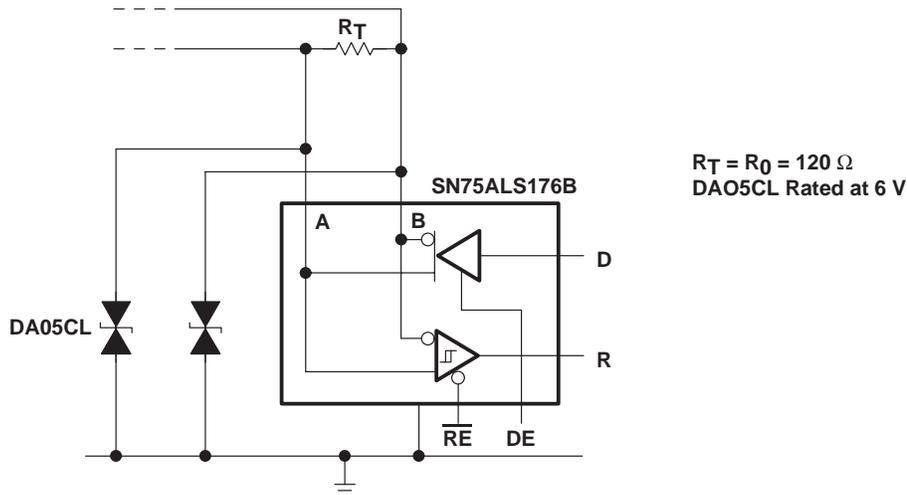


**Figure 5. 485 Signal Distortion vs Signaling Rate**

### Fault Protection and Fail-Safe Operation

**Fault Protection** — As with any system design, consideration should be given to the natural and induced environmental conditions to be encountered during operation. Factory-controlled applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential transmission scheme, and, in particular, the wide common-mode voltage range of 485, may be insufficient. Protection can be accomplished in a number of ways, the most effective being through galvanic isolation, which is discussed later. Galvanic isolation provides good system-level protection but results in higher cost. A more popular and less-expensive solution is the use of protection diodes. The tradeoff using the diode approach over galvanic isolation is a lower level of protection. Examples of external and integrated transient protection diodes are given in the following figures:

Figure 6 shows how external diodes offer transient spike protection for the 485 transceiver, SN75ALS176.

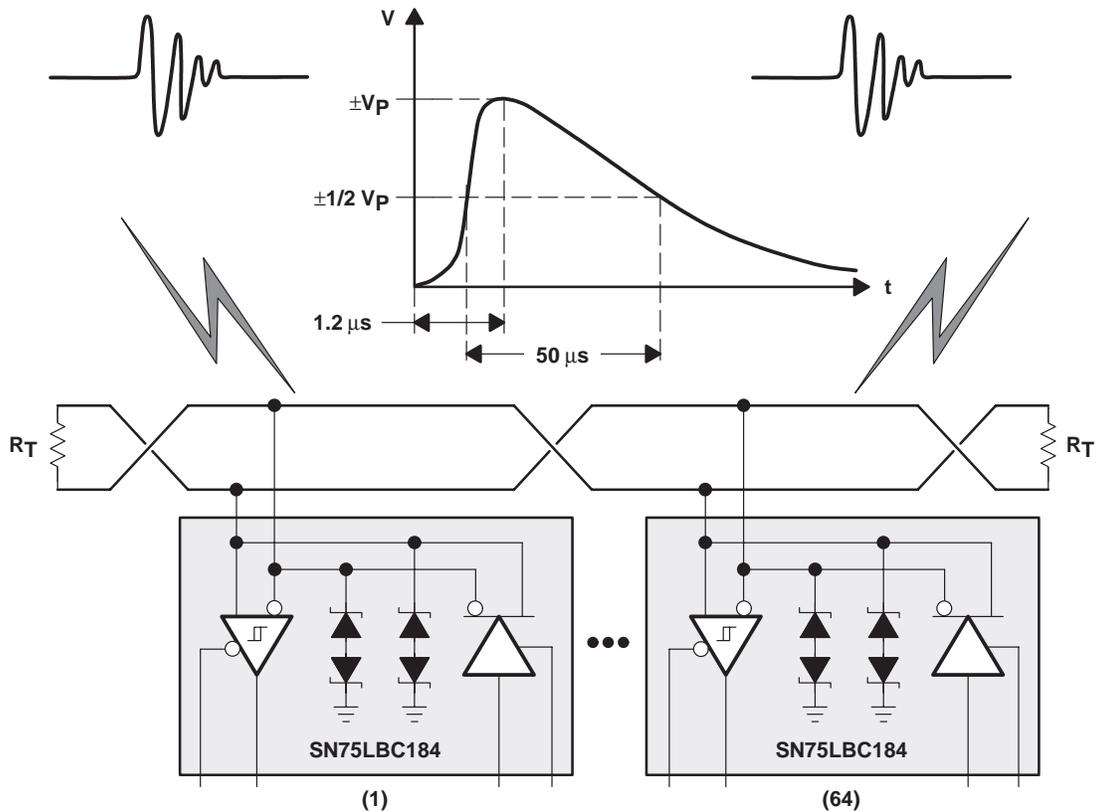


**Figure 6. Input Protection for Noisy Environments**

$R_T$  is the usual termination resistance and is equivalent in value to the characteristic impedance of the line.

DA05CL was selected to protect the transceiver from both positive and negative voltage spikes, which could be seen at the bus pins during an electrical overstress. The peak voltage at the peak current rating of the DA05CL should be less than the absolute maximum ratings of the device.

Figure 7 shows integrated transient suppression diodes for those applications where board space is a premium. The SN75LBC184 ('LBC176 footprint) offers built-in protection against high-energy transients for electrically noisy environments.



- Transceiver with integrated transient suppression
- Protects against pulses of 400 W peak
- 250-kbit/s in electrically noisy environment
- Slew rate controlled for longer stub lengths

**Figure 7. Integrated Transient Voltage Protection for Noisy Environments**

**Fail-Safe Operation** — The feature of fail-safe protection also is a requirement in many 485 applications; however, its usefulness needs to be considered and understood at an application level.

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**The Need For Fail-Safe Protection** — In any party-line interface system with multiple driver/receivers, there are long periods of time when the driving devices are inactive. This state is known as line idle and occurs when the drivers place their outputs into a high-impedance state. During line idle, the voltage along the line is left floating (i.e., indeterminate – neither logic-high nor logic-low state). As a result, the receiver can be falsely triggered into either a logic-high or logic-low state, depending on the presence of noise and the last polarity of the floating lines. Obviously, this is undesirable, as the circuitry following the receiver could interpret this as valid information. It is best to detect such a situation and place the receiver outputs into a known and predetermined state. The name given to methods that ensure this condition is fail safe. An additional feature that a fail safe should provide is to protect the receiver from shorted line conditions, which can again cause erroneous processing of data.

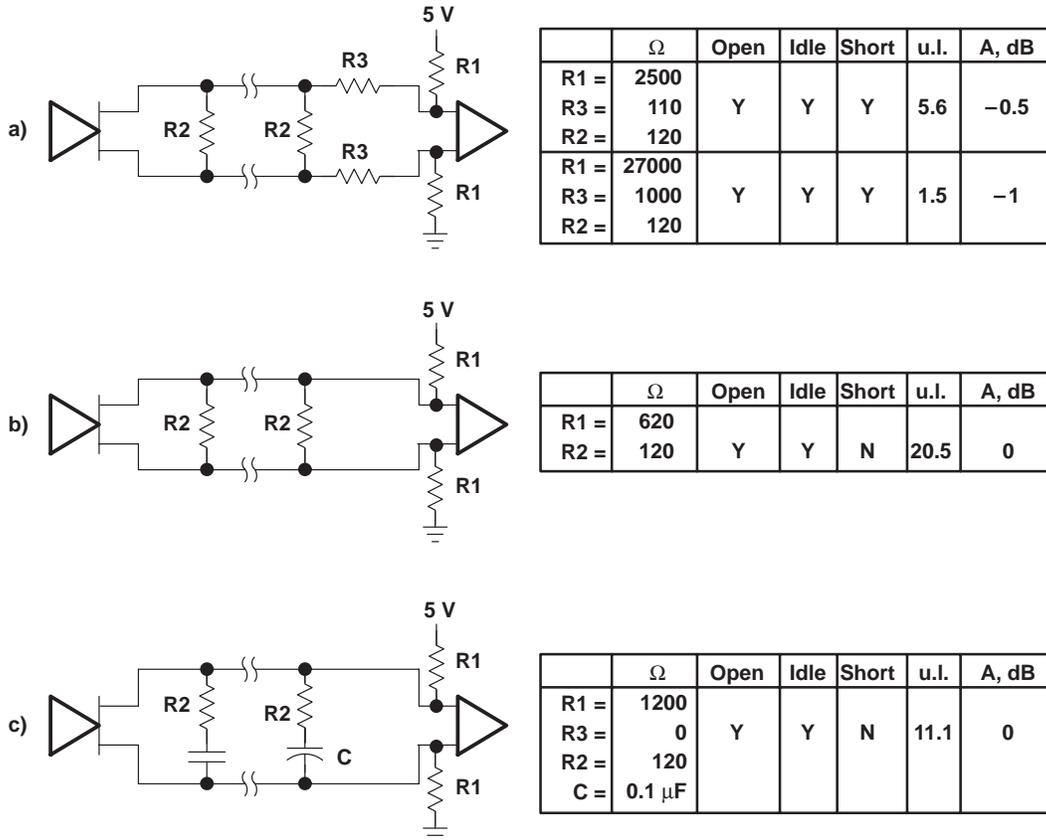
There are several ways to implement a fail safe, including a hard-wired fail safe using protocols on line bias resistors. Protocols, although complicated to implement, are the preferred method. However, since most system designers, hardware designers in this case, prefer to implement such functions in hardware, a hard-wired fail safe most often is implemented.

A hard-wired fail safe should provide a defined voltage across the receiver's input, regardless of whether the signal pair is shorted together or is left open circuited. The fail safe also should be incorporated into the line termination, if present, when at the extremes of the line.

**Internal Fail Safe** — Manufacturers have begun to facilitate fail-safe design by including some form of open-line fail-safe circuitry within the integrated circuits. Quite often, the extra circuitry is just a large pullup resistor on the noninverting receiver input and a large pulldown resistor on the inverting input of the receiver. These resistors normally are in the range of 100 k $\Omega$  and, when used in conjunction with line-termination resistors (typically 50  $\Omega$  to 100  $\Omega$ ) to form a potential divider, only a few millivolts are generated differentially. As a result, this voltage (receiver threshold voltage) is insufficient to assume the receiver state. To use these internal resistors effectively means no line-termination resistors can be used, which reduces the allowed reliable signaling rate significantly.

**External Fail Safe for Open-Line and Terminated Conditions** — Figure 8 shows some common circuits used to provide an external hard-wired fail safe for a 485 interchange circuit. The purpose of each is to maintain a voltage at the receiver inputs above the minimum input threshold and a known logic state under one or more of three fault conditions. In each, R2 represents the resistors for impedance matching of the transmission line and becomes part of a voltage divider creating the steady-state bias voltage. Each receiver is assumed to represent one UL.

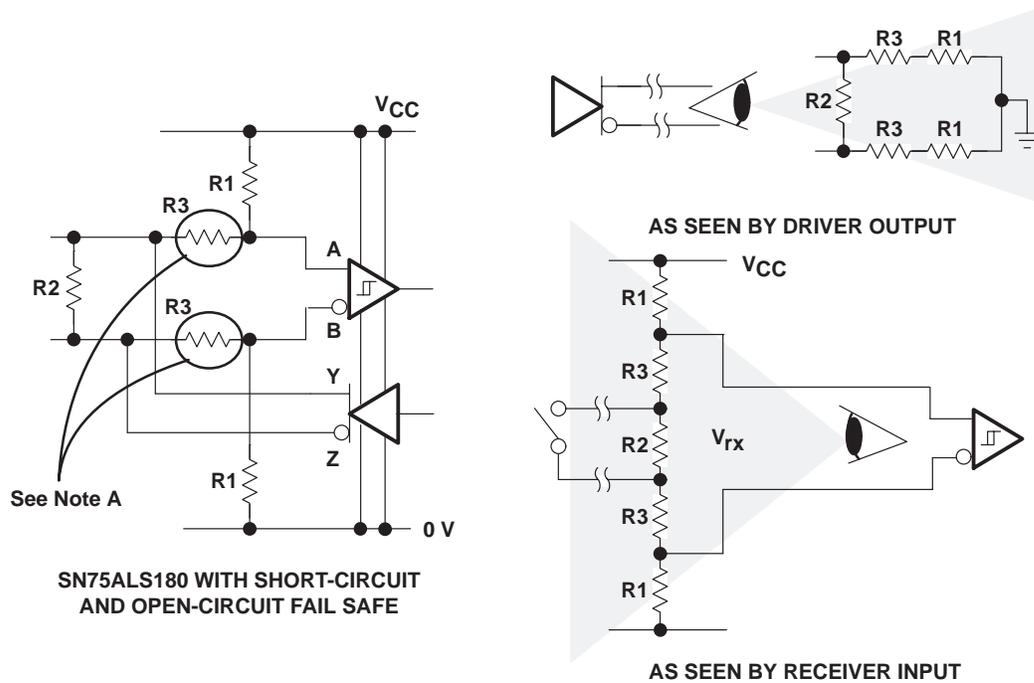
The tables to the right of the schematics indicate some typical resistor or capacitor values, the types of fail safe provided, the number of ULs used, and the signal attenuation. The next section goes through the resistance value calculations for the shorted-line fail-safe circuit for some insight on how the values can be modified for a particular design.



**Figure 8. External 485 Fail-Safe Circuits**

**External Fail Safe With Shorted-Line Conditions** — To implement protection from the shorted-line condition, more resistors are required. When the line is shorted, the transmission line's impedance goes to zero and the termination resistors also are shorted. Putting extra resistors in series with the input to the receiver provides shorted-line fail-safe protection.

The extra resistors R3 in Figure 9 can be added only when using devices with separate driver outputs and receiver inputs. Internally wired transceivers cannot be used for shorted-line fail safe. If this form of protection is required, then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver-type of device is used, then the extra R3 resistors would cause extra attenuation of the output signal. The 'ALS180 has its driver outputs fed directly to the line, then bypassing the R3 resistors.



NOTE A: Cannot implement short-circuit fail safe with SN75176 type transceiver

**Figure 9. Short-/Open-Circuit Fail Safe**

**Calculating The Resistor Values** — If the line becomes shorted, R2 is removed from the circuit, leaving a voltage across the receiver inputs of:

$$V_{ID} = V_{CC} \times \frac{2R3}{2R1 + 2R3}$$

For 485 applications, the standard specifies the maximum input voltage threshold ( $V_{IT}$ ) to be less than 200 mV. So, a known state can be assumed when  $V_{ID} > V_{IT}$  or  $V_{ID} > 200$  mV. This condition becomes the first design constraint.

$$V_{CC} \times \frac{2R3}{2R1 + 2R3} > 200 \text{ mV} \tag{1}$$

When the line goes into a high-impedance state, the receiver sees the two R3s in series, with R2 plus the two R1s pulling up and down on either input. The receiver input voltage is now:

$$V_{ID} = V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3}$$

This gives the second design constraint:

$$V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3} > 200 \text{ mV} \tag{2}$$

The transmission line sees an effective line-termination resistance, R2, in parallel with twice the sum of R1 and R3. This should match the transmission line's characteristic impedance,  $Z_0$ , and therefore provides a third constraint of:

$$Z_0 = 2R2 \times \frac{R1 + R3}{2R1 + R2 + 2R3} \tag{3}$$

---

Other design constraints include the additional line loading presented by the fail-safe circuit and the attenuation caused by R3, R1, and the input resistance of the receiver.

## Galvanic Isolation

Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer. A proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground-loop currents from data lines; and, hence, the impressed noise voltage that affects the signal also are eliminated. Common-mode noise effects can be removed completely and many forms of radiated noise can be reduced to negligible limits using this technique.

For example, consider the case of a process control system where the interface node, shown in Figure 10, connects between a data logger and host computer via a 485 link.

When an adjacent electric motor starts up, a momentary difference in ground potentials at the data logger and at the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and, in the worst case, damage to the computer could occur.

**Circuit Description:** The schematic shown in Figure 10 forms a one-node interface for a distributed controlling, regulating, and supervision (DSCRS) system. Such a scheme can be used in a process control application. Transmission takes place via a two-wire bus, formed by a twisted-pair and ground wire with an overall shield connected in a ring. Low power is useful in this type of application, because many remote outstations are either battery operated or require battery backup capability. In addition, with low power, the isolation transformer can be very small. The bus driver shown in Figure 10 is the SN75LBC176, which has very low power consumption. Of course, other drivers could be used, such as any LVDS device.

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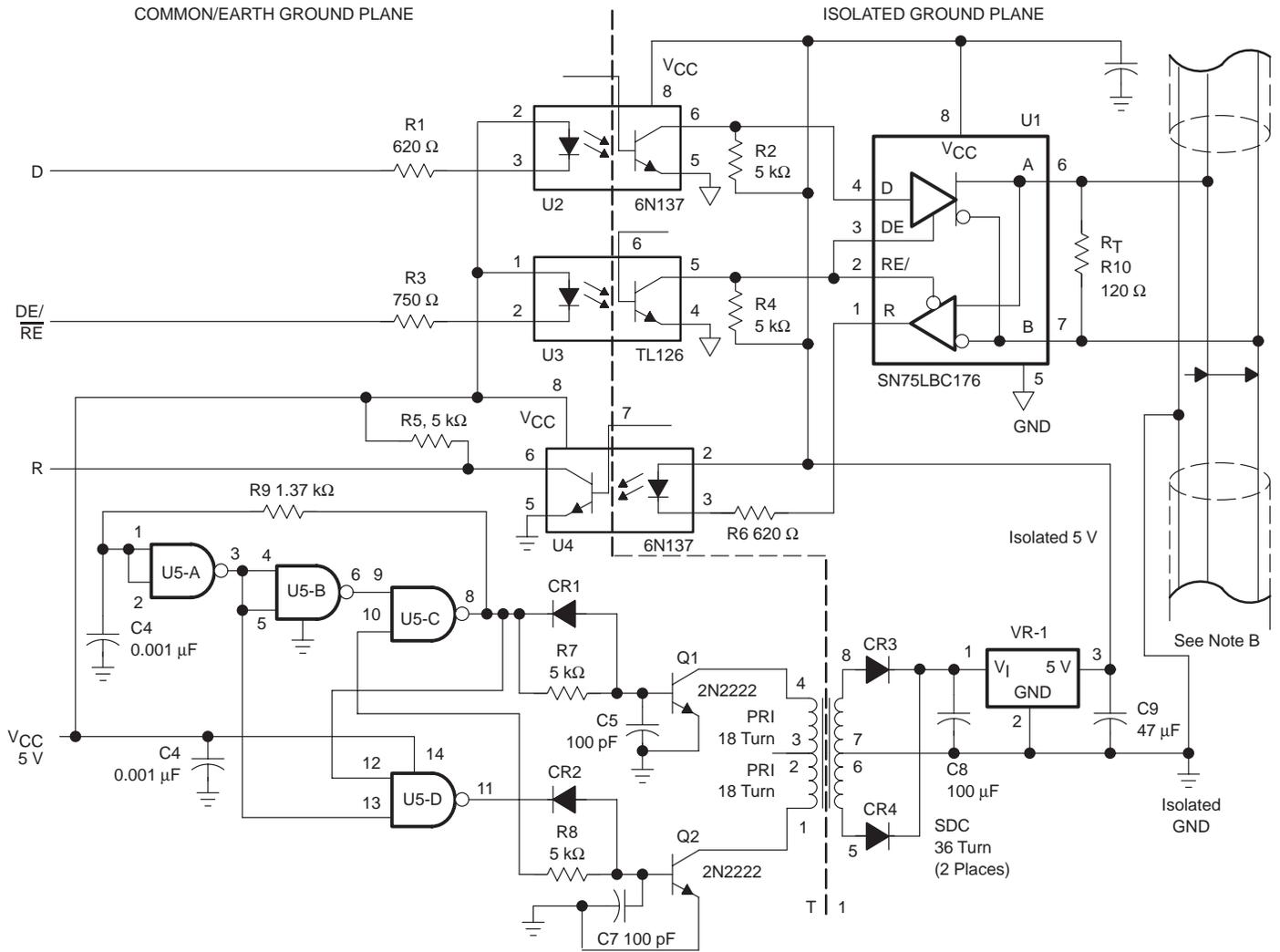
**Theory of Operation:** The example shown in Figure 10 provides Galvanic isolation through the use of optocouplers and an isolation transformer. Because the LBC176 needs power from a isolated power source, the 78L05 regulator must also be isolated. This is accomplished by the NAND-gate oscillator driving the isolation transformer. The output of the transformer is rectified, filtered, and used to bias the regulator. In high EMI environments, this approach is often used to prevent noise from being coupled into the main power source where it can be passed to other subsystems connected to the same source. Galvanic isolation is provided by three optocouplers/optoisolators. Transmit and receive channels are isolated using the 6N137 optocoupler, which was chosen for its high data-rate capability ( $t_p = 75$  ns maximum) and its high-voltage isolation. The 6N137 was designed for use in high-speed digital interfacing applications that require high-voltage isolation between the input and the output. Its use is highly recommended for use in high-ground-noise or induced-noise environments. And, if necessary, the 78L05 can provide power to other devices. The circuit shown was tested with regulator loads up to 100 mA.

The 6N137 consists of a GaAsP light-emitting diode and integrated light detector, composed of a photo-diode, a high-gain amplifier, and a Schottky-clamped open-collector output transistor. An input diode forward current of 5 mA switches the output transistor low, providing an on-state drive current of 13 mA (eight 1.6 mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-pin DIP plastic package, the 6N137 is characterized for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a common-mode transient immunity of 1000 V/ $\mu$ s.

The enable line is isolated using a TIL126 where high bandwidth is not required and, although the example shows the TIL126, several TL devices can be used. Other devices can be used in place of the LBC176. For example, other 485/422 devices can be used. This circuit also can be used with LVDS devices, but the system bandwidth would be limited to that of the optocouplers selected, approximately 20 Mbit/s.

Components are available that provide all of the functions shown in Figure 10. However, the example shown using discrete components provides much better power-supply isolation and is significantly less expensive than the two-packaged-device solution.



REFERENCE DESIGNATOR	DESCRIPTION
R1, R6	Resistor, 620 Ω, 1/4 W, 1%
R2, R4, R5	Resistor, 5 k Ω, 1/4 W, 1%
R3	Resistor, 750 Ω, 1/4 W, 1%
R7, R8	Resistor, 1 k Ω, 1/4 W, 1%
R9	Resistor, 130 k Ω, 1/4 W, 1%
R10	Resistor, 120 Ω, 1/4 W, 1%
C1, C2, C3, C10	Capacitor, 0.1 μF, 100 V, 10%
C4, C6	Capacitor, 0.001 μF, 100 V, 10%
C5, C7	Capacitor, 100 μF, 100 V, 10%
C8	Capacitor, 100 μF, 50 V, 10%

REFERENCE DESIGNATOR	DESCRIPTION
C9	Capacitor, 47 μF, 50 V, 20%
CR1, CR2	Diode, 1N4148
CR3, CR4	Diode, 1N5817
Q1, Q2	Transistor, 2N2222
T1	Transformer
U1	IC, SN75LBC176, Diff. Bus Transceiver
U2, U4	IC, 6N137 Optocoupler/Isolator
U3	IC, TIL126 Optocoupler/Isolator
U5	IC, SN74HC132N, Quadruple Positive NAND Gate
VR1	Regulator, Voltage, UA78M05CKC, 5 V, Positive

- NOTES: A. The line-matching resistor,  $R_T$ , is used only at the ends of the cable. Terminated fail-safe circuitry also can be included at one point on the bus.
- B. Shield should be terminated to each chassis ground and earth ground at one point only. The third-wire ground should be earth grounded at one point only.

**Figure 10. Isolated 485 Node With the SN75LBC176**

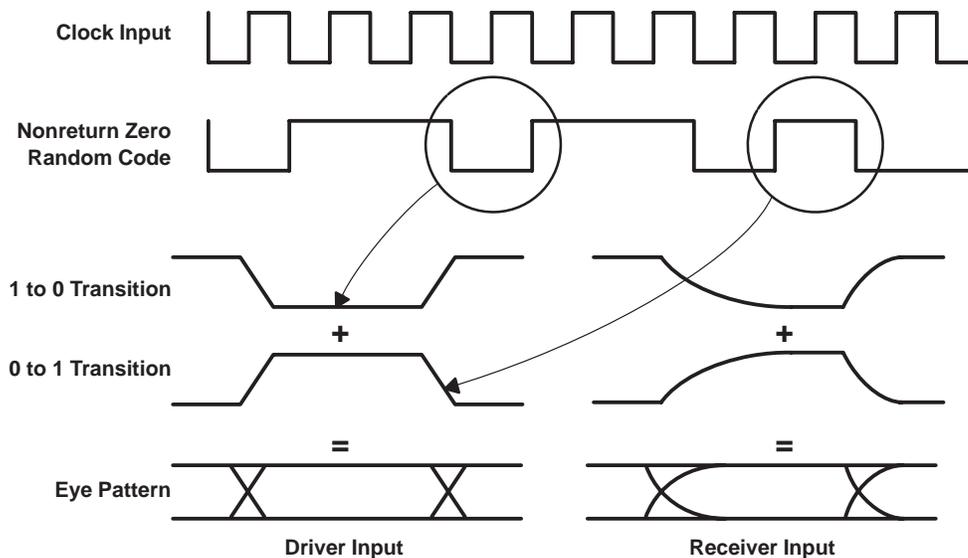
## Eye Patterns

To measure the effects of signal distortion, noise, and signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system, the eye pattern is used. ISI is the effect of neighboring pulses in a pulse train interfering with preceding or succeeding pulses, and forces a reduction in the signaling rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope, with the term *eye* coming from the appearance of the trace on the CRT.

### Setting Up the Eye Pattern

The eye pattern is obtained by applying a pseudo-random non-return-to-zero (NRZ) code down the transmission line under test. This represents nearly all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the scope triggered using the synchronization clock to the NRZ code generator on a separate trace (see Figure 11).

Formation of Eye Pattern



**Figure 11. Signal Distortion Using Eye Patterns**

Over any one unit interval, the pseudo-random code generator should produce a combination of signals. The resulting signals then can be viewed on the oscilloscope over a one-unit interval; each unit interval should resemble an eye similar to that shown in Figure 12. For differential transmission, both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

Figure 13 shows a circuit that generates the NRZ code. In this case, it was used to test the 485 SN75176-type transceiver.

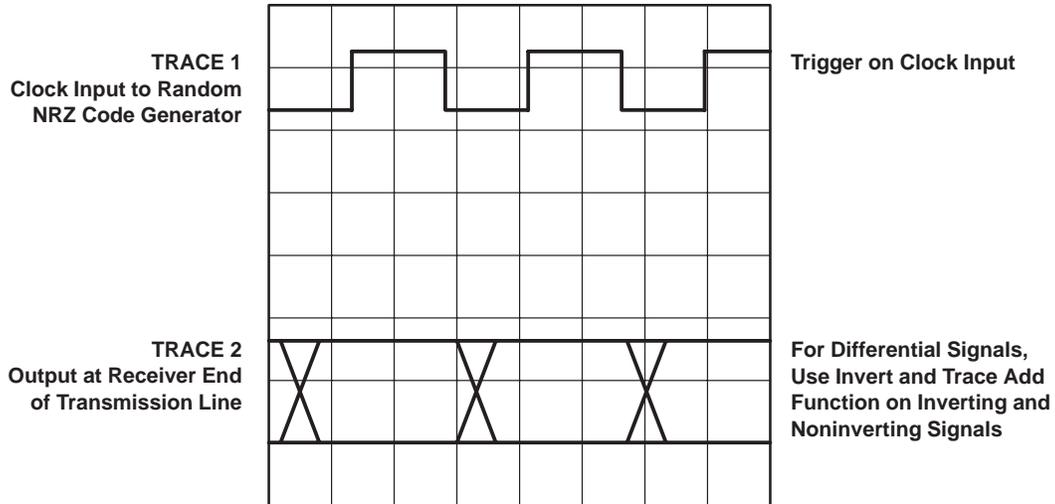


Figure 12. Eye Pattern Oscilloscope Trace

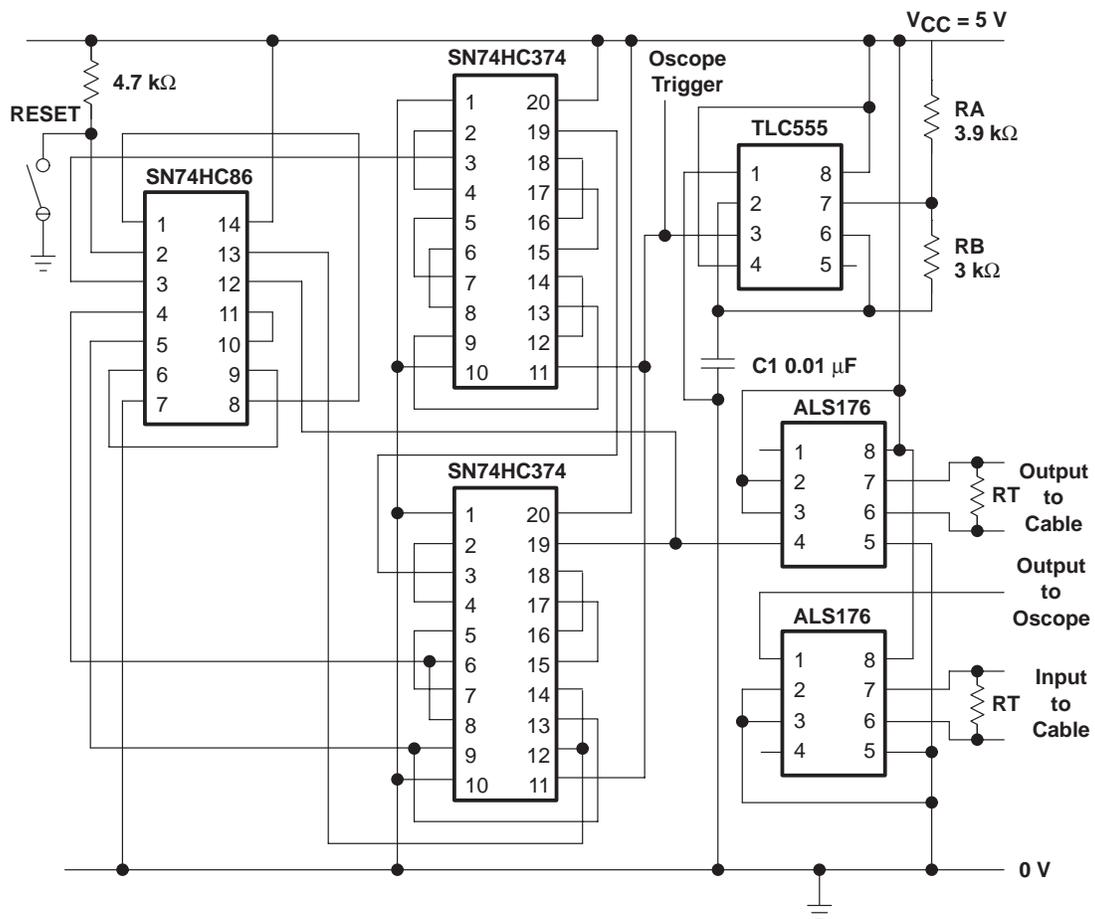


Figure 13. NRZ Random Code Generator

## Taking Measurements from Eye Patterns

Before considering actual measurements, the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The openness of the eye is an indication of the quality of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

For actual measurements, the decision points of the transceiver should be superimposed on the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum time jitter of the system. The maximum allowable jitter is dependent on the timing accuracy of the receiving circuitry. A conservative guide used by cable manufacturers to determine signaling rate versus line-length curves is no more than 5% jitter. Where percent jitter is defined as the ratio of threshold crossing skew to unit interval as shown in Figure 14. Jitter is caused by a number of factors, including signal frequency, noise, and crosstalk. Noise frequency can modulate the transmitted signal, for example 50-Hz hum or noise from other low-frequency sources. Also the effect of threshold misalignment can cause severe problems with the received signal, reducing the detected pulse width considerably.

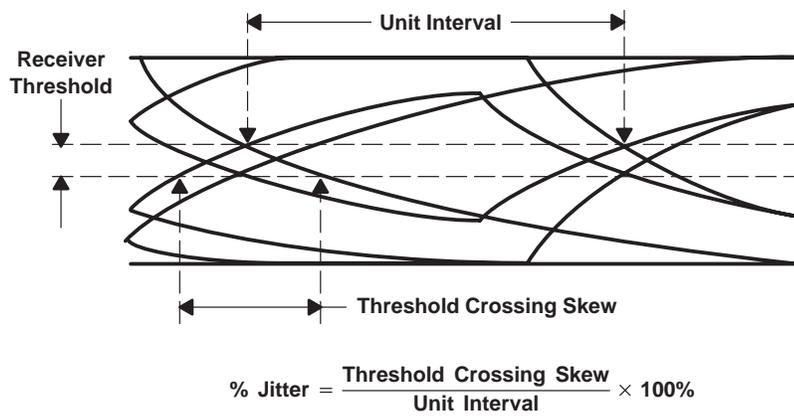


Figure 14. Measuring Signal Transmission Quality