

SANYO**LA6543M****4-Channel Bridge (BTL) Driver for CD-ROM****Overview**

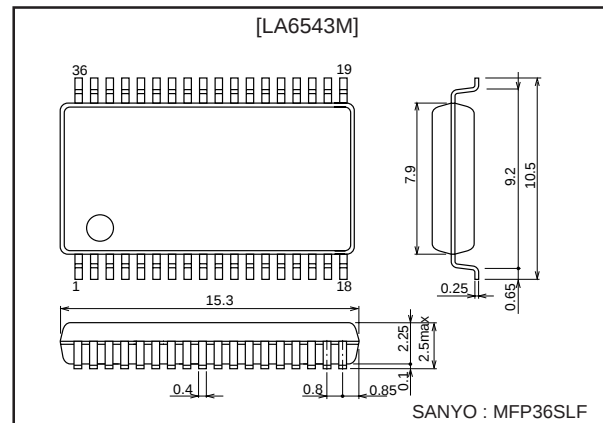
The LA6543M is a 4-channel bridge (BTL) driver developed for CD-ROM applications.

Functions

- 4-channel power amplifier with bridge circuit (BTL)
- I_O max: 1A
- Integrated muting circuit (MUTE: Output OFF at Low, output ON at High. MUTE1 is for channel 1, and MUTE2 for channels 2, 3 and 4.)
- Integrated thermal shutdown circuit
- Divided output stage power supply (VS1: CH1, CH2, CH3; VS2: CH4)

Package Dimensions

unit: mm

3129-MFP36SLF**Specifications****Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC\max}$		14	V
Maximum supply voltage 2	$V_{S\max}$	$V_{S1, 2}$	14	V
Input voltage	$V_{IN\max}$	Input pins V_{IN1} to 4	13	V
Mute pin voltage	$V_{MUTE\max}$		13	V
Allowable power dissipation	$P_d \max$	IC only	0.9	W
		Specified substrate Note 1	2.1	W
Operating temperature	T_{opr}		- 20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		- 55 to +150	$^\circ\text{C}$

Note 1: Specified substrate 76.1 x 114.3 x 1.6 (t)mm, glass exposy

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operation voltage 1	V_{CC}		4 to 13	V
Recommended operation voltage 2-1	V_{S1}	V_{S1} : CH1 to CH3	4 to 13	V
Recommended operation voltage 2-2	V_{S2}	V_{S2} : CH4 output reference power supply	4 to 13	V

* $V_{CC} > V_{S1, 2}$

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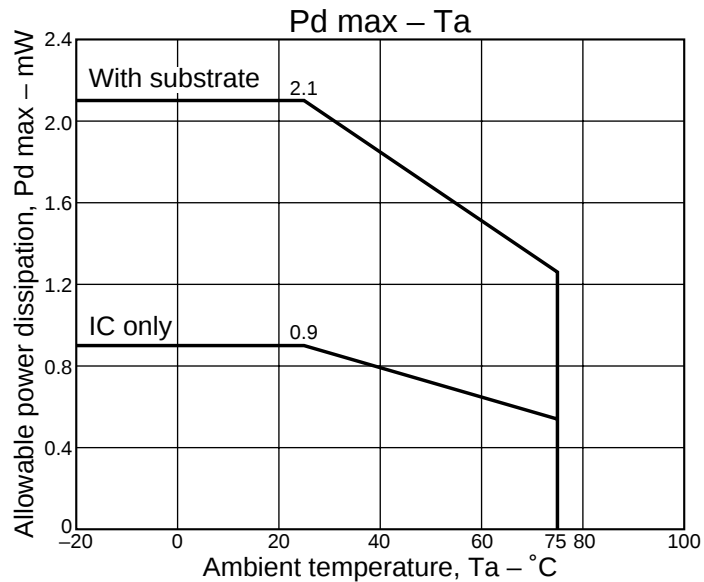
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Electrical Characteristics at $V_{CC} = 12V$, $V_S = 5V$, $T_a = 25^\circ C$

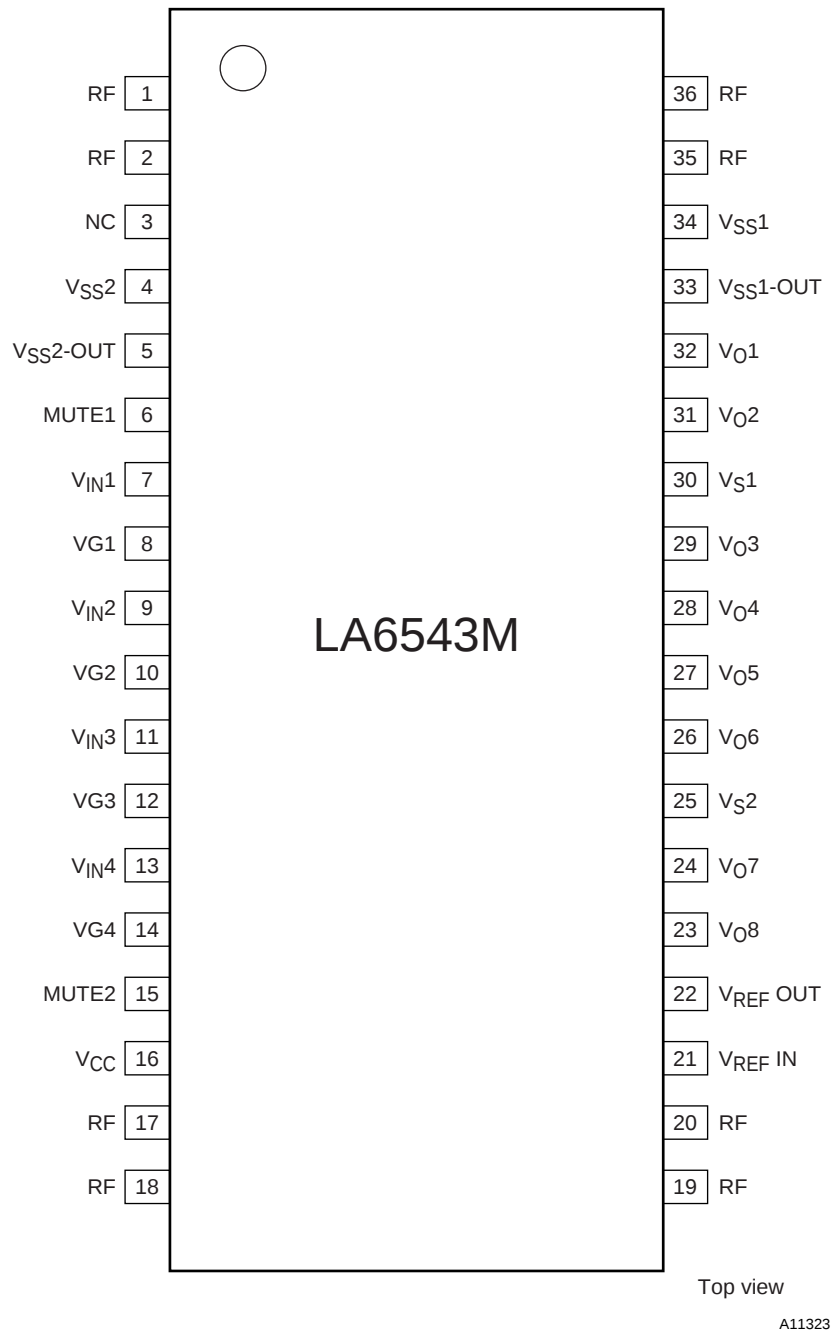
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no-load current drain	I_{CC1}	All outputs ON (MUTE1, MUTE2: High)	5	10	20	mA
	I_{CC2}	All outputs OFF (MUTE1, MUTE2: Low)		5	10	mA
V_S1 no-load current drain	I_{S1-1}	CH1 - CH2 ON (MUTE1, MUTE2: High)		20	30	mA
	I_{S1-2}	CH1 - CH2 OFF (MUTE1, MUTE2: Low)			4	mA
V_S2 no-load current drain	I_{S2-1}	CH3 - CH4 ON (MUTE1, MUTE2: High)		5	10	mA
	I_{S2-2}	CH3 - CH4 OFF (MUTE1, MUTE2: Low)			4	mA
Output offset voltage	V_{OF1} to 4	Potential difference between plus and minus outputs for CH1 to CH4	-50		+50	mV
Input voltage range	V_{IN}	Input voltage range for V_{IN1} to V_{IN4}	0.5		5	V
Output voltage (source) (sink)	V_{source}	Plus and minus outputs at high level	4.4	4.7		V
		$I_O = 700$ mA				
	V_{sink}	Plus and minus outputs at low level		0.3	0.6	V
		$I_O = 700$ mA				
Closed circuit voltage gain	VG1	Voltage gain between CH1 to CH3 BTL amplifiers		7		dB
	VG2	Voltage gain between CH4 BTL amplifiers		14		dB
Slew rate	SR	(Note 1)		0.5		V/ μ s
Mute ON voltage	V_{MUTE}	MUTE1, MUTE2 voltage when output is ON (Note 2)		1.5	2	V
Mute ON current	I_{MUTE}	MUTE1, MUTE2 current when output is ON (Note 2)		6	10	μ A

Note 1: Guaranteed design value

Note 2: MUTE turns amplifier output ON at High and OFF at Low. (Output impedance becomes high.) This applies to MUTE1 and MUTE2.



Pin Assignment

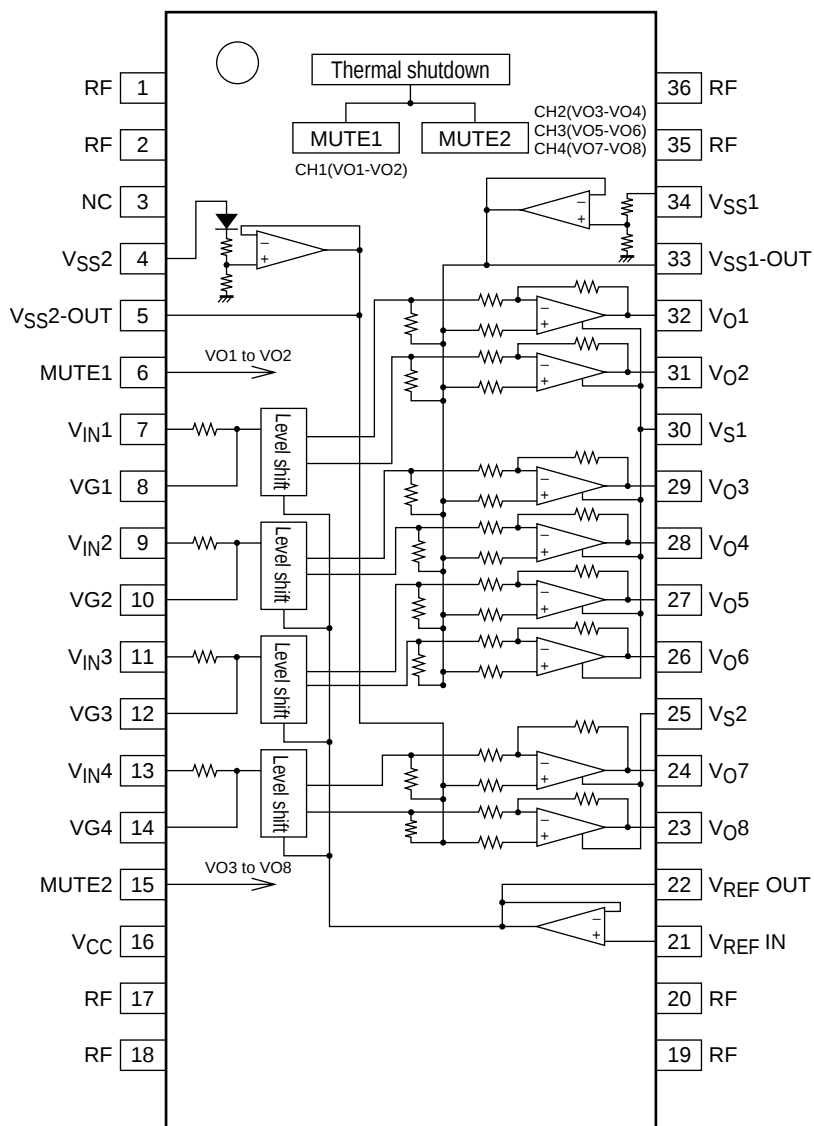


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Pin Function

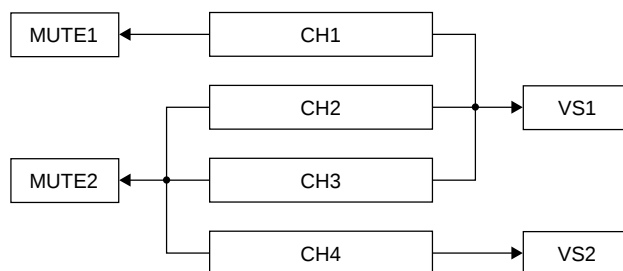
Pin number	Pin name	Equivalent circuit	Pin function
1, 2 17, 18 19, 20 35, 36	RF		Substrate (minimum potential)
7 9 11 13	V _{IN} 1 V _{IN} 2 V _{IN} 3 V _{IN} 4		Input pin for CH1 Input pin for CH2 Input pin for CH3 Input pin for CH4
8 10 12 14	VG1 VG2 VG3 VG4		Input pin for CH1 (gain adjustment) Input pin for CH2 (gain adjustment) Input pin for CH3 (gain adjustment) Input pin for CH4 (gain adjustment)
16	V _{CC}		Power supply
22	V _{REF} OUT		Level shift circuit reference voltage (V _{REF} 1 buffer amplifier output)
3	NC		May not be used.
4	V _{SS} 2		Connect to V _S 2
5	V _{SS} 2-OUT		Output stage reference voltage output (V _S 2-V _{BE})/2: typ)
6 15	MUTE1 MUTE2		CH1 output ON/OFF CH2 to CH4 output ON/OFF
21	V _{REF} IN		Level shift circuit reference voltage input (V _{REF} 1 buffer amplifier input)
23 24 26 27 28 29 31 32	V _O 8 V _O 7 V _O 6 V _O 5 V _O 4 V _O 3 V _O 2 V _O 1		CH4 inverted output (AMP8 output) CH4 non-inverted output (AMP7 output) CH3 inverted output (AMP6 output) CH3 non-inverted output (AMP5 output) CH2 inverted output (AMP4 output) CH2 non-inverted output (AMP3 output) CH1 inverted output (AMP2 output) CH1 non-inverted output (AMP1 output)
25	VS2		CH3 (AMP5, AMP6), CH4 (AMP7, AMP8) output stage power supply
30	VS1		CH1 (AMP1, AMP2), CH2 (AMP3, AMP4) output stage power supply
33	V _{SS} 1-OUT		Output stage reference voltage (V _{SS} 1/2:typ) (V _{REF} 2 buffer amplifier input)
34	V _{SS} 1		Connect to VS1 (resistance split to generate V _{SS} 1-OUT)

Block Diagram



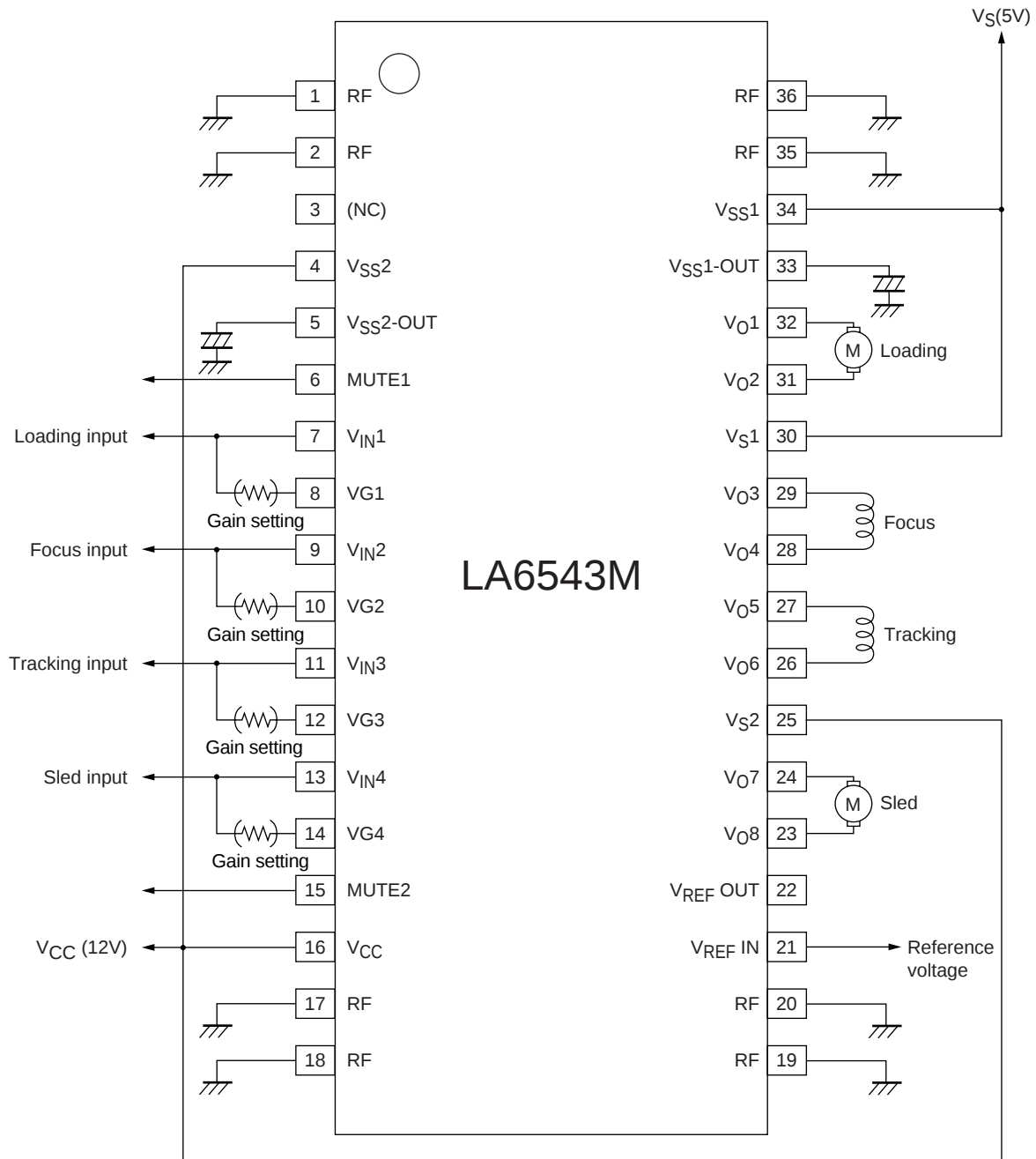
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System Diagram (relationship between power supply and MUTE)



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Sample Application Circuit



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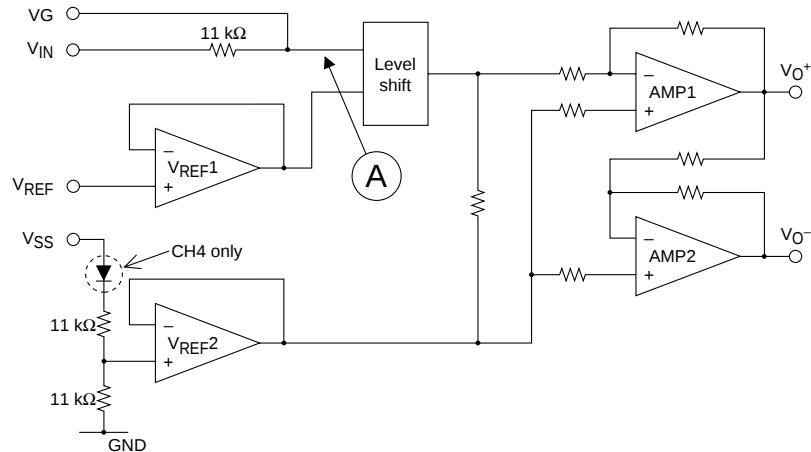
Gain Setting (input pins and adjustment pins)

A simplified diagram of V_{IN} and V_G is shown below.

- 1) Consider an 11 k Ω (typ.) inserted between V_{IN} and V_G .
- 2) When only V_{IN} and not V_G is used, the BTL gain (between V_{O+} and V_{O-}) is set to 6 dB (0 dB for AMP only). This also applies for the case when V_{IN} is not used and an 11 k Ω external resistor is connected to V_G for input.
- 3) Gain is set by the input impedance as seen from point A.

When V_G only is used and the external resistor is R , the BTL gain (between V_{O+} and V_{O-}) is $20 \log (11 \text{ k}\Omega/R) + 6 \text{ dB}$.

When an 11 k Ω resistor is inserted between V_{IN} and V_G , and input is via V_{IN} , the combined resistance R_z as seen from point A is $R_z = 5.5 \text{ k}\Omega$. Gain is $20 \log (11 \text{ k}\Omega/5.5 \text{ k}\Omega) + 6 \text{ dB} = 12 \text{ dB}$.



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Offset Voltage

This IC incorporates a level shifter circuit. The input references the voltage V_{REF} to be applied and references the voltage $(V_{SS} - V_{BE} (0.7))/2V$ to be output.

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