

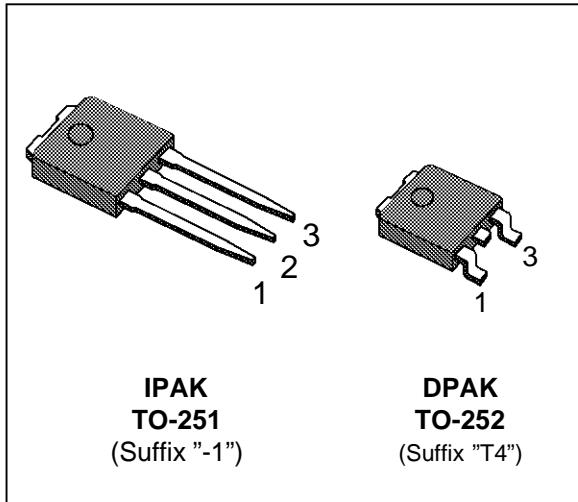
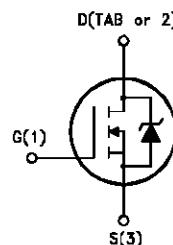
N - CHANNEL ENHANCEMENT MODE  
 LOW THRESHOLD POWER MOS TRANSISTOR

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD15N06L	60 V	< 0.1 Ω	15 A

- TYPICAL R<sub>DS(on)</sub> = 0.075 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

**APPLICATIONS**

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)


**INTERNAL SCHEMATIC DIAGRAM**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	60	V
V <sub>GS</sub>	Gate-source Voltage	± 15	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	15	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	10	A
I <sub>DM(•)</sub>	Drain Current (pulsed)	60	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	50	W
	Derating Factor	0.33	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

# STD15N06L

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## THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	3	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}\text{C}/\text{W}$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}\text{C}/\text{W}$
$T_L$	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}\text{C}$

## AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta < 1\%$ )	15	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 25\text{ V}$ )	50	mJ
$E_{AR}$	Repetitive Avalanche Energy (pulse width limited by $T_j$ max, $\delta < 1\%$ )	12	mJ
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive ( $T_c = 100^{\circ}\text{C}$ , pulse width limited by $T_j$ max, $\delta < 1\%$ )	10	A

## ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$			250 1000	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 15\text{ V}$			$\pm 100$	nA

### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 5\text{ V}$ $I_D = 7.5\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 7.5\text{ A}$ $T_c = 100^{\circ}\text{C}$		0.075	0.1 0.2	$\Omega$ $\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)\max}$ $V_{GS} = 10\text{ V}$	15			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)\max}$ $I_D = 7.5\text{ A}$	3	5		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		700 230 80	950 310 110	pF pF pF

**ELECTRICAL CHARACTERISTICS (continued)**

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Time Rise Time	$V_{DD} = 30 \text{ V}$ $I_D = 7.5 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 5 \text{ V}$ (see test circuit figure)		15 160	60 200	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 40 \text{ V}$ $I_D = 15 \text{ A}$ $R_G = 47 \Omega$ $V_{GS} = 5 \text{ V}$ (see test circuit figure)		70		A/ $\mu\text{s}$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 40 \text{ V}$ $I_D = 15 \text{ A}$ $V_{GS} = 5 \text{ V}$		18 8 9	30	nC nC nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 48 \text{ V}$ $I_D = 15 \text{ A}$ $R_{GS} = 47 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit figure)		52 100 170	80 140 240	ns ns ns

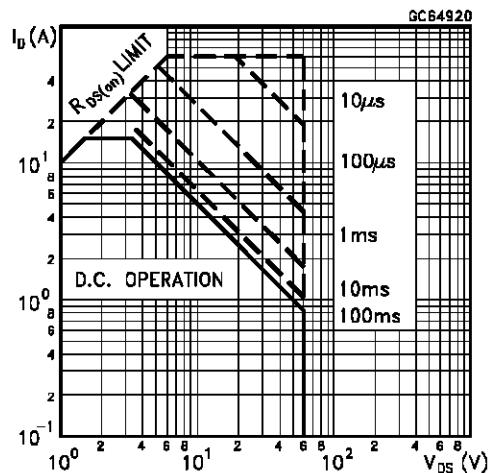
## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM(\bullet)}$	Source-drain Current Source-drain Current (pulsed)				15 60	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 15 \text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 15 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 25 \text{ V}$ $T_j = 150^\circ\text{C}$		60 0.14 5		ns $\mu\text{C}$ A

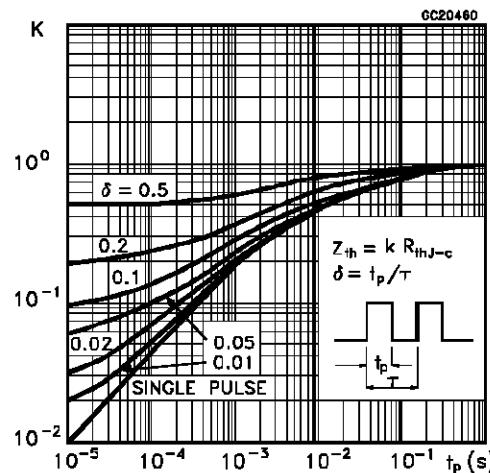
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(\*) Pulse width limited by safe operating area

## Safe Operating Area



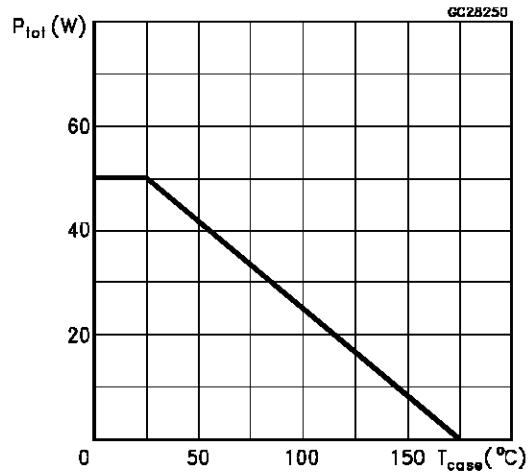
## Thermal Impedance



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Derating Curve



Output Characteristics

Transfer Characteristics

Transconductance

Static Drain-source On Resistance

Gate Charge vs Gate-source Voltage

Capacitance Variations

Normalized Gate Threshold Voltage vs  
Temperature

Normalized On Resistance vs Temperature

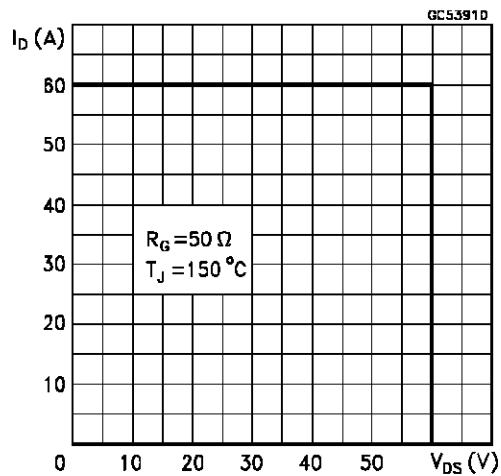
Turn-on Current Slope

Turn-off Drain-source Voltage Slope

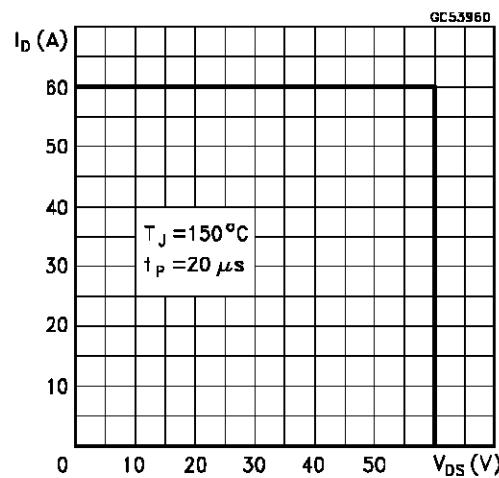
Cross-over Time

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### Switching Safe Operating Area

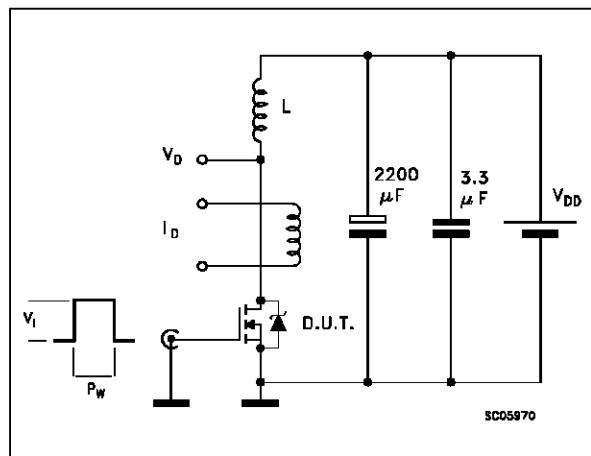


### Accidental Overload Area

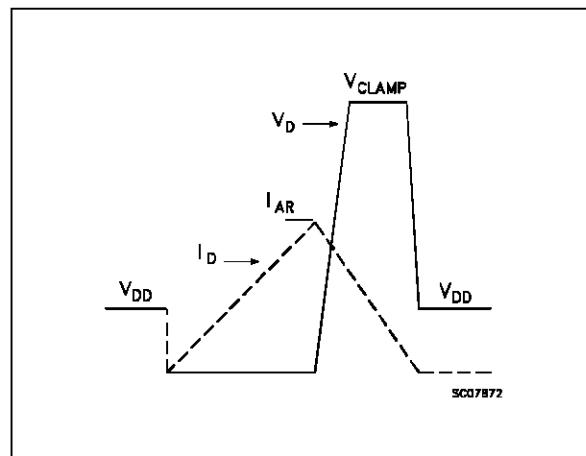


### Source-drain Diode Forward Characteristics

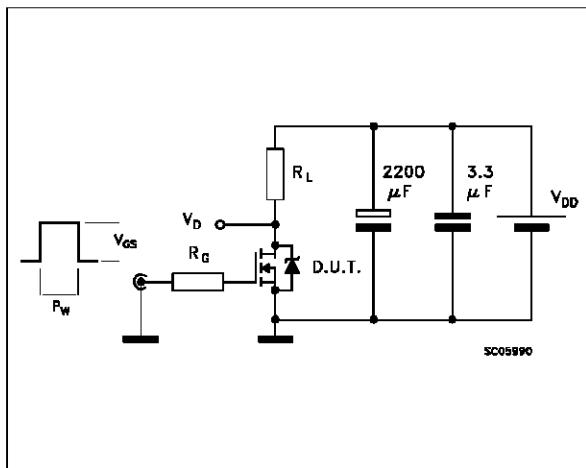
**Fig. 1:** Unclamped Inductive Load Test Circuits



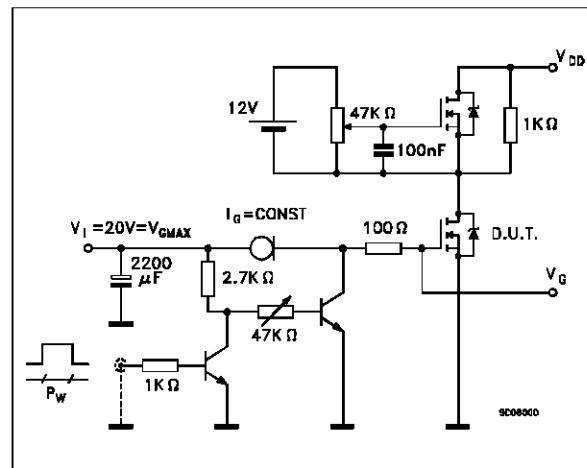
**Fig. 2:** Unclamped Inductive Waveforms



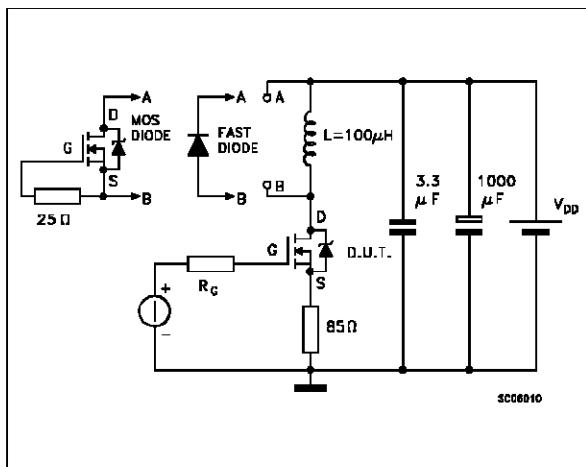
**Fig. 3:** Switching Times Test Circuits For Resistive Load



**Fig. 4:** Gate Charge Test Circuit

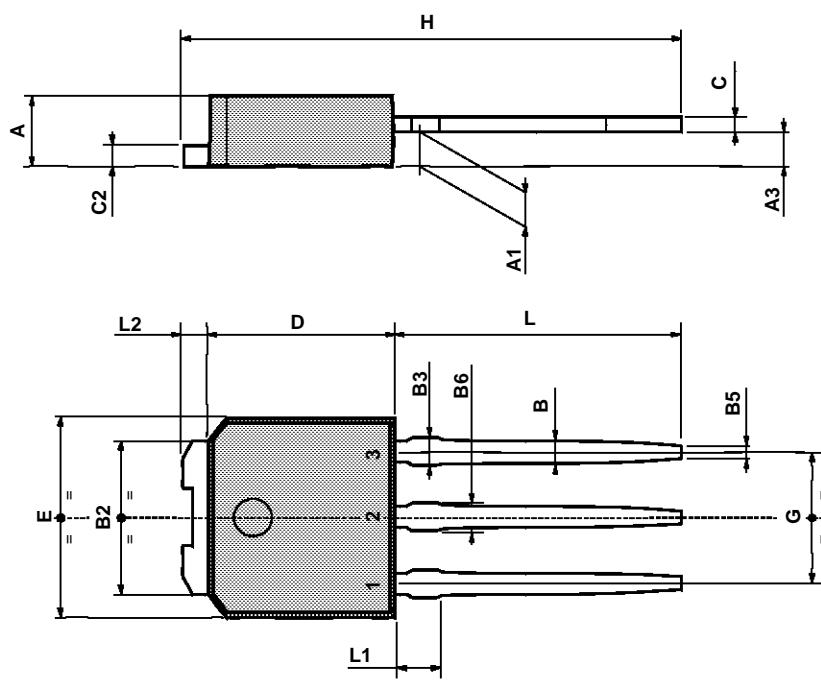


**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-251 (IPAK) MECHANICAL DATA

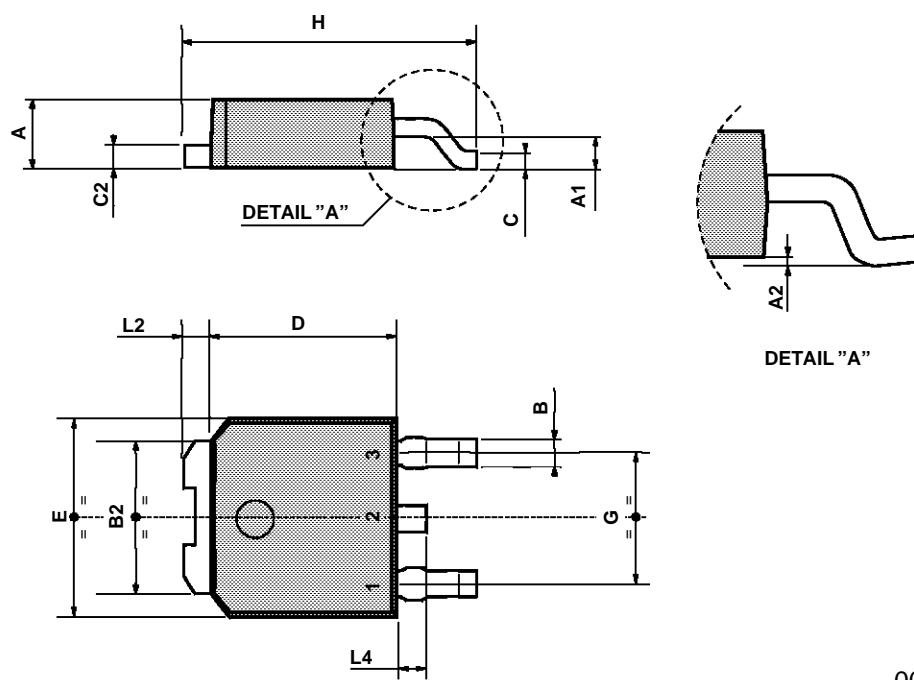
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



0068772-B

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