MK41T56
MKI41T56

512 bit (64b x8) Serial Access TIMEKEEPER® SRAM

NOT FOR NEW DESIGN

- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH and YEARS
- SOFTWARE CLOCK CALIBRATION
- AUTOMATIC POWER-FAIL DETECT and SWITCH CIRCUITRY
- I^2C BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA
- OPERATING TEMPERATURE:
  - MK41T56: 0 to 70°C
  - MKI41T56: –40 to 85°C
- AUTOMATIC LEAP YEAR COMPENSATION

PSDIP8 (N)
0.4mm Frame

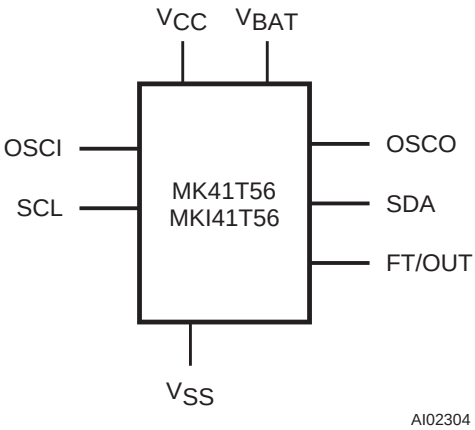
SO8 (M)
150mil Width

DESCRIPTION

The MK41T56 TIMEKEEPER® is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell.

Data retention time is in excess of 10 years with a 50mAh 3V lithium cell. The MK41T56 is supplied in 8 pin Plastic Dual-in-Line and 8 lead Plastic SOIC packages.

Figure 1. Logic Diagram



This is information on a product still in production but not recommended for new designs.

Figure 2. DIP Connections

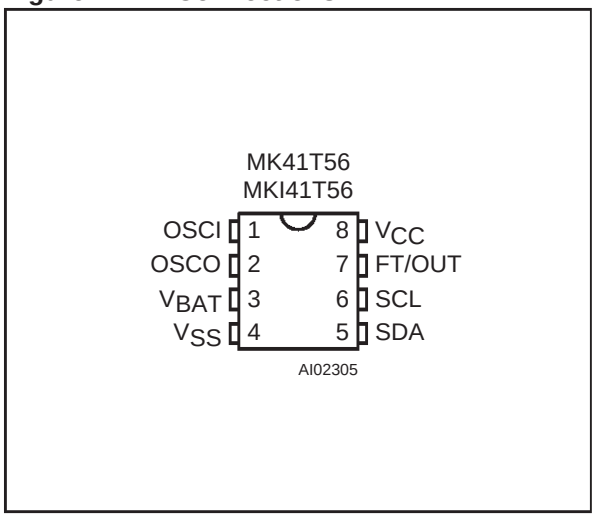


Figure 3. SOIC Connections

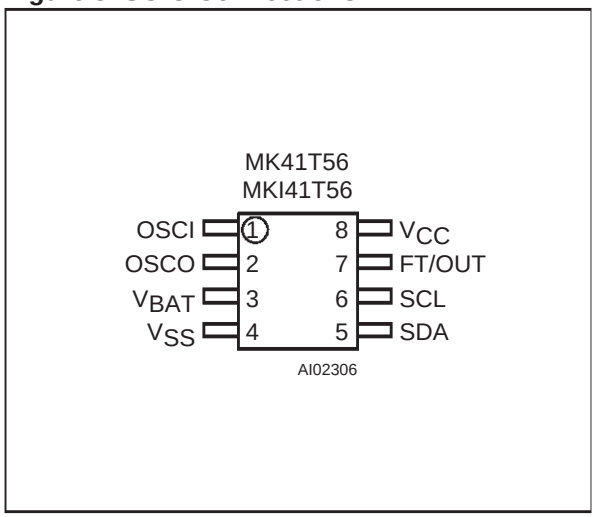


Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test / Output Driver (Open Drain)
SDA	Serial Data Address Input / Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

OPERATION

The MK41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (11010000). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds Register
2. Minutes Register
3. Hours Register
4. Day Register
5. Date Register
6. Month Register
7. Years Register
8. Control Register

9 to 64. RAM

The clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	MK41T56	0 to 70	°C
		MKI41T56	–40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)		–55 to 125	°C
V_{IO}	Input or Output Voltages		–0.3 to 7	V
V_{CC}	Supply Voltage		–0.3 to 7	V
I_O	Output Current		20	mA
P_D	Power Dissipation		0.25	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Register Map

Address	Data								Function/ Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	X	10 Minutes			Minutes				Minutes	00-59
2	X	X	10 Hours		Hours				Hour	00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 Date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 Years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit
ST = STOP Bit
OUT = Output level
X = Don't care

Figure 4. Block Diagram

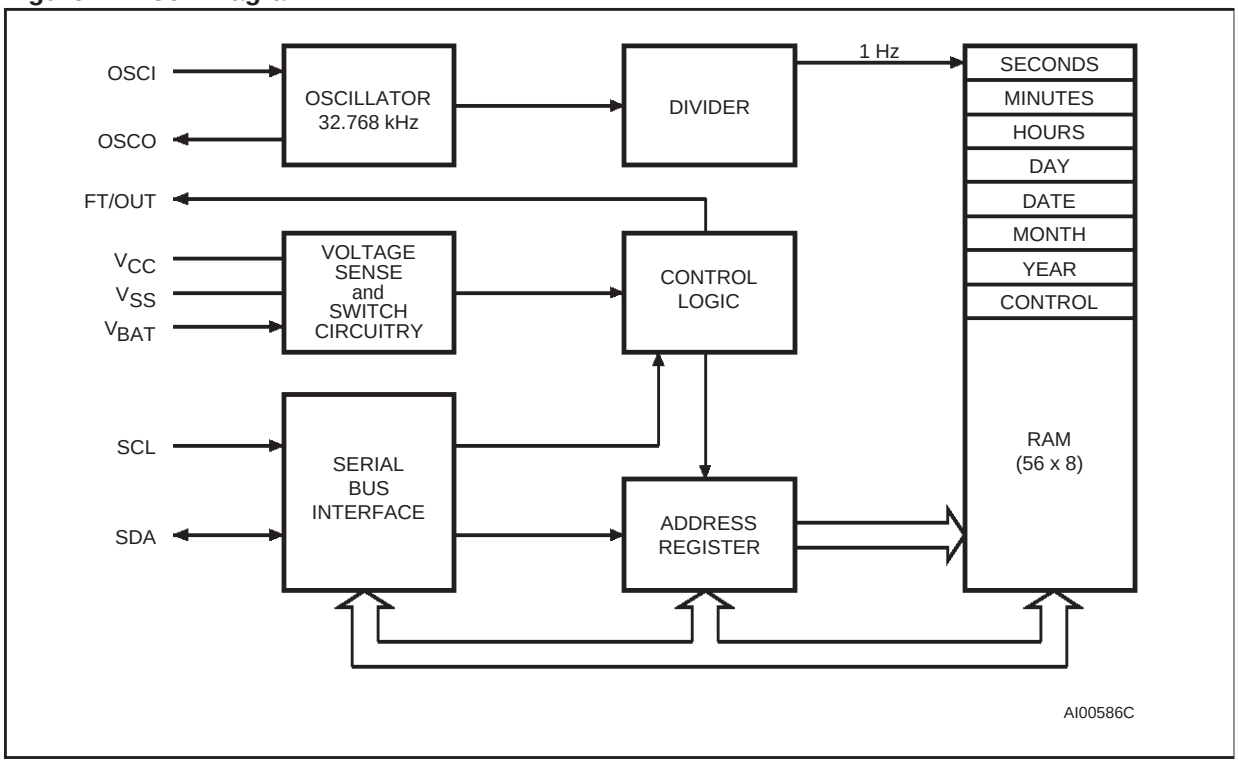


Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

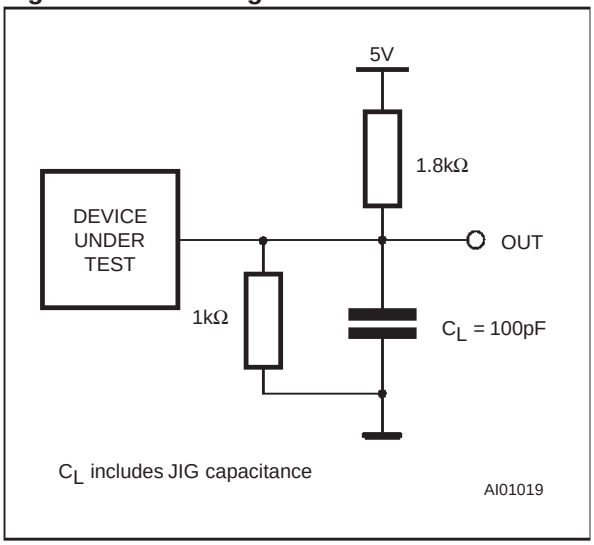


Table 5. Capacitance (1, 2)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SCL)		7	pF
C_{OUT} (2)	Output Capacitance (SDA, FT/OUT)		10	pF

Note: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±10	µA
I_{CC1}	Supply Current	SCL/SDA = V_{CC} – 0.3V			1	mA
I_{CC2}	Supply Current (Stand-by)				1	mA
V_{IL}	Input Low Voltage		–0.3		1.5	V
V_{IH}	Input High Voltage		3		V_{CC} + 0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{CC} = 4.5V			0.4	V
V_{BAT} (1)	Battery Supply Voltage		2.6	3	3.5	V
I_{BAT}	Battery Supply Current	T_A = 25°C, V_{CC} = 0V, Oscillator ON, V_{BAT} = 3V		450	500	nA

Note: 1. The RAYOVAC BR1225 or equivalent is recommended as the battery supply.

Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	1.2 V_{BAT}	1.25 V_{BAT}	1.285 V_{BAT}	V
V_{SO}	Battery Back-up Switchover Voltage		V_{BAT}		V

Note: 1. All voltages referenced to V_{SS}.

Table 8. Crystal Electrical Characteristics
(Externally Supplied)

Symbol	Parameter	Min	Typ	Max	Unit
f_O	Resonant Frequency		32.768		kHz
R_S	Series Resistance			35	kΩ
C_L	Load Capacitance		12.5		pF

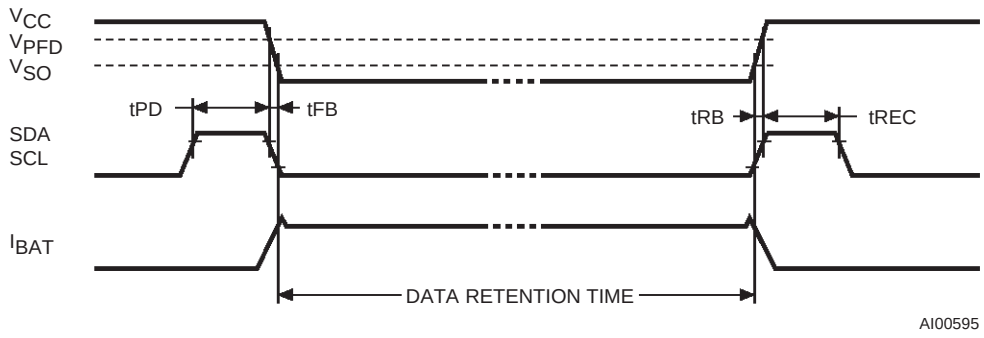
Note: Load capacitors are integrated within the MK41T56. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

STMicroelectronics recommends the ECS-.327-12.5-8SP-2 quartz crystal is recommended for industrial temperature operations. ESC Inc. can be contacted at 800-237-1041 or 913-782-7787 for further information on this crystal type.

Table 9. Power Down/Up Mode AC Characteristics
(T_A = 0 to 70 °C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before Power Down	0		ns
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	300		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	100		µs
t_{REC}	SCL and SDA at V_{IH} after Power Up	200		µs

Figure 6. Power Down/Up Mode AC Waveforms



2-WIRE BUS CHARACTERISTICS

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.
– During data transfer, the data line must remain stable whenever the clock line is High.
– Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number

Table 10. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL Clock Frequency	0	100	kHz
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4		µs
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{HD:STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	4		µs
$t_{SU:STA}$	START Condition Setup Time (only relevant for a repeated start condition)	4.7		µs
$t_{SU:DAT}$ (1)	Data Setup Time	250		ns
$t_{HD:DAT}$	Data Hold Time	0		µs
$t_{SU:STO}$	STOP Condition Setup Time	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
t_I	Noise suppression time constant at SCL and SDA input	0.25	1	µs

Note: 1. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called ”transmitter”, the receiving device that gets the message is called ”receiver”. The device that controls the message is called ”master”. The devices that are controlled by the master are called ”slaves”.

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 7. Serial Bus Data Transfer Sequence

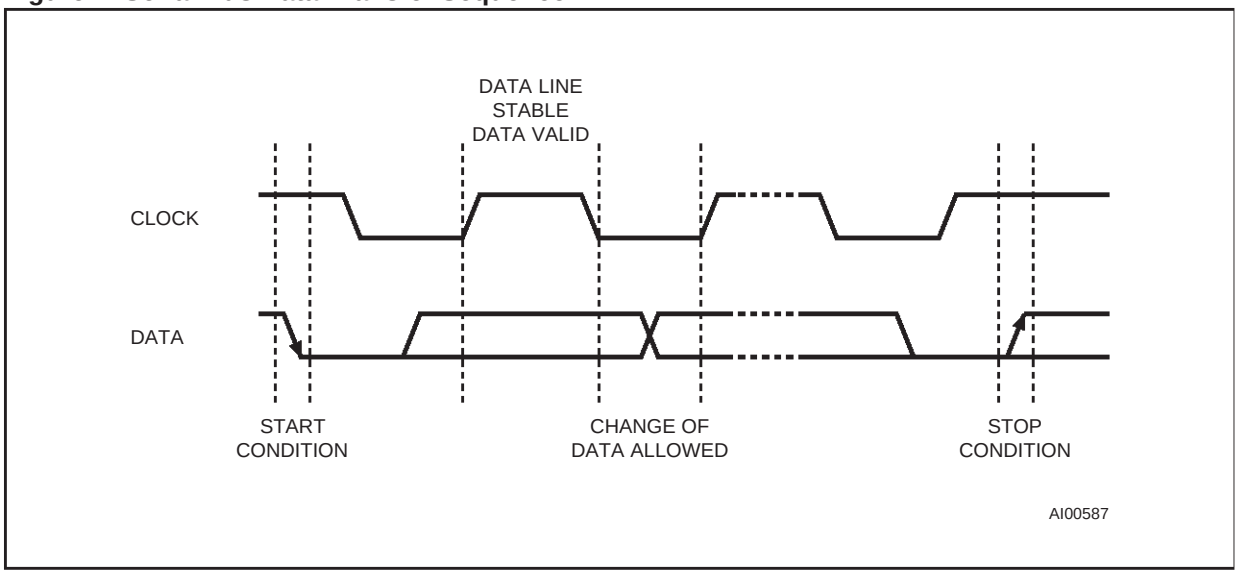


Figure 8. Acknowledgment Sequence

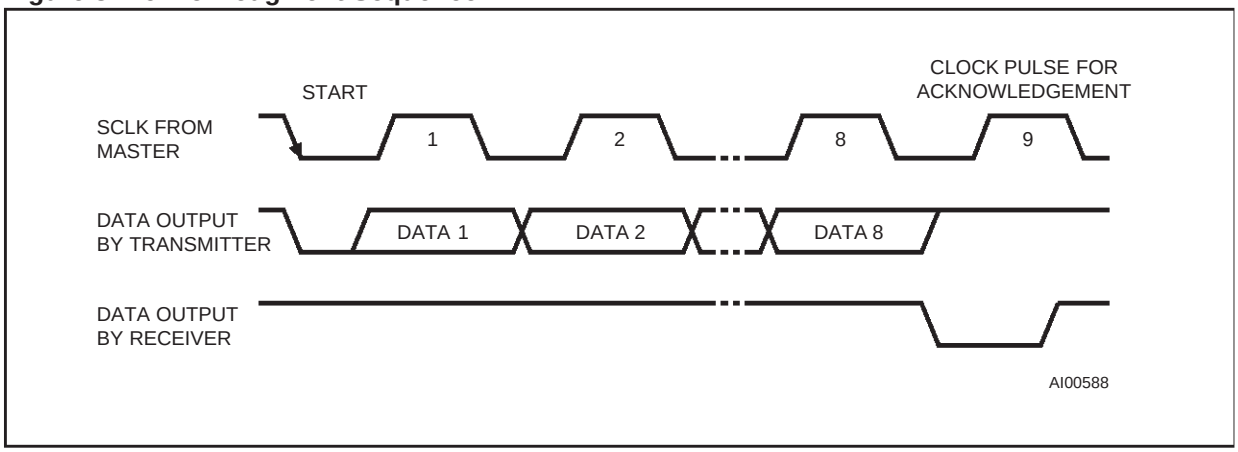
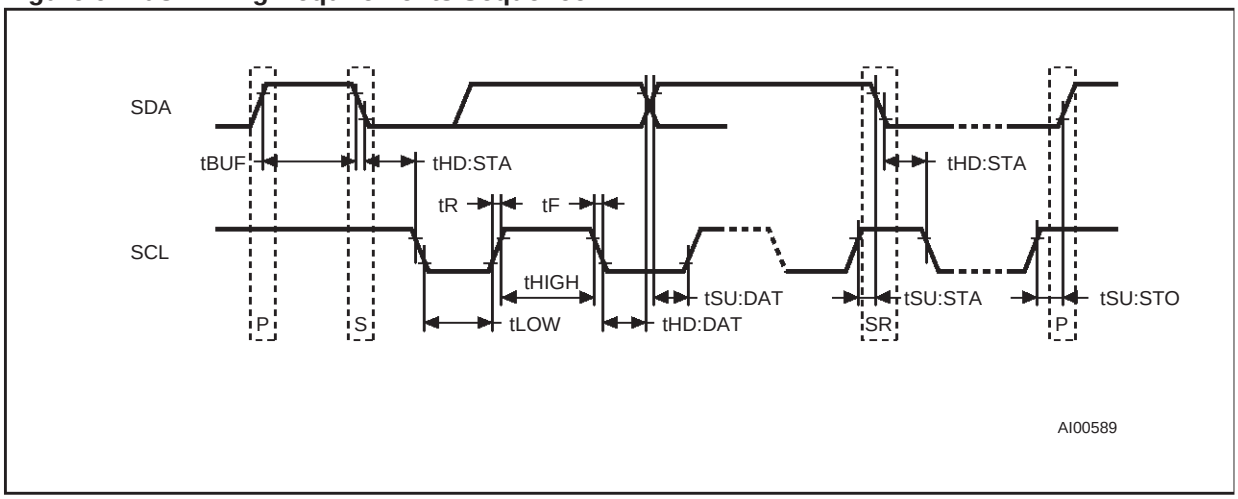


Figure 9. Bus Timing Requirements Sequence



Note: P = STOP and S = START

WRITE MODE

In this mode the master transmitter transmits to the MK41T56 slave receiver. Bus protocol is shown in Figure 10. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The MK41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see Figure 9).

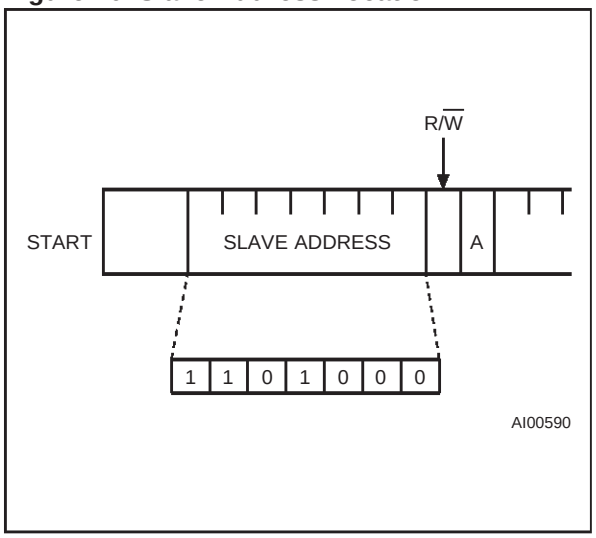
READ MODE

In this mode, the master reads the MK41T56 slave after setting the slave address (see Figure 11). Following the write mode control bit (R/$\overline{W}$ = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/$\overline{W}$ = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The MK41T56 slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the MK41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see Figure 12.

Figure 10. Slave Address Location



CLOCK CALIBRATION

The MK41T56 is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. A typical MK41T56 is accurate within ±1minute per month at 25°C without calibration. The devices are tested not to exceed 35ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. The oscillation rate of any crystal changes with temperature (see Figure 14).

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 13. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Figure 11. Write Mode Sequence

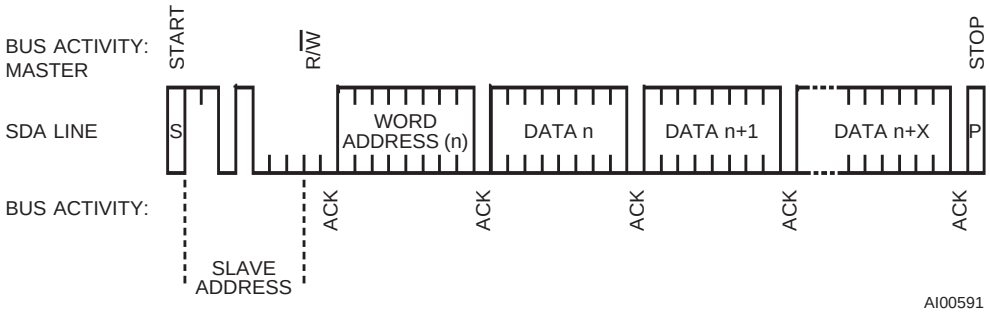


Figure 12. Read Mode Sequence

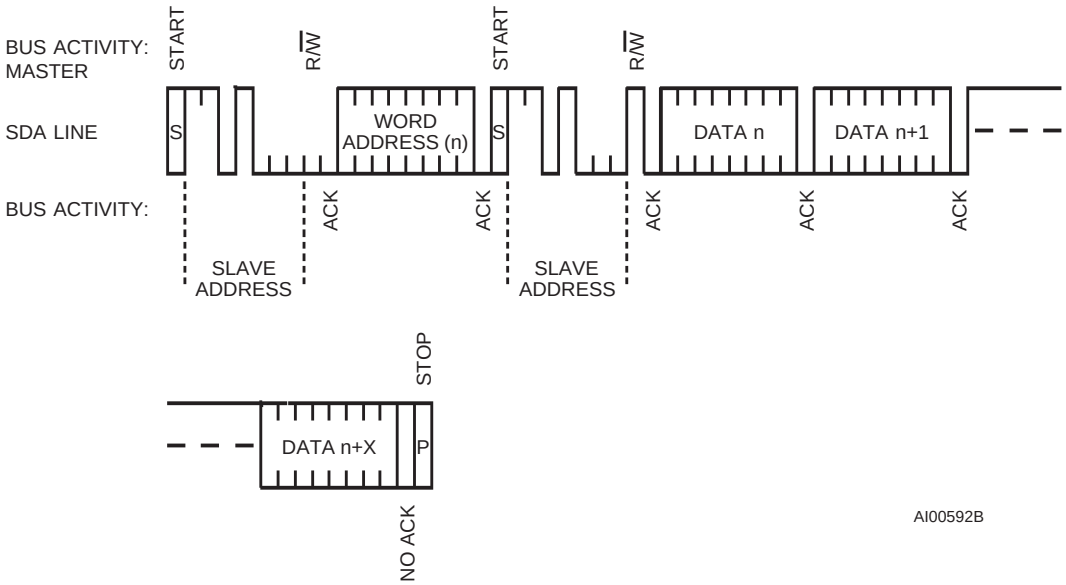


Figure 13. Alternate Read Mode Sequence

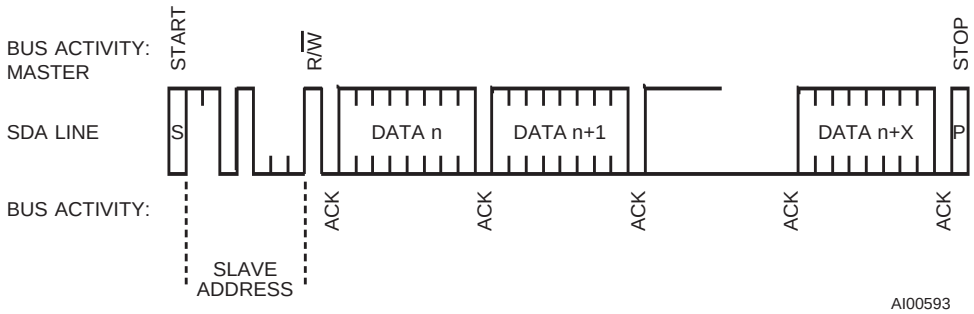
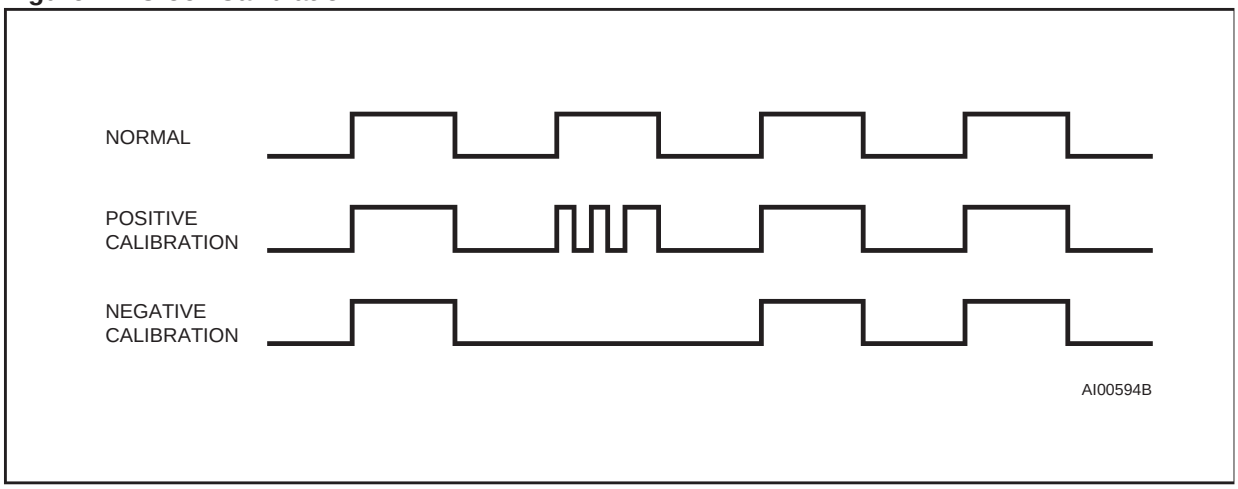


Figure 14. Clock Calibration



Two methods are available for ascertaining how much calibration a given MK41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Control Register, is set to a '1', and the oscillator is running at 32,768Hz, the FT/OUT pin of the device will toggle at 512Hz. Any deviation from 512Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

For example, a reading of 512.01024Hz would indicate a +20ppm oscillator frequency error, requiring a –10(XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

OUTPUT DRIVER PIN

When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D6 of location 7 is a zero and D7 of location 7 is a zero and then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is open drain which requires an external pull-up resistor.

Figure 15. Crystal Accuracy Across Temperature

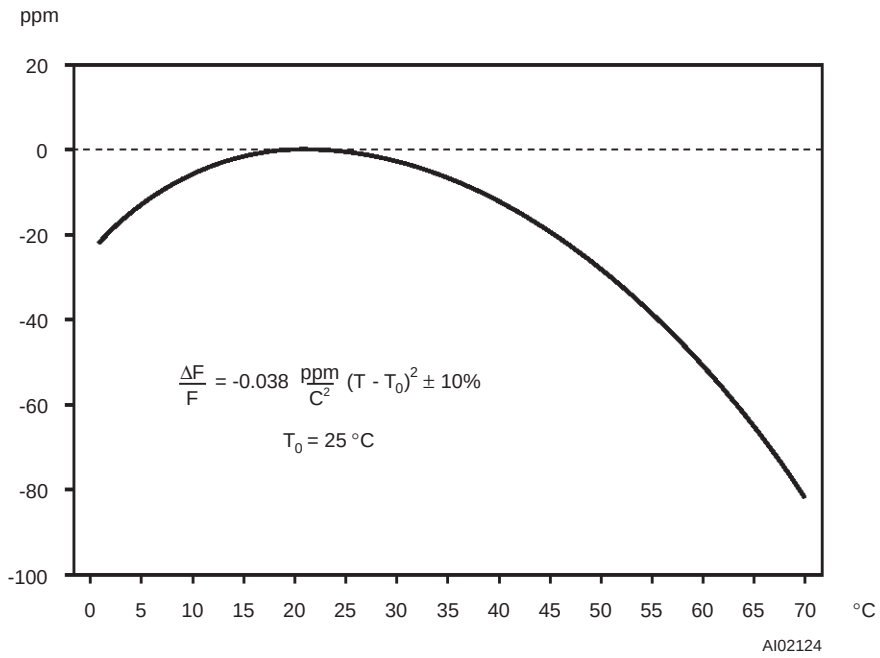


Table 11. Ordering Information Scheme

Example: MKI41T56 N 00 TR

Operating Temperature
blank = 0 to 70°C
I = –40 to 85°C

Package
N = PSDIP8 0.40mm Frame
S = SO8 0.15mm Frame

Speed
00 = No Speed Options

Shipping Method for SOIC
blank = Tubes
TR = Tape & Reel

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

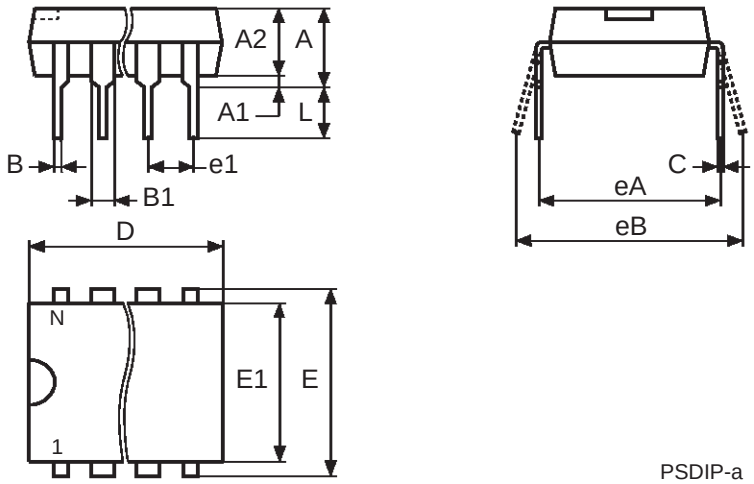
Table 12. Revision History

Date	Revision Details
March 1999	First Issue
11/30/00	From Data Sheet to Not for New Design

Table 13. PSDIP8 - 8 pin Plastic Small Skinny DIP, 0.4mm lead frame, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	4.80		–	0.1890
A1		0.70	–		0.0276	–
A2		3.10	3.60		0.1220	0.1417
B		0.38	0.58		0.0150	0.0228
B1		1.15	1.65		0.0453	0.0650
C		0.38	0.52		0.0150	0.0205
D		9.20	9.90		0.3622	0.3898
E	7.62	–	–	0.3000	–	–
E1		6.30	7.10		0.2480	0.2795
e1	2.54	–	–	0.1000	–	–
eA		8.40	–		0.3307	–
eB		–	9.20		–	0.3622
L		3.00	3.80		0.1181	0.1496
N	8			8		

Figure 16. PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame, Package Outline

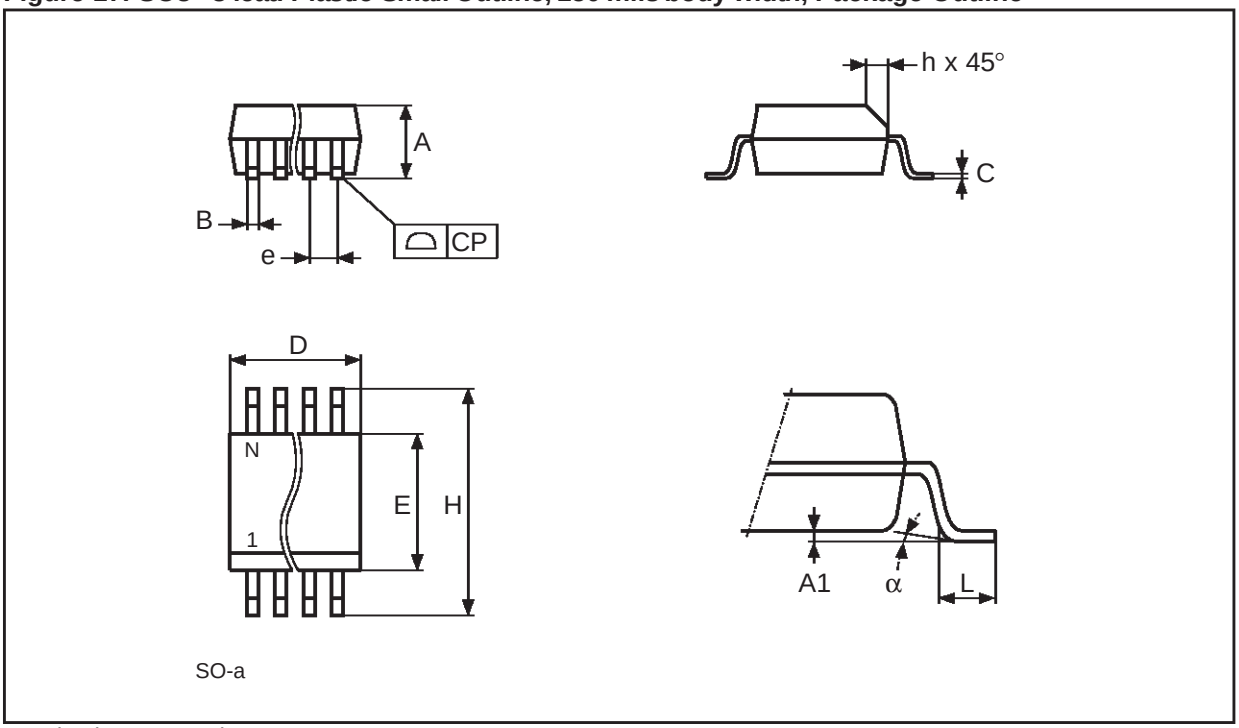


Drawing is not to scale.

Table 14. SO8 - 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.0531	0.0689
A1		0.10	0.25		0.0039	0.0098
B		0.33	0.51		0.0130	0.0201
C		0.19	0.25		0.0075	0.0098
D		4.80	5.00		0.1890	0.1969
E		3.80	4.00		0.1496	0.1575
e	1.27	–	–	0.0500	–	–
H		5.80	6.20		0.2283	0.2441
h		0.25	0.50		0.0098	0.0197
L		0.40	0.90		0.0157	0.0354
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.0039

Figure 17. SO8 - 8 lead Plastic Small Outline, 150 mils body width, Package Outline



Drawing is not to scale.