M40SZ100Y
M40SZ100W

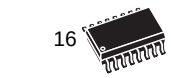
NVRAM SUPERVISOR for LPSRAM

PRELIMINARY DATA

FEATURES SUMMARY

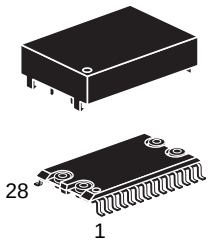
- CONVERT LOW POWER SRAMs INTO NVRAMs
- 3V OR 5V OPERATING VOLTAGE
- PRECISION POWER MONITORING and POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION WHEN V_{CC} is OUT-OF-TOLERANCE
- CHOICE of SUPPLY VOLTAGES and POWER-FAIL DESELECT VOLTAGES:
  - M40SZ100Y: V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.40 ± 0.10V
  - M40SZ100W: V_{CC} = 2.7 to 3.6V; V_{PFD} = 2.65 ± 0.05V
- RESET OUTPUT ($\overline{RST}$) for POWER ON RESET
- 1.25V REFERENCE (for PFI/$\overline{PFO}$)
- LESS THAN 10ns CHIP ENABLE ACCESS PROPAGATION DELAY (at 5V)
- OPTIONAL PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT® TOP (to be Ordered Separately)
- 28-LEAD SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP WHICH CONTAINS THE BATTERY
- BATTERY LOW PIN ($\overline{BL}$)

Figure 1. Packages



SO16 (MQ)

SNAPHAT (SH)
Battery



SOH28 (MH)

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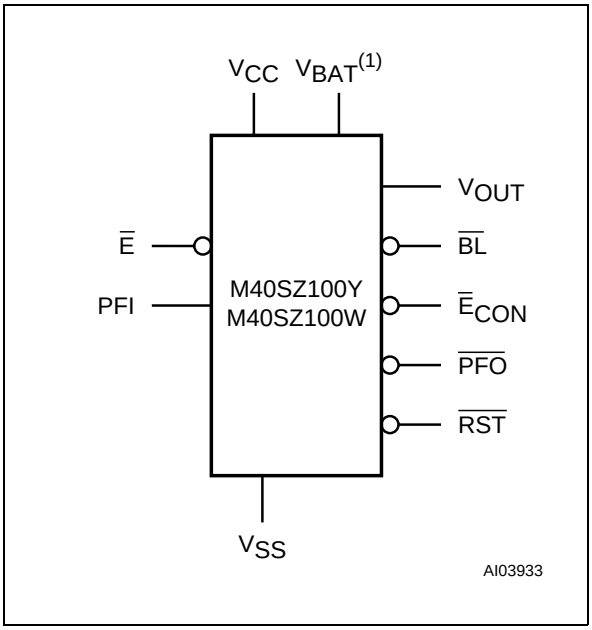
SUMMARY DESCRIPTION

The M40SZ100Y/W NVRAM Controller is a self-contained device which converts a standard low-power SRAM into a non-volatile memory. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition.

When an invalid V_{CC} condition occurs, the conditioned chip enable output ($\overline{E}_{CON}$) is forced inactive to write-protect the stored data in the SRAM. During a power failure, the SRAM is switched from the V_{CC} pin to the lithium cell within the SNAPHAT (or external battery for the 16-lead SOIC) to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns.

The 28 pin, 330 mil SOIC provides sockets with gold plated contacts for direct connection to a separate SNAPHAT housing containing the battery. The SNAPHAT housing has gold plated pins which mate with the sockets, ensuring reliable connection. The housing is keyed to prevent improper insertion. This unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process which greatly reduces the board manufacturing process complexity of either directly soldering or inserting a battery into a soldered holder. Providing non-volatility becomes a "SNAP". Also available in “topless” 16-pin SOIC package (MQ).

Figure 2. Logic Diagram



Note: 1. For 16-pin SOIC package only.

Table 1. Signal Names

$\overline{E}$	Chip Enable Input
$\overline{E}_{CON}$	Conditioned Chip Enable Output
$\overline{RST}$	Reset Output (Open Drain)
$\overline{BL}$	Battery Low Output (Open Drain)
V_{OUT}	Supply Voltage Output
V_{CC}	Supply Voltage
V_{BAT} (1)	Back-up Supply Voltage
PFI	Power Fail Input
$\overline{PFO}$	Power Fail Output
V_{SS}	Ground
NC	Not Connected Internally

Note: 1. For SO16 only.

Figure 3. SOIC16 Connections

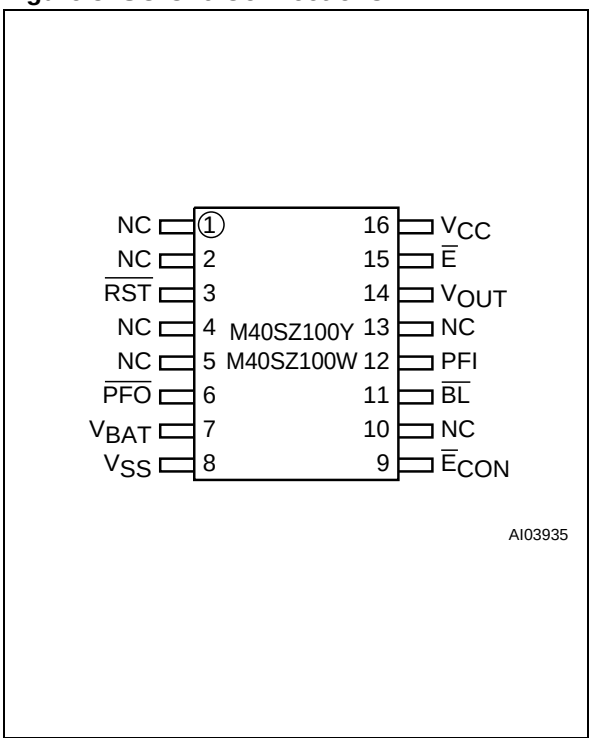


Figure 4. SOIC28 Connections

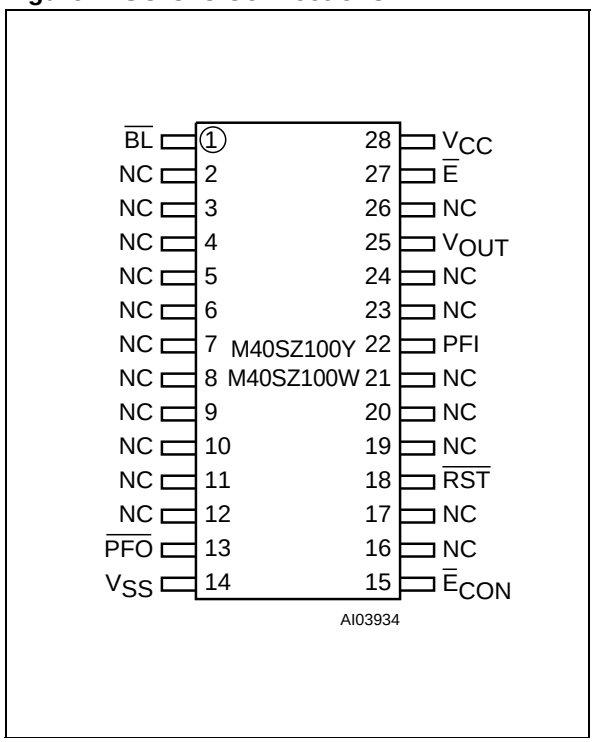
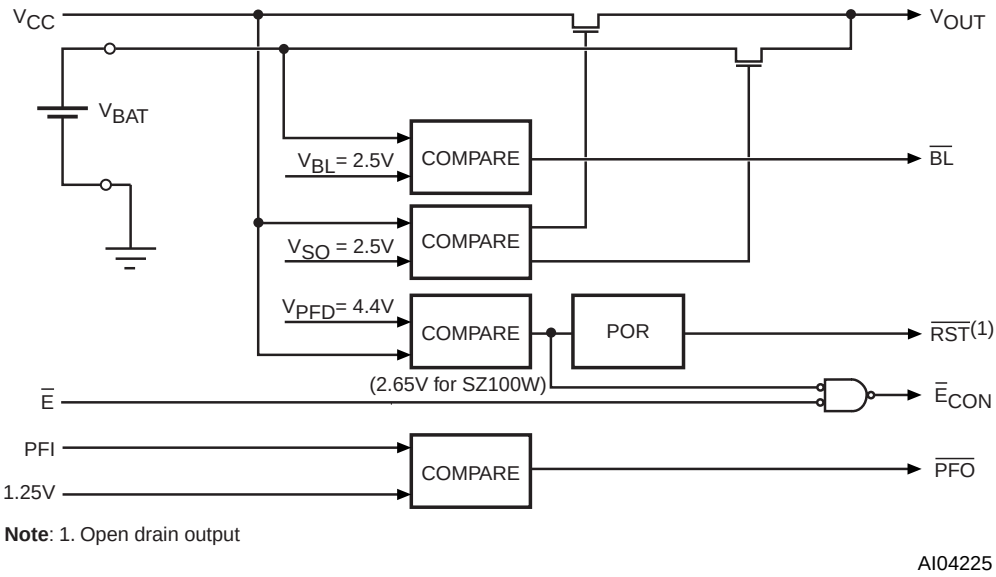
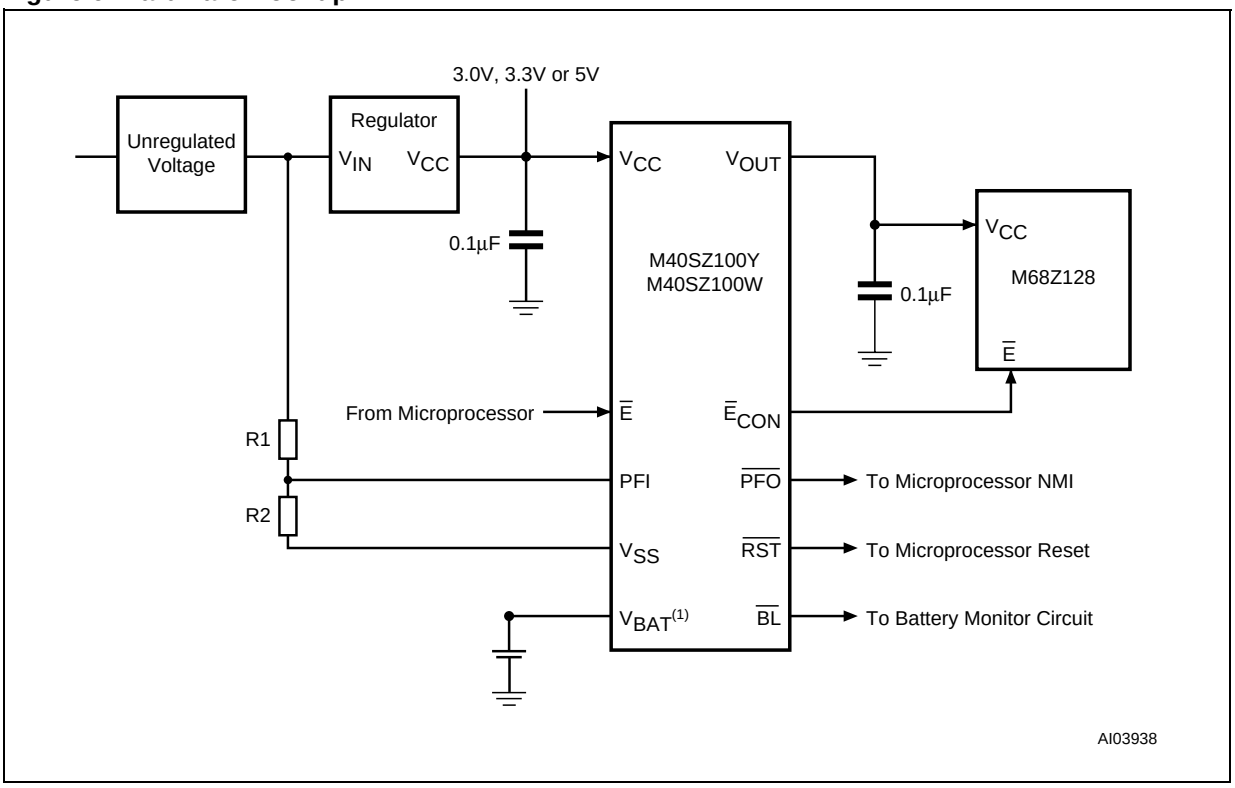


Figure 5. Block Diagram



Note: 1. Open drain output

Figure 6. Hardware Hookup



Note: 1. User supplied for the 16-pin package

OPERATION

The M40SZ100Y/W, as shown in Figure 6, page 5, can control one (two, if placed in parallel) standard low-power SRAM. This SRAM must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ($\overline{E}_{CON}$) output pin follows the chip enable ($\overline{E}$) input pin with timing shown in Table 6, page 12. An internal switch connects V_{CC} to V_{OUT}. This switch has a voltage drop of less than 0.3V (I_{OUT1}).

When V_{CC} degrades during a power failure, $\overline{E}_{CON}$ is forced inactive independent of $\overline{E}$. In this situation, the SRAM is unconditionally write protected as V_{CC} falls below an out-of-tolerance threshold (V_{PFD}). For the M40SZ100Y/W the power fail detection value associated with V_{PFD} is shown in Table 5, page 10.

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time t_{WPT}, $\overline{E}_{CON}$ is unconditionally driven high, write protecting the SRAM. A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below V_{PFD} (min), the user can be assured the memory will be write protected within the Write Protect Time (t_{WPT}) provided the V_{CC} fall time does not exceed t_F (see Table 6, page 12).

As V_{CC} continues to degrade, the internal switch disconnects V_{CC} and connects the internal battery to V_{OUT}. This occurs at the switchover voltage (V_{SO}). Below the V_{SO}, the battery provides a voltage V_{OHB} to the SRAM and can supply current I_{OUT2} (see Table 5, page 10).

When V_{CC} rises above V_{SO}, V_{OUT} is switched back to the supply voltage. Output $\overline{E}_{CON}$ is held inactive for t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{E}$ input, to allow for processor stabilization (see Figure 11, page 12).

Data Retention Lifetime Calculation

Most low power SRAMs on the market today can be used with the M40SZ100Y/W NVRAM Controller. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40SZ100Y/W and SRAMs to be Don't Care once V_{CC} falls below V_{PFD} (min). The SRAM should also guarantee data retention down to V_{CC} = 2.0V. The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{CCDR} value of the M40SZ100Y/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT of your choice (see Table 12, page 17) can then be divided by this current to determine the amount of data retention available.

CAUTION: Take care to avoid inadvertent discharge through V_{OUT} and $\overline{E}_{CON}$ after battery has been attached.

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

Power-on Reset Output

All microprocessors have a reset input which forces them to a known state when starting. The M40SZ100Y/W has a reset output ($\overline{RST}$) pin which is guaranteed to be low by V_{PFD} (see Table 5, page 10). This signal is an open drain configuration. An appropriate pull-up resistor to V_{CC} should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when V_{CC} equals V_{SS} (with valid battery voltage).

Once V_{CC} exceeds the power failure detect voltage V_{PFD}, an internal timer keeps $\overline{RST}$ low for t_{REC} to allow the power supply to stabilize.

Battery Low Pin

The M40SZ100Y/W automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The Battery Low ($\overline{BL}$) pin will be asserted if the battery voltage is found to be less than approximately 2.5V. The $\overline{BL}$ pin will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced.

The M40SZ100Y/W only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The $\overline{BL}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

Power-fail Input/output

The Power-Fail Input (PFI) is compared to an internal reference voltage (independent from the V_{PFD} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the Power-Fail Output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 10, page 11) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the M40SZ100Y/W or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator turns off and $\overline{PFO}$ goes (or remains) low. This occurs after V_{CC} drops below V_{PFD}(min). When power returns, $\overline{PFO}$ is forced high, irrespective of V_{PFI} for the write protect time (t_{REC}), which is the time from V_{PFD}(max) until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to Vss and $\overline{PFO}$ left unconnected.

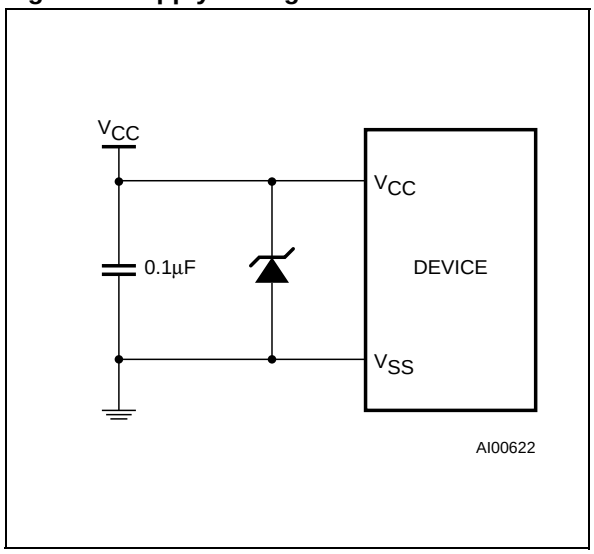
V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur.

A ceramic bypass capacitor value of 0.1µF (as shown in Figure 7, page 7) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 7. Supply Voltage Protection



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off)	SNAPHAT	–40 to 85	°C
		SOIC	–55 to 125	°C
T_{SLD}	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply Voltage	M40SZ100Y	–0.3 to 7	V
		M40SZ100W	–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

CAUTION: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC Measurement Conditions

Parameter	M40SZ100Y	M40SZ100W
V_{CC} Supply Voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient Operating Temperature	–40 to 85°C	–40 to 85°C
Load Capacitance (C_L)	100pF	50pF
Input Rise and Fall Times	≤ 5ns	≤ 5ns
Input Pulse Voltages	0.2 to 0.8V_{CC}	0.2 to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3 to 0.7V_{CC}	0.3 to 0.7V_{CC}

Figure 8. AC Testing Load Circuit

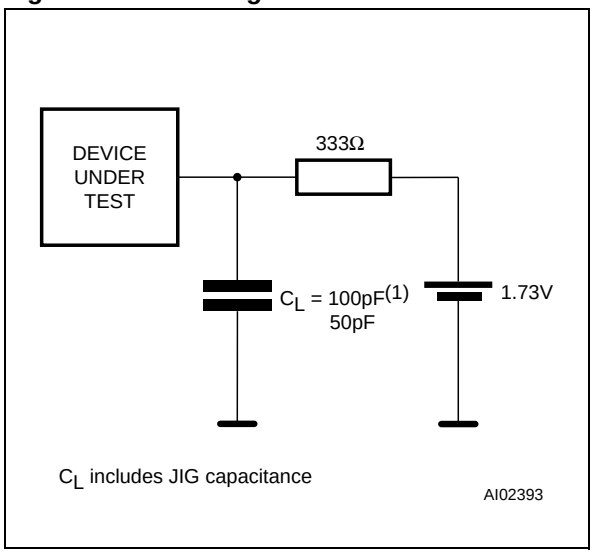
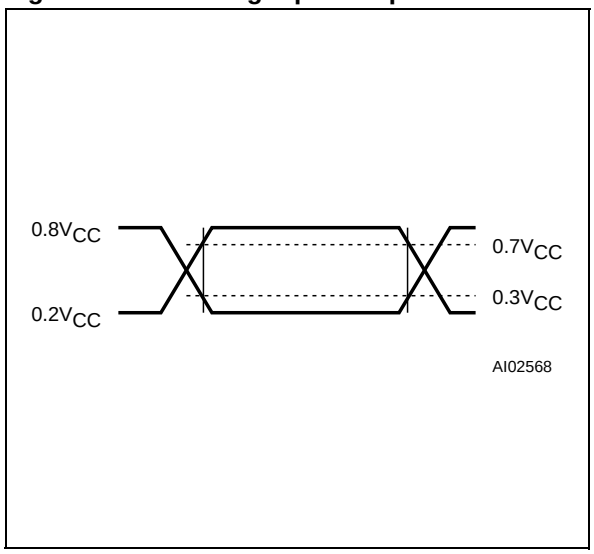


Figure 9. AC Testing Input/Output Waveforms



Note: 1. CL = 100pF for M40SZ100Y and 50pF for M40SZ100W.

Table 4. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		7	pF
C_{OUT}(1)	Output Capacitance	V_{OUT} = 0V		10	pF

Note: Sampled only, not 100% tested.
1. Outputs deselected

Table 5. DC Characteristics

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
I_{CC}	Supply Current	M40SZ100Y	Outputs open			1	mA
		M40SZ100W				0.5	mA
I_{CCDR}	Data Retention Mode Current (4)					100	nA
I_{LI} (1)	Input Leakage Current		$0V \le V_{IN} \le V_{CC}$			±1	µA
	Input Leakage Current (PFI)		$0V \le V_{IN} \le V_{CC}$	–25	2	25	nA
I_{LO} (1)	Output Leakage Current		$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{OUT1}	V_{OUT} Current (Active)		$V_{OUT} > V_{CC} - 0.3$			250	mA
			$V_{OUT} > V_{CC} - 0.2$			100	mA
I_{OUT2}	V_{OUT} Current (Battery Back-up)		$V_{OUT} > V_{BAT} - 0.3$		100		µA
V_{BAT}	Battery Voltage	M40SZ100Y		2.0	3.0	3.5(5)	V
		M40SZ100W			3.0		V
V_{IH}	Input High Voltage			$0.7V_{CC}$		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage			–0.3		$0.3V_{CC}$	V
V_{OH}	Output High Voltage		$I_{OH} = -1.0mA$	2.4			V
V_{OHB}	V_{OH} Battery Back-up (3)		$I_{OUT2} = -1.0\mu A$	2.0	2.9	3.6	V
V_{OL}	Output Low Voltage		$I_{OL} = 3.0mA$			0.4	V
	Output Low Voltage (open drain)(2)		$I_{OL} = 10mA$			0.4	V
V_{PFD}	Power-fail Deselect Voltage	M40SZ100Y		4.30	4.40	4.50	V
		M40SZ100W		2.60	2.65	2.70	V
V_{PFI}	PFI Input Threshold			1.225	1.250	1.275	V
V_{SO}	Battery Back-up Switchover Voltage				2.5		V

Note: 1. Outputs deselected.
2. For $\overline{RST}$ & $\overline{BL}$ pins (Open Drain).
3. Chip Enable output ($\overline{E}_{CON}$) can only sustain CMOS leakage currents in the battery back-up mode. Higher leakage currents will reduce battery life.
4. Measured with V_{OUT} and $\overline{E}_{CON}$ open.
5. For rechargeable back-up, V_{BAT} (max) may be considered $V_{CC} - 0.5V$.

Figure 10. Power Down Timing

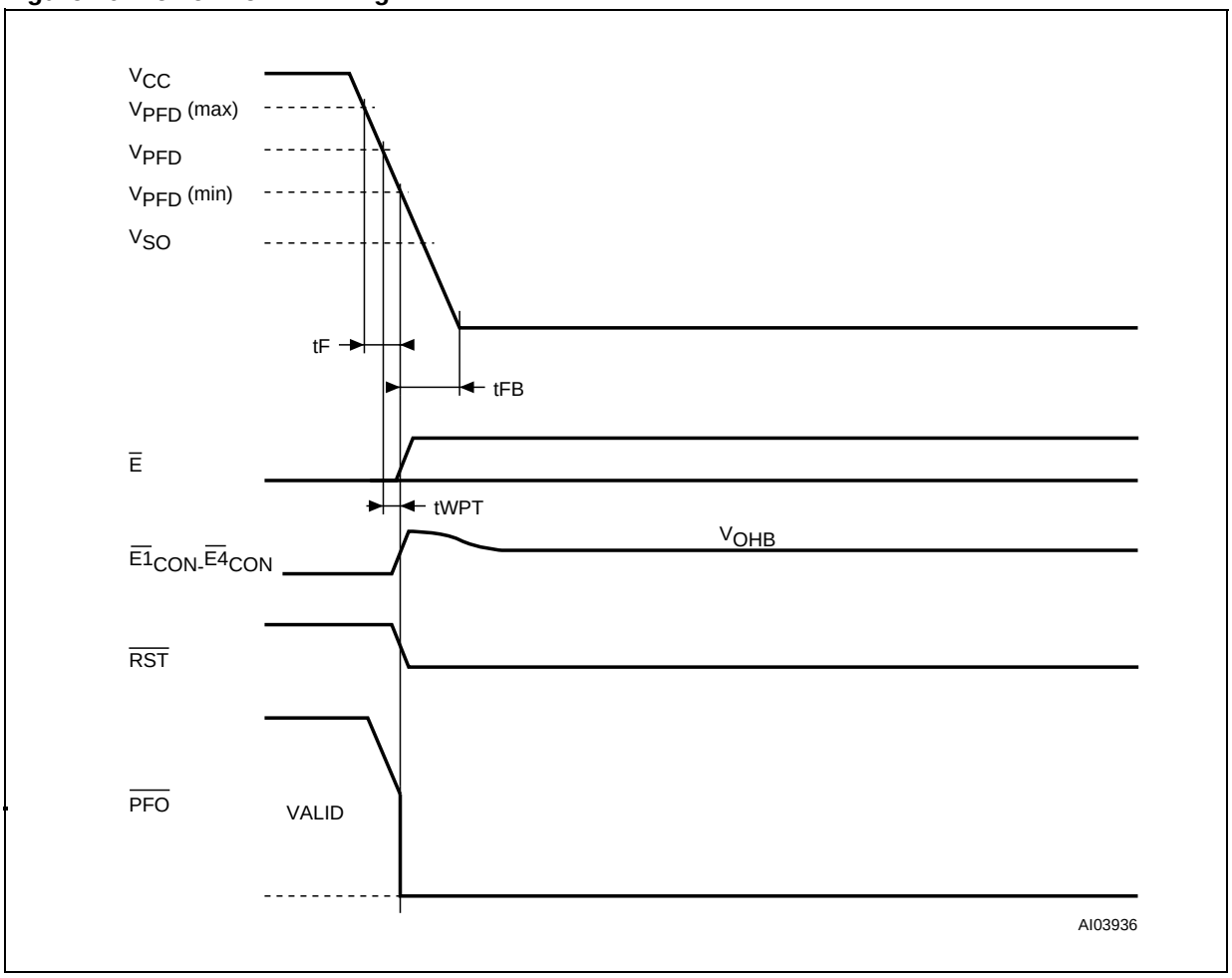


Figure 11. Power Up Timing

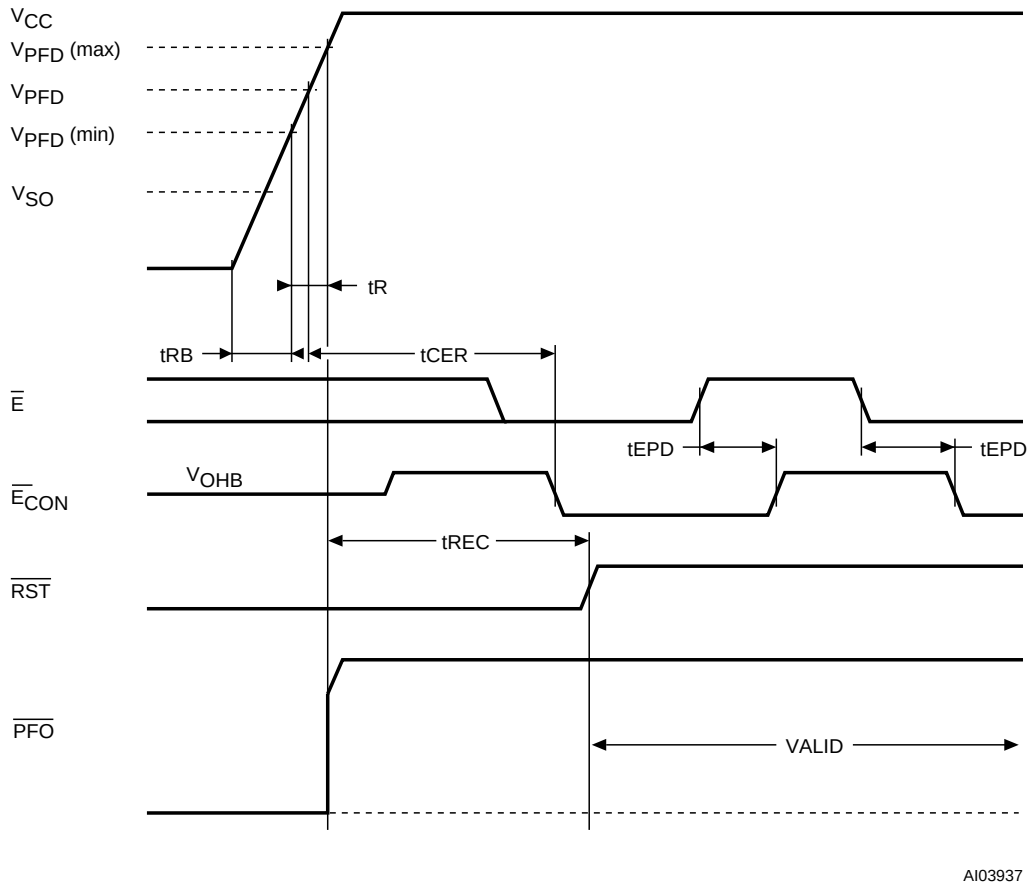


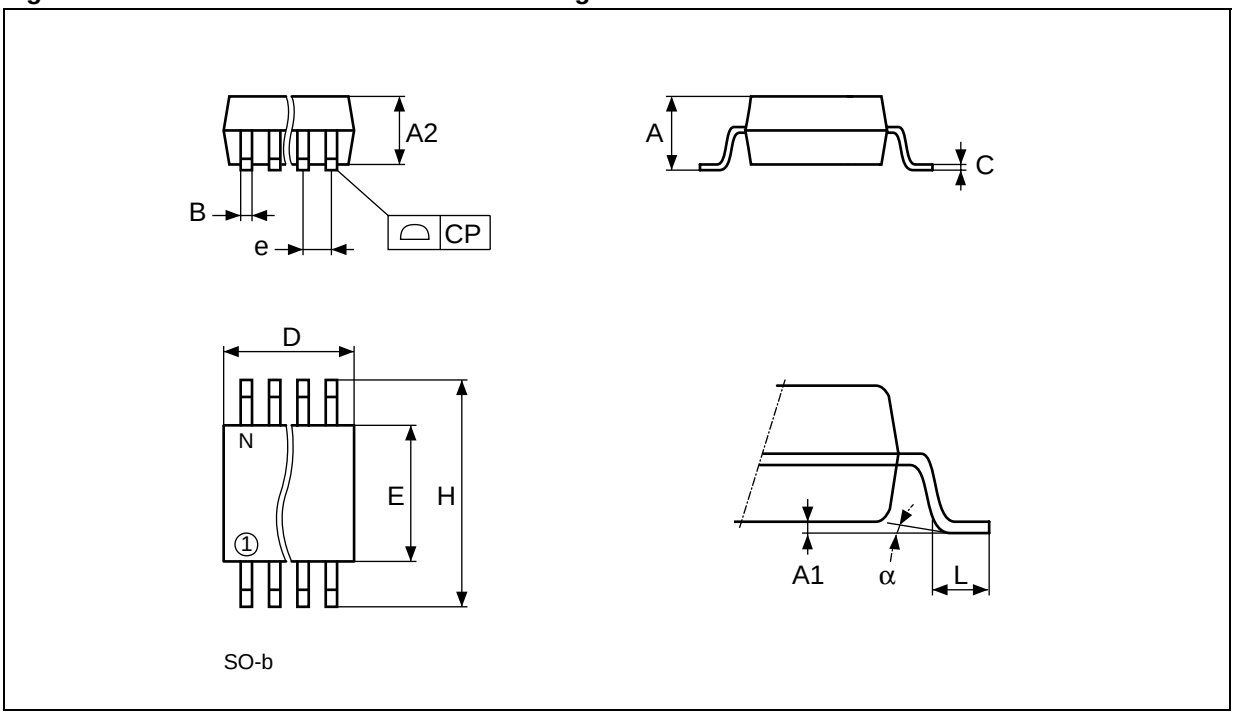
Table 6. Power Down/Up AC Characteristics

Symbol	Parameter		Min	Max	Unit
t_F(1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time		300		µs
t_{FB}(2)	V_{PFD} (min) to V_{SS} V_{CC} Fall Time		10		µs
t_{PFD}	PFI to $\overline{PFO}$ Propagation Delay		15	25	ns
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time		10		µs
t_{EPD}	Chip Enable Propagation Delay (Low or High)	M40SZ100Y		10	ns
		M40SZ100W		15	ns
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time		1		µs
t_{CER}	Chip Enable Recovery		40	120	ms
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High		40	200	ms
t_{WPT}	Write Protect Time		40	200	µs

Note: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than tF may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SS} fall time of less than tFB may cause corruption of RAM data.

PACKAGE MECHANICAL

Figure 12. SO16 - 16 lead Plastic Small Package Outline

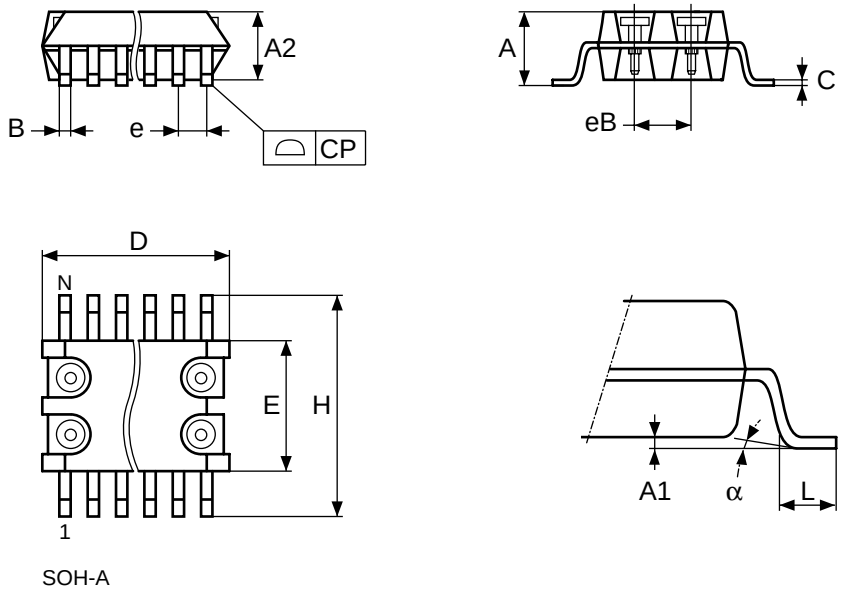


Note: Drawing is not to scale.

Table 7. SO16 - 16 lead Plastic Small Plastic Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.80	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

Figure 13. SOH28 - 28 lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline

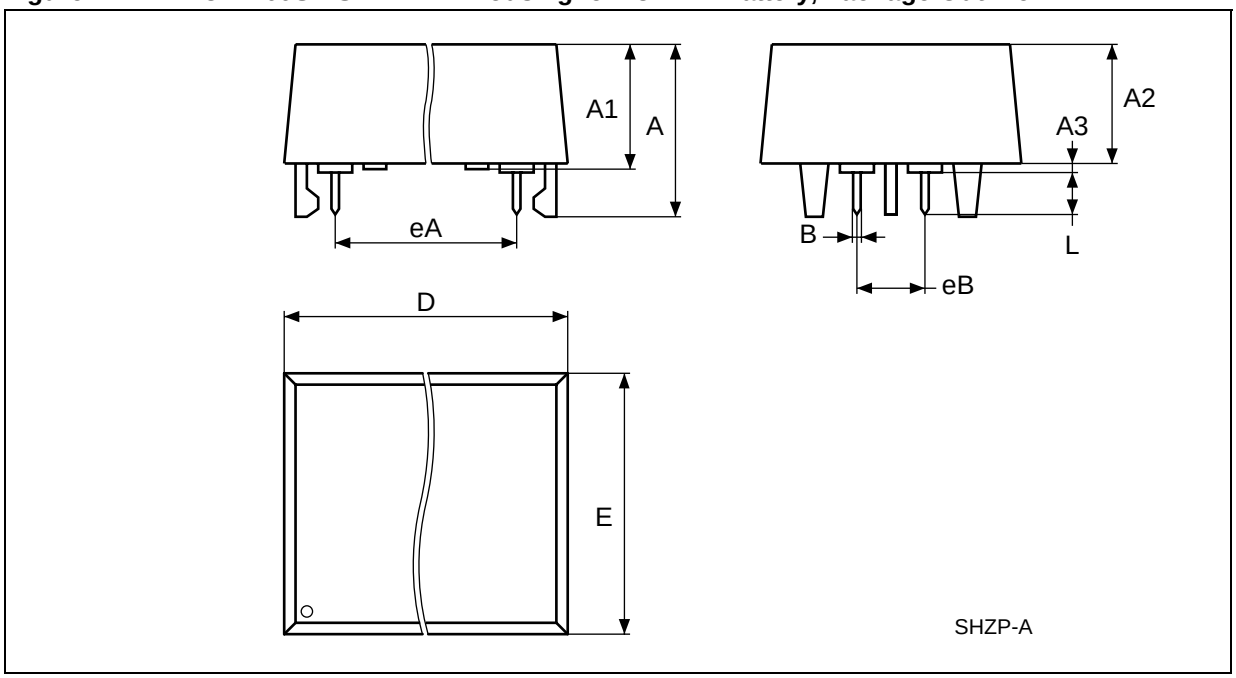


Note: Drawing is not to scale.

Table 8. SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 14. M4Z28-BR00SH SNAPHAT Housing for 48 mAh Battery, Package Outline

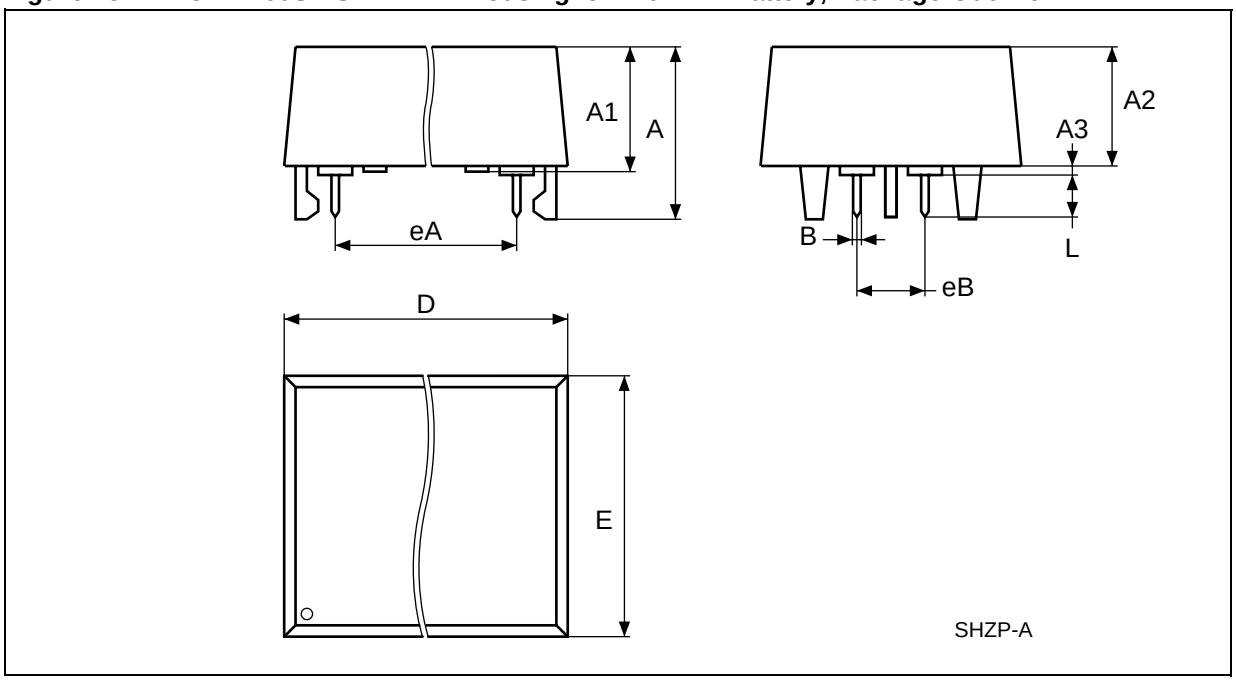


Note: Drawing is not to scale.

Table 9. M4Z28-BR00SH SNAPHAT Housing for 48 mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 15. M4Z32-BR00SH SNAPHAT Housing for 120 mAh Battery, Package Outline



Note: Drawing is not to scale.

Table 10. M4Z32-BR00SH SNAPHAT Housing for 120 mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M40SZ 100Y MH 6 TR

Device Type

M40SZ

Supply Voltage and Write Protect Voltage

100Y = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.3 to 4.5V

100W = V_{CC} = 2.7 to 3.6V; V_{PFD} = 2.6 to 2.7V

Package

MQ = SO16

MH(1) = SOH28

Temperature Range

6 = –40 to 85°C

Shipping Method for SOIC

blank = Tubes

TR = Tape & Reel

Note: 1. The SOIC package (SOH28) requires the battery package (SNAPHAT) which is ordered separately under the part number “M4ZXX-BR00SHX" in plastic tube or "M4ZXX-BR00SHXTR" in Tape & Reel form.

Caution: Do not place the SNAPHAT battery package "M4Zxx-BR00SH1" in conductive foam since will drain the lithium button-cell battery.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. Battery Table

Part Number	Description	Package
M4Z28 – BR00SH	SNAPHAT Housing for 48 mAh Battery	SH
M4Z32 – BR00SH	SNAPHAT Housing for 120 mAh Battery	SH

REVISION HISTORY

Table 13. Document Revision History

Date	Revision Details
September 2000	First Draft Issue
12/18/00	Reformatted, TOC added, and PFI Input Leakage Current added (Table 5)