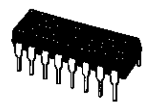
SGS-THOMSON MICROELECTRONICS

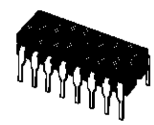
HCC/HCF4046B

MICROPOWER PHASE-LOCKED LOOP

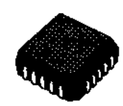
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- VERY LOW POWER CONSUMPTION : 100µW (TYP.) AT VCO f_0 = 10kHz, V_{DD} = 5V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT V_{DD} = 10V
- LOW FREQUENCY DRIFT : 0.06%/°C (typ.) AT V_{DD} = 10V
- CHOICE OF TWO PHASE COMPARATORS :
  1) EXCLUSIVE - OR NETWORK
  2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY : 1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



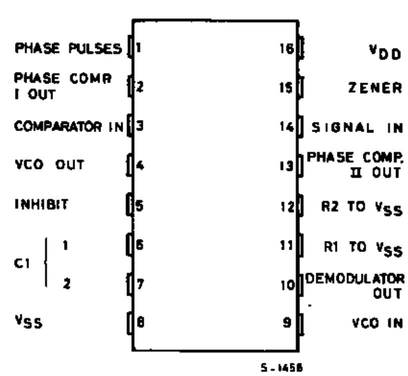
F
(Ceramic Package)



C1
(Chip Carrier)

ORDER CODES :
HCC4046BF HCF4046BEY
HCF4043BC1

PIN CONNECTIONS



DESCRIPTION

The **HCC4046B** (extended temperature range) and **HCF4046B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF4046B** COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12\Omega}$) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the **HCC/HCF4024B**, **HCC/HCF4018B**, **HCC/HCF4020B**, **HCC/HCF4022B**, **HCC/HCF4029B**,and **HBC/HBF4059A**. One or more **HCC/HCF4018B** (Presettable Divide-by-N Counter) or **HCC/HCF4029B** (Presettable Up/Down Counter), or **HBC/HBF4059A** (Programmable Divide-by-"N" Counter), together with the **HCC/HCF4046B** (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤ 30 % (V_{DD} – V_{SS}), logic "1" ≥ 70 % (V_{DD} - V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network ; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2 f_c$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2 f_L$). The capture range is ≤ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in fig. (b). Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

Figure a : Phase-Comparator I Characteristics at Low-Pass Filter Output.

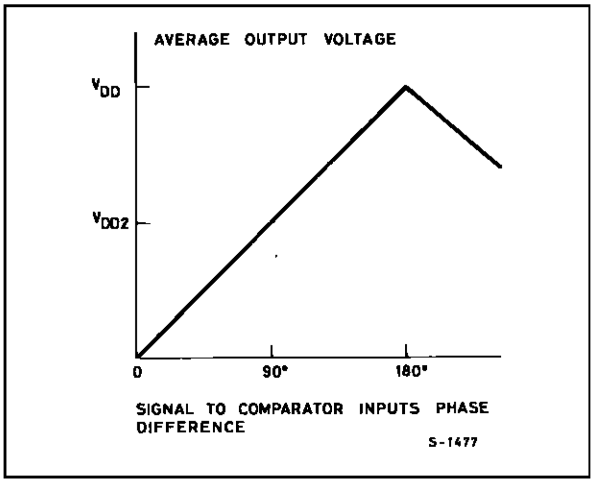


Figure b : Typical Waveforms for COS/MOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of f_o.

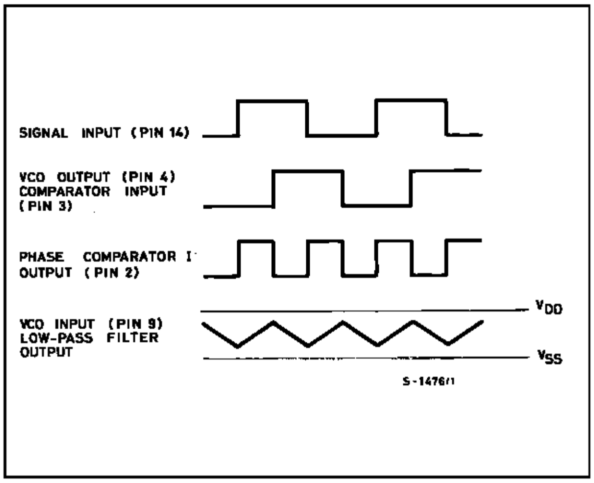
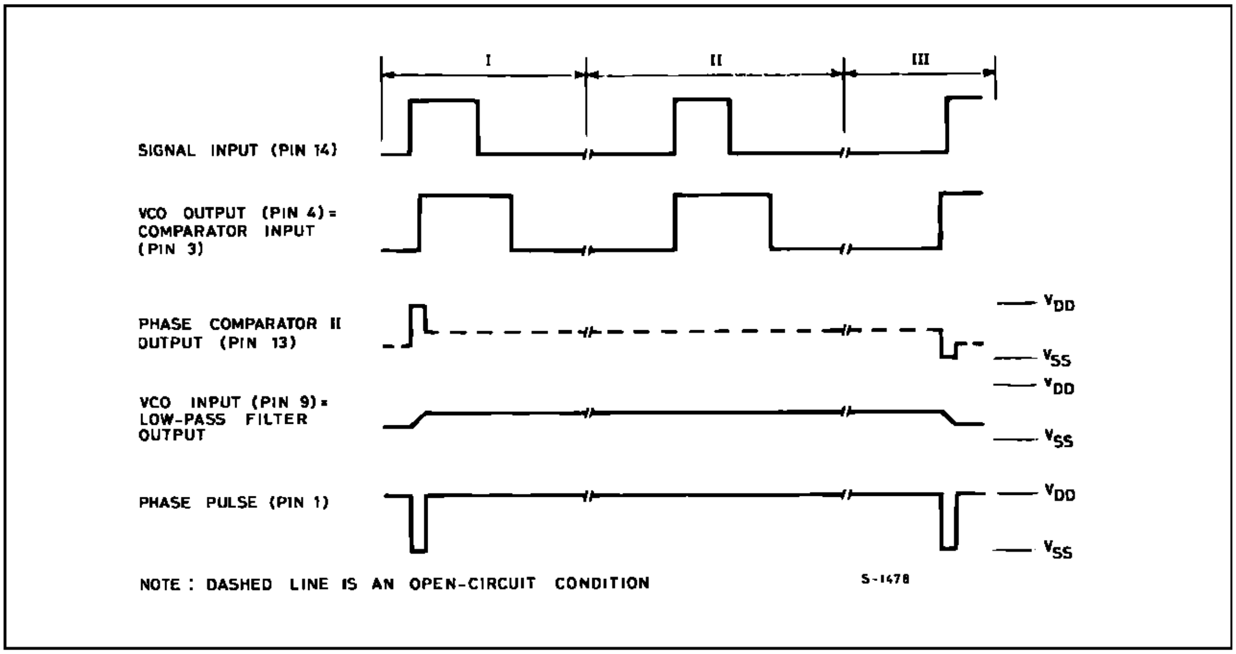
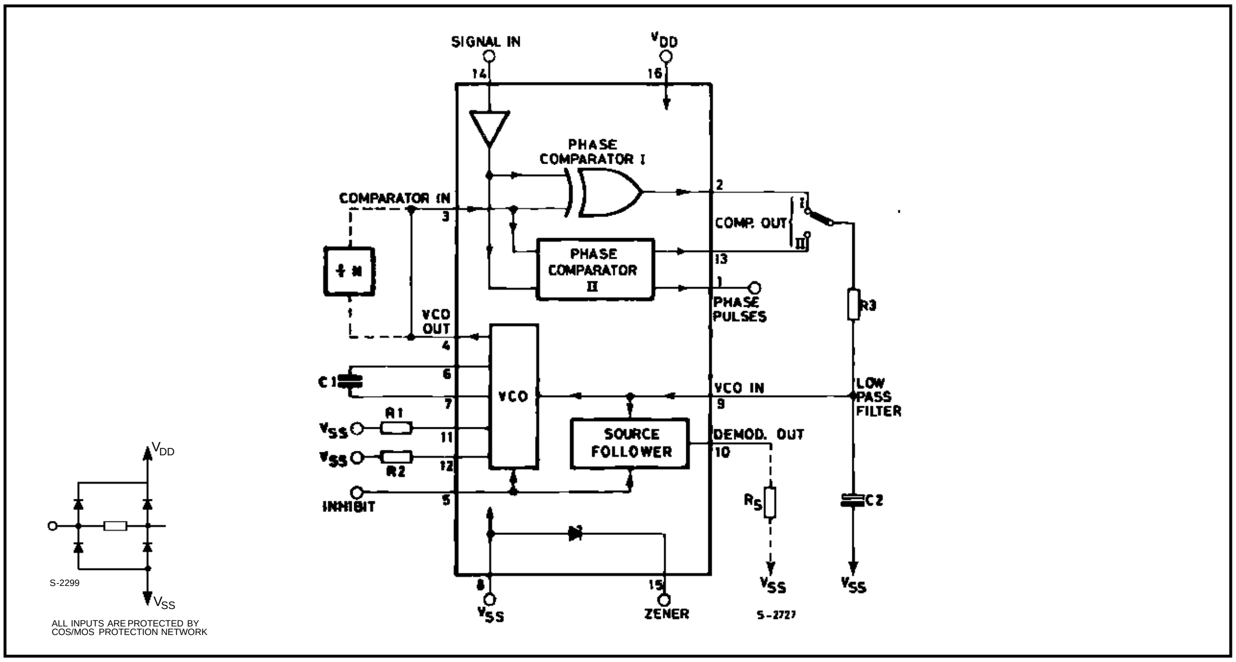


Figure C : Typical Waveforms For COS/MOS Phase-locked Loop Employing Phase Comparator II In Locked Condition.



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	– 0.5 to + 20 – 0.5 to + 18	V V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	°C °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
VCO SECTION														
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95	5		4.95		V
			0/10		< 1	10	9.95		9.95	10		9.95		
			0/15		< 1	15	14.95		14.95	15		14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
PHASE COMPARATOR SECTION														
I_{DD}	Total Device Current Pin 14 = Open Pin 5 = V_{DD}		0/ 5			5		0.1		0.05	0.1		0.1	mA
			0/10			10		0.5		0.25	0.5		0.5	
			0/15			15		1.5		0.75	1.5		1.5	
			0/20			20		4		2	4		4	
	Pin 14 = V_{SS} or V_{DD} Pin 5 = V_{DD}	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/ 5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/ 5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	Value T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{IH}, I_{IL}	Input Leakage Current (except. pin 14)	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	µA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
I_{OUT}	3-state Leakage Current	HCC Types	0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	µA
		HCF Types	0/15	0/15		15		± 1.0		$\pm 10^{-4}$	± 1.0		± 7.5	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{Low} = – 55°C for **HCC** device : – 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

ELECTRICAL CARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
VCO SECTION							
P_D	Operating Power Dissipation	fo = 10 KHz R1 = 10 MΩ R2 = ∞ $V_{COIN} = \frac{V_{DD}}{2}$	5		70	140	µW
			10		800	1600	
			15		3000	6000	
f_{max}	Maximum Frequency	R1 = 10 KΩ C1 = 50 pF R2 = ∞ V_{COIN} = V_{DD}	5	0.3	0.6		MHz
			10	0.6	1.2		
			15	0.8	1.6		
		R1 = 5 KΩ n C1 = 50 pF R2 = ∞ V_{COIN} = V_{DD}	5	0.5	0.8		
			10	1	1.4		
			15	1.4	2.4		
	Center Frequency (f_o) and Frequency Range f_{max} - f_{min}	Programmable with external components R1, R2 and C1					
	Linearity	V_{COIN}=2.5V $^{\pm 0.3}$ R1=10 KΩ	5		1.7		%
		V_{COIN}=5V $^{\pm 1}$ R1=100 KΩ	10		0.5		
		V_{COIN}=5V $^{\pm 2.5}$ R1=400 KΩ	10		4		
		V_{COIN}=7.5V $^{\pm 1.5}$ R1=100 KΩ	15		0.5		
		V_{COIN}=7.5V $^{\pm 5}$ R1=1 MΩ	15		7		
	Temperature Frequency Stability (no frequency offset) f_{min} = 0		5		±0.12		%/°C
			10		±0.04		
			15		±0.015		
	Temperature Frequency Stability (frequency offset) $f_{min} \neq 0$		5		±0.09		
			10		±0.07		
			15		±0.03		
V_{CO}	Output Duty Cycle		5, 10, 15		50		%
t_{THL} t_{TLH}	VCO Output Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
	Source Follower Output (demodulated Output): Offset Voltage V_{COIN} - V_{DEM}	R_S > 10 KΩ	5, 10, 15		1.8	2.5	V
	Source Follower Output (demodulated Output): Linearity	R_S=100 KΩ V_{COIN}=2.5$^{\pm 0.3}$V	5		0.3		%
		R_S=300 KΩ V_{COIN}=5$^{\pm 2.5}$V	10		0.7		
		R_S=500 KΩ V_{COIN}=7.5$^{\pm 5}$V	15		0.9		
V_Z	Zener Diode Voltage	I_Z = 50 µA		4.45	5.5	7.5	V
R_Z	Zener Dynamic Resistance	I_Z = 1 mA			40		Ω
PHASE COMPARATOR SECTION							
R14	Pin 14 (signal in) Input Resistance		5	1	2		MΩ
			10	0.2	0.4		
			15	0.1	0.2		
	A.C. Coupled Signal Input Voltage Sensitivity * (peak to paek)	f_{in} = 100 KHz sine wave	5	180	360		mV
			10	330	660		
			15	900	1800		

ELECTRICAL CHARACTERISTICS (continued)

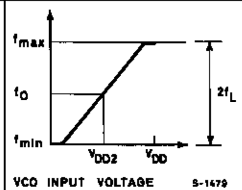
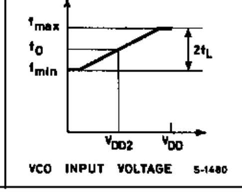
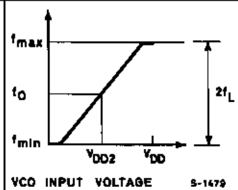
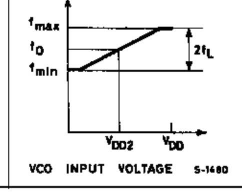
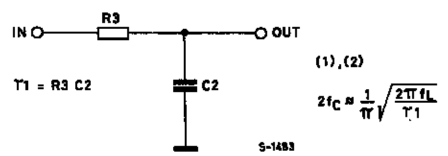
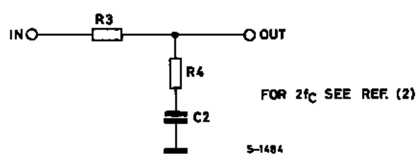
Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
PHASE COMPARATOR SECTION (cont'd)							
T_{PHL}	Propagation Delay Time High to Low Level Pins 14 to 13		5	225	450		ns
			10	100	200		
			15	65	130		
T_{PLH}	Propagation Delay Time Low to High, Level		5		350	700	ns
			10		150	300	
			15		100	200	
T_{PHZ}	Propagation Delay Time 3-state High Level to High Impedance Pins 14 to 13		5		225	450	ns
			10		100	200	
			15		65	130	
T_{PLZ}	Low Level to High Impedance		5		285	570	ns
			10		130	260	
			15		95	190	
t_r, t_f	Input Rise or Fall Time Comparator Pin 3		5			50	µs
			10			1	
			15			0.3	
	Signal Pin 14		5			500	µs
			10			20	
			15			2.5	
T_{THL}, T_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	

* For sine wave the frequency must be greater than $10KH_Z$ for Phase Comparator II.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the **HCC/HCF 4046B** in a Phase-Locked-Loop system. The selected external components must be within the following ranges :

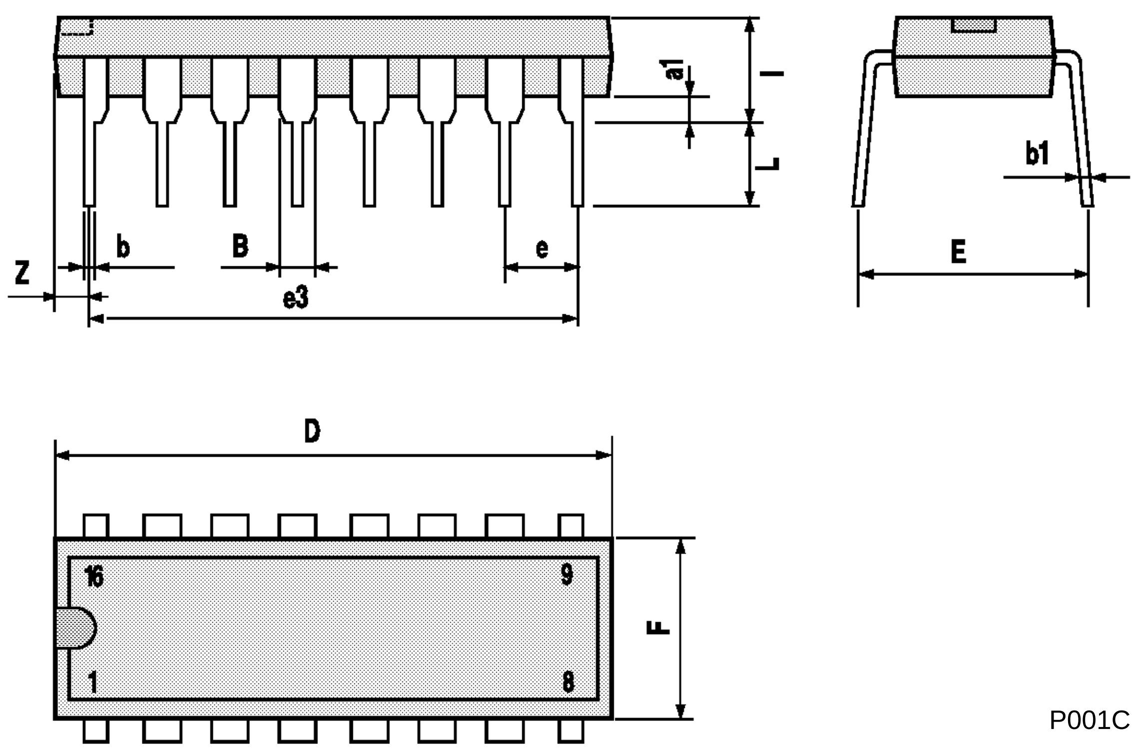
$5k\Omega \leq R1, R2, R_S \leq 1M\Omega$ $C1 \geq 100pF$ at $V_{DD} \geq 5V$ $C1 \geq 50pF$ at $V_{DD} \geq 10V$

<table>
<tr><th rowspan="2">CHARACTERISTICS</th><th colspan="2">USING PHASE COMPARATOR I</th><th colspan="2">USING PHASE COMPARATOR II</th></tr>
<tr><th>VCO WITHOUT OFFSET R2 = ∞</th><th>VCO WITH OFFSET</th><th>VCO WITHOUT OFFSET R2 = ∞</th><th>VCO WITH OFFSET</th></tr>
<tr><td>VCO Frequency</td><td></td><td></td><td></td><td></td></tr>
<tr><td>For No Signal Input</td><td colspan="2">VCO in PLL System will Adjust to centre frequency f_o</td><td colspan="2">VCO in PLL System will Adjust to Lowest Operating Frequency f_{min}</td></tr>
<tr><td>Frequency Lock Range, 2 f_L</td><td colspan="4">2 f_L = full VCO frequency range
$2 f_L = f_{max} - f_{min}$</td></tr>
<tr><td>Frequency Capture Range, 2 f_C</td><td colspan="2"></td><td colspan="2" rowspan="2">$f_C = f_L$</td></tr>
<tr><td>Loop Filter Component Selection</td><td colspan="2"></td></tr>
<tr><td>Phase Angle Between Signal and Comparator</td><td colspan="2">90^o at Centre Frequency (f_o), approximating 0^o and 180^o at ends of lock range (2 f_L)</td><td colspan="2">Always 0^o in lock</td></tr>
<tr><td>Locks on Harmonics of Centre Frequency</td><td colspan="2">Yes</td><td colspan="2">No</td></tr>
<tr><td>Signal Input Noise Rejection</td><td colspan="2">High</td><td colspan="2">Low</td></tr>
</table>

* G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ, may 1965

Plastic DIP16 (0.25) MECHANICAL DATA

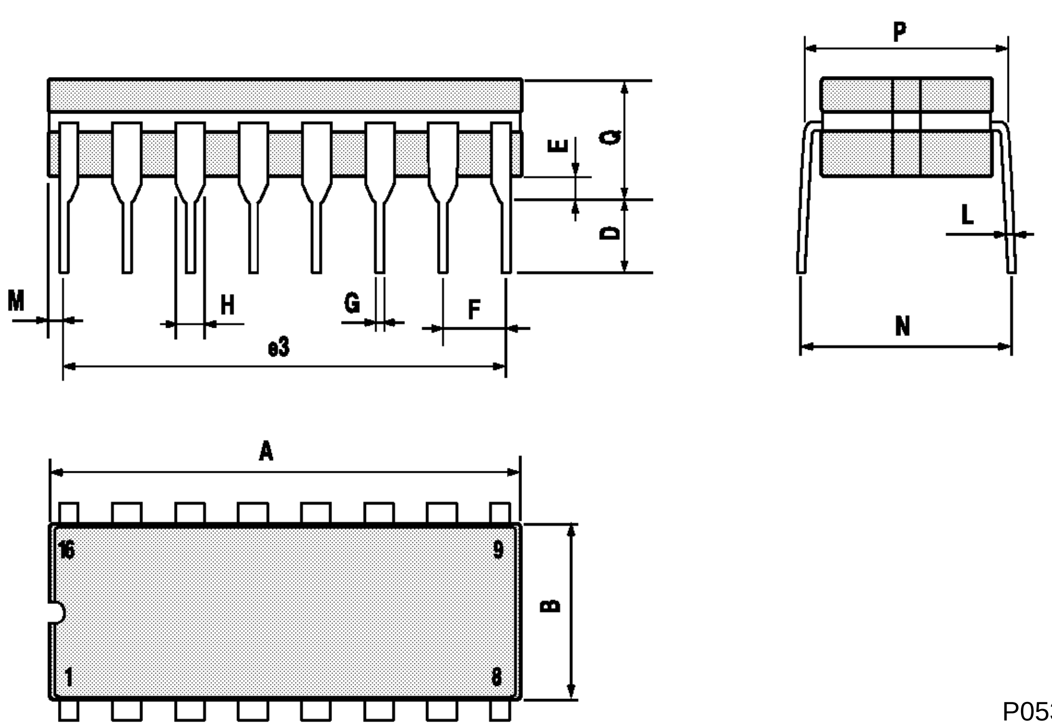
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053D

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045