M7020

32 Kbit x 68 bit Entry Network Search Engine

FEATURES SUMMARY

- 32K ENTRIES IN 68-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO FOUR (4) QUADRANTS
  (Data entry width in each quadrant is configurable as 34, 68, 136, or 272 bits.)
- UP TO 66 MILLION SUSTAINED SEARCHES PER SECOND IN 68-BIT and 136-BIT CONFIGURATIONS
- UP TO 33 MILLION SEARCHES PER SECOND IN 34-BIT and 272-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 248K to 1984K DEPENDING ON THE SIZE OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE:
  V_{DD} (Operating Supply Voltage) = 1.8V
  V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 272 BALL, 27mm x 27mm, CAVITY-UP BGA

Figure 1. Package

272 PBGA
27mm x 27mm
1.27mm ball pitch
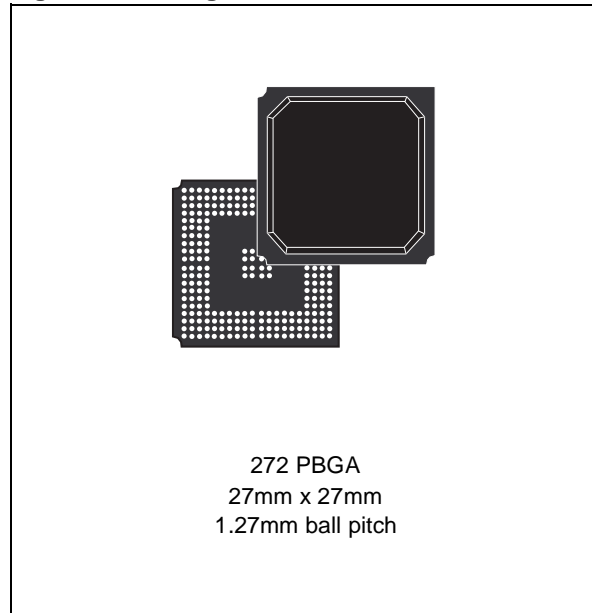
DESCRIPTION

Overview

The M7020 is a feature-rich hardware search engine optimized for networking and communications applications. It incorporates leading-edge Associative Processing Technology (APT, trademark of Lara Networks, Inc.) and Advanced Power Management. The data table may be partitioned into up to four (4) quadrants, allowing the user to configure each quadrant with different table entry widths (x34, x68, x136, or x272-bit). It is also programmable to accelerate performance.

Performance

The M7020 outperforms competitive solutions using software sequential search algorithms in conjunction with SRAMs or ASICs, or hardware implementation with ASICs and CAMs. The latter solution, while faster than a software-based solution, still suffers from performance degradation when depth-cascaded and is unable to scale to next-generation requirements. The M7020-based solutions overcome all of these drawbacks.

Applications

The performance and features of the M7020 makes it ideal in applications such as enterprise LAN switches, broadband switching and routing equipment, supporting multiple data rates from OC–48 and beyond.

Figure 2 illustrates how a search engine subsystem can be optimized using a host bridge ASIC (or a dedicated co-processor, such as the Lara Networks LNI8010), the M7020, and synchronous or non-synchronous SRAMs. It also illustrates how this system fits into a switch-router implementation.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed
M7020R-066ZA1	1.8V	2.5 or 3.3V	66MHz
M7020R-050ZA1	1.8V	2.5 or 3.3V	50MHz

Figure 2. Switch/Router Implementation Using the M7020
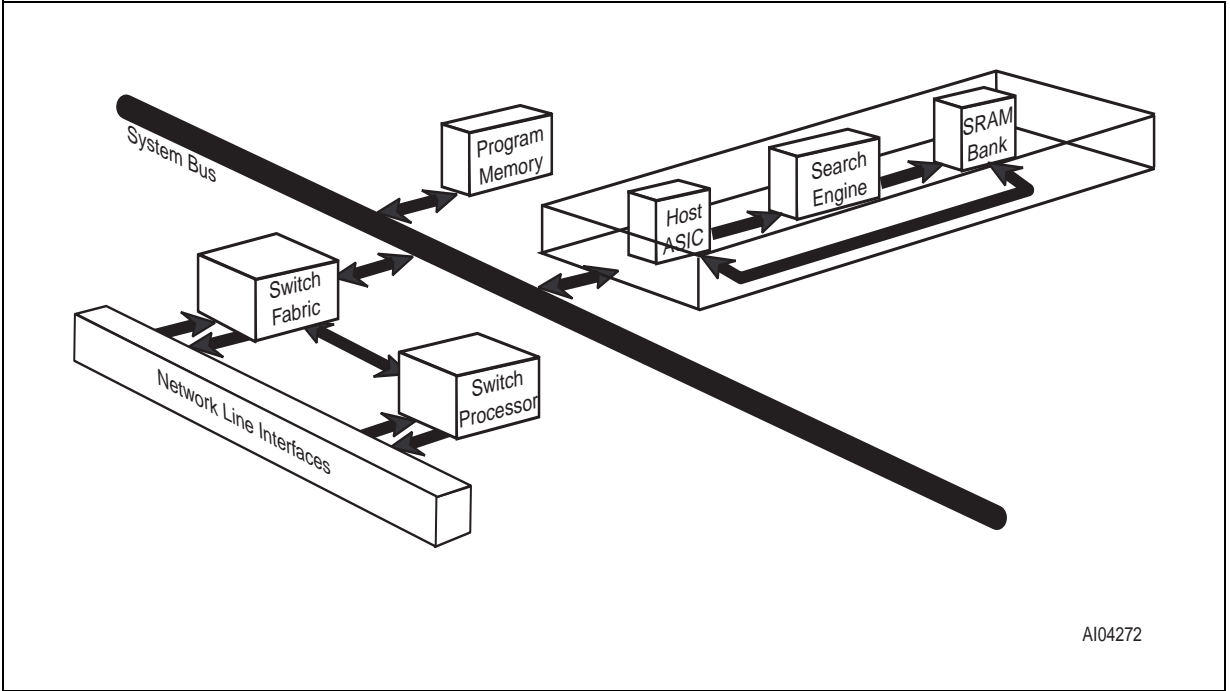
AI04272

Table 2. Signal Names

Clocks and Reset	
CLK2X	Master Clock
PHS_L	Phase
RST_L	Reset
Command and DQ Bus	
CMD[8:0]	Command Bus
CMDV	Command Valid
DQ[67:0]	Address/Data Bus
ACK	READ Acknowledge
EOT	End of Transfer
SSF	Search Successful Flag
SSV	Search Successful Flag Valid
SADR[21:0]	SRAM Address
CE_L	SRAM Chip Enable
WE_L	SRAM Write Enable
OE_L	SRAM Output Enable
ALE_L	Address Latch Enable

Cascade Interface	
LHI[6:0]	Local Hit In
LHO[1:0]	Local Hit Out
BHI[2:0]	Block Hit In
BHO[2:0]	Block Hit Out
FULI[6:0]	Full In
FULO[1:0]	Full Out
FULL	Full Flag
Device Identification	
ID[4:0]	Device Identification
Test Access Port	
TDI	Test Access Port's Test Data In
TCK	Test Access Port's Test Clock
TDO	Test Access Port's Test Data Out
TMS	Test Access Port's Test Mode Select
TRST_L	Test Access Port's Reset

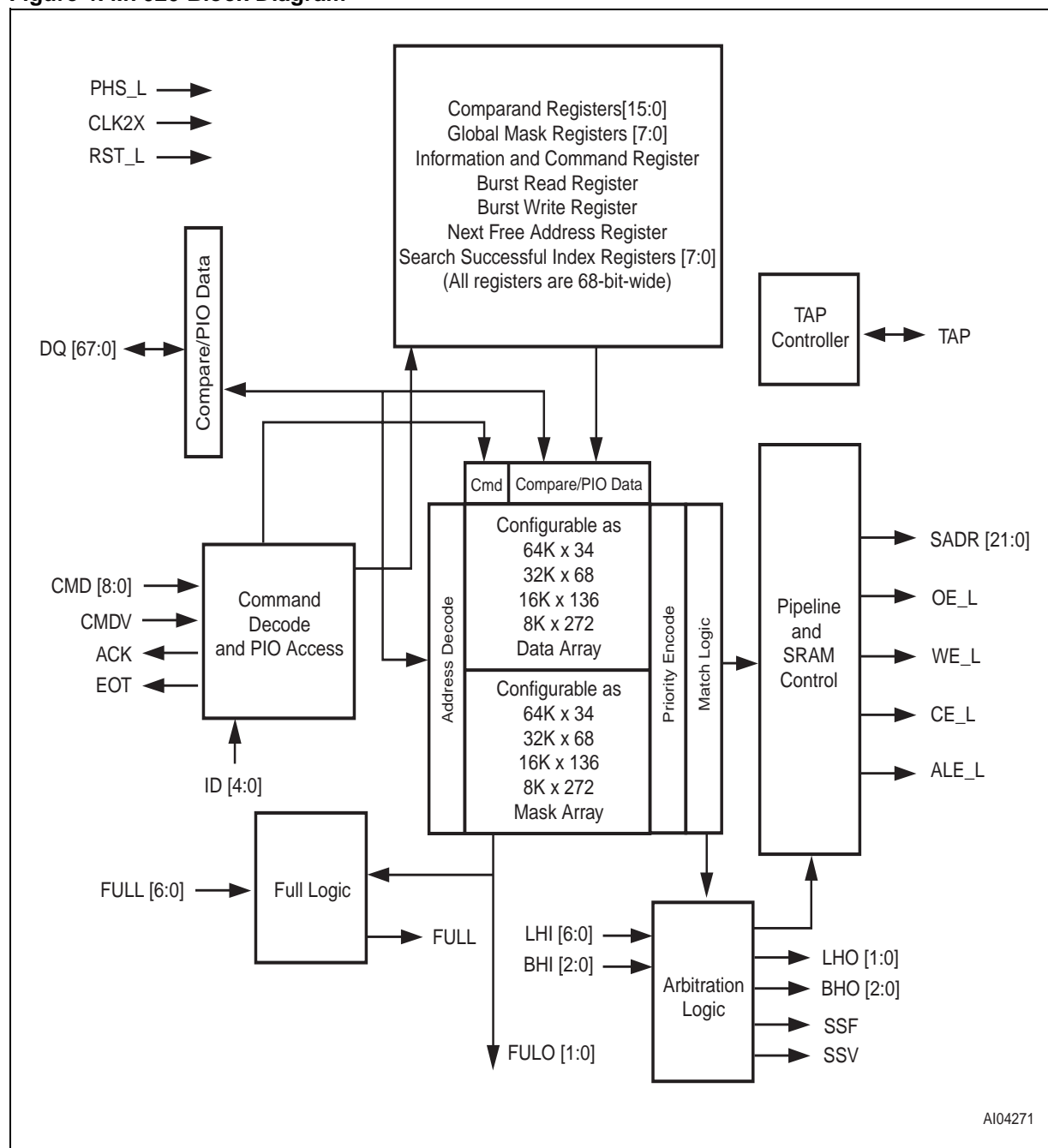Note: Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate
1. ACK and EOT Signals require a pull-down resistor of 47 ohms.

Figure 3. Connections

NC	GND	EOT	NC	NC	V_{DD}	FULI5	FULI4	FULI1	BHO0	V_{DD}	BHI0	LHI6	NC	V_{DD}	ID2	ID0	TDO	NC	NC
NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	BHO1	BHI2	V_{DDQ}	LHI5	LHI3	LHI2	ID3	TMS	TDI	V_{DD}	NC
DQ64	NC	NC	V_{DDQ}	V_{DD}	V_{DDQ}	NC	NC	V_{DDQ}	BHO2	V_{DD}	LHO1	LHI4	V_{DDQ}	LHI0	ID1	TCK	NC	NC	DQ65
DQ62	NC	V_{DD}	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	T RST_L	GND	DQ63	DQ61	DQ57
DQ60	V_{DDQ}	NC	DQ66				TOP									DQ67	DQ59	NC	DQ53
V_{DD}	NC	DQ56	DQ58													V_{DDQ}	DQ55	DQ49	V_{DD}
DQ50	V_{DDQ}	DQ52	DQ54													DQ47	V_{DDQ}	DQ51	V_{DDQ}
NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ43
DQ40	DQ42	V_{DDQ}	DQ44			GND	GND	GND	GND							DQ41	DQ39	V_{DD}	DQ37
V_{DD}	NC	DQ36	DQ38	LEFT		GND	GND	GND	GND							V_{DDQ}	DQ35	DQ33	DQ31
V_{DDQ}	DQ34	DQ32	DQ30			GND	GND	GND	GND		RIGHT					V_{DDQ}	NC	DQ29	V_{DD}
NC	DQ28	V_{DDQ}	DQ26			GND	GND	GND	GND							NC	DQ23	DQ25	DQ27
DQ24	V_{DD}	DQ20	GND													GND	DQ19	V_{DDQ}	DQ21
DQ22	DQ16	DQ14	V_{DDQ}													V_{DDQ}	NC	DQ15	DQ17
V_{DD}	DQ18	V_{DDQ}	DQ6													DQ9	DQ11	DQ13	V_{DD}
NC	DQ12	DQ8	DQ0				BOTTOM									DQ1	DQ5	DQ7	NC
DQ10	NC	V_{DDQ}	GND	NC	CMD2	CMD4	GND	WE_L	CLK2X	V_{DD}	SADR 15	GND	V_{DDQ}	SADR 5	V_{DDQ}	GND	NC	NC	V_{DDQ}
DQ2	DQ4	V_{DD}	SSF	CMD6	CMD3	CMD0	AE_L	OE_L	SADR 21	SADR 18	SADR 16	SADR 12	SADR 9	SADR 7	SADR 6	NC	SADR 0	V_{DD}	DQ3
NC	NC	NC	SSV	CMD5	CMD1	CMDV	V_{DDQ}	PHS_L	V_{DDQ}	SADR 19	V_{DDQ}	NC	SADR 10	SADR 11	NC	SADR 4	SADR 3	NC	NC
NC	NC	CMD8	CMD7	V_{DDQ}	V_{DD}	NC	CE_L	NC	V_{DD}	SADR 20	SADR 17	SADR 14	SADR 13	V_{DD}	SADR 8	V_{DDQ}	SADR 2	SADR 1	NC

AI04270

Figure 4. M7020 Block Diagram

Comparand Registers[15:0]
Global Mask Registers [7:0]
Information and Command Register
Burst Read Register
Burst Write Register
Next Free Address Register
Search Successful Index Registers [7:0]
(All registers are 68-bit-wide)

PHS_L
CLK2X
RST_L

TAP Controller — TAP

Compare/PIO Data

DQ [67:0]

Cmd | Compare/PIO Data

Address Decode

Configurable as
64K x 34
32K x 68
16K x 136
8K x 272
Data Array

Configurable as
64K x 34
32K x 68
16K x 136
8K x 272
Mask Array

Priority Encode

Match Logic

Command Decode and PIO Access

CMD [8:0]
CMDV
ACK
EOT

ID [4:0]

Pipeline and SRAM Control

SADR [21:0]
OE_L
WE_L
CE_L
ALE_L

FULL [6:0]

Full Logic

FULL

FULO [1:0]

LHI [6:0]
BHI [2:0]

Arbitration Logic

LHO [1:0]
BHO [2:0]
SSF
SSV

AI04271

PART NUMBERING

Table 3. Ordering Information Scheme

Example: M7   020   R   –066   ZA   1   T

Device Type

M7 Search Engine

Density

020 = 2Mb (64Kb x 34 Entries)

Operating Supply Voltage

V_{DD} = 1.8V = R

Speed

–066 = 66 Million Searches per Second

–050 = 50 Million Searches per Second

Package

PBGA = 272-count, 27mm x 27mm[1], 1.27mm ball pitch

Temperature Range

1 = 0 to 70 °C

Shipping Option

Tape & Reel Packing = T

Note: 1. Where "Z" is the symbol for BGA packages and "A" denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.