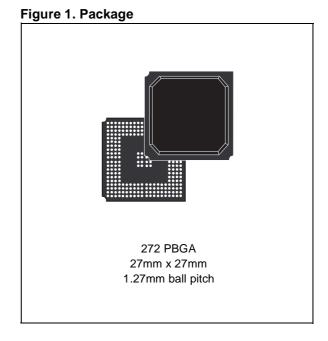


16 Kbit x 68 bit Entry Network Search Engine

DATA BRIEFING

FEATURES SUMMARY

- 16K DATA ENTRIES IN 68-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO FOUR (4) QUADRANTS (Data entry width in each quadrant is configurable as 34, 68, 136, or 272 bits.)
- UP TO 83 MILLION SUSTAINED SEARCHES PER SECOND IN 68-BIT and 136-BIT CONFIGURATIONS
- UP TO 41.5 MILLION SEARCHES PER SECOND IN 34-BIT and 272-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 124K to 992K DEPENDING ON THE SIZE OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE: V_{DD} (Operating Supply Voltage) = 1.8V V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 272 BALL, 27mm x 27mm, CAVITY-UP BGA



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DESCRIPTION

Overview

The M7010 is a feature-rich hardware search engine optimized for networking and communications applications. It incorporates leading-edge Associative Processing Technology (APT, trademark of Lara Networks. Inc.) and Advanced Power Management. The data table may be partitioned into up to four (4) quadrants, allowing the user to configure each quadrant with different table entry widths (x34, x68, x136, or x272-bit). It is also programmable to accelerate performance.

Performance

The M7010 outperforms competitive solutions using software sequential search algorithms in conjunction with SRAMs or ASICs, or hardware implementation with ASICs and CAMs. The latter solution, while faster than a software-based solution, still suffers from performance degradation when depth-cascaded and is unable to scale to next-generation requirements. The M7010-based solutions overcome all of these drawbacks.

Applications

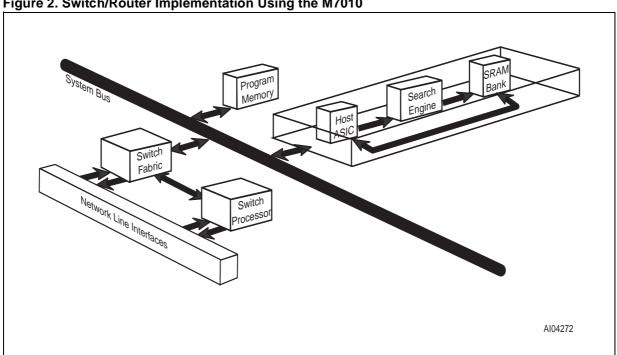
The performance and features of the M7010 makes it ideal in applications such as enterprise LAN switches, broadband switching and routing equipment, supporting multiple data rates from OC-48 and beyond.

Figure 2 illustrates how a search engine subsystem can be optimized using a host bridge ASIC (or a dedicated co-processor, such as the Lara Networks LNI8010), the M7010, and synchronous or non-synchronous SRAMs. It also illustrates how this system fits into a switch-router implementation.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed		
M7010R-083ZA1	1.8V	2.5 or 3.3V	83MHz		
M7010R-066ZA1	1.8V	2.5 or 3.3V	66MHz		





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Table 2. Signal Names

Clocks and Reset						
CLK2X	Master Clock					
PHS_L	Phase					
RST_L	Reset					
	Command and DQ Bus					
CMD[8:0]	Command Bus					
CMDV	Command Valid					
DQ[67:0]	Address/Data Bus					
ACK	READ Acknowledge					
EOT	End of Transfer					
SSF	Search Successful Flag					
SSV	Search Successful Flag Valid					
SADR[21:0]	SRAM Address					
CE_L	SRAM Chip Enable					
WE_L	SRAM Write Enable					
OE_L	SRAM Output Enable					
ALE_L	Address Latch Enable					

Cascade Interface							
LHI[6:0]	Local Hit In						
LHO[1:0]	Local Hit Out						
BHI[2:0]	Block Hit In						
BHO[2:0]	Block Hit Out						
FULI[6:0]	Full In						
FULO[1:0]	Full Out						
FULL	Full Flag						
	Device Identification						
ID[4:0]	Device Identification						
Test Access Port							
TDI	Test Access Port's Test Data In						
TCK	Test Access Port's Test Clock						
TDO	Test Access Port's Test Data Out						
TMS	Test Access Port's Test Mode Select						
TRST_L	Test Access Port's Reset						

Note: Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate 1. ACK and EOT Signals require a pull-down resistor of 47 ohms.

Figure 3. Connections

NC	GND	EOT	NC	NC	V_{DD}	FULI5	FULI4	FULI1	вно0	V _{DD}	BHI0	LHI6	NC	V_{DD}	ID2	ID0	TDO	NC	NC
NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	вно1	BHI2	V_{DDQ}	LHI5	LHI3	LHI2	ID3	TMS	TDI	V _{DD}	NC
DQ64	NC	NC	V _{DDQ}	V _{DD}	V_{DDQ}	NC	NC	V_{DDQ}	вно2	V _{DD}	LHO1	LHI4	V_{DDQ}	LHI0	ID1	TCK	NC	NC	DQ
DQ62	NC	V _{DD}	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	T RST_L	GND	DQ63	DQ61	DQ:
DQ60	V_{DDQ}	NC	DQ66						TC)P					DQ67	DQ59	NC	DQ	
V_{DD}	NC	DQ56	DQ58													V _{DDQ}	DQ55	DQ49	٧ _D
DQ50	V _{DDQ}	DQ52	DQ54													DQ47	V_{DDQ}	DQ51	۷ _{DI}
NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ.
DQ40	DQ42	V_{DDQ}	DQ44					GND	GND	GND	GND						DQ39	V _{DD}	DQ
V_{DD}	NC	DQ36	DQ38	LEFT				GND	GND	GND	GND		RIGHT			V _{DDQ}	DQ35	DQ33	DQ
V _{DDQ}	DQ34	DQ32	DQ30	LEFI				GND	GND	GND	GND					V _{DDQ}	NC	DQ29	٧ _D
NC	DQ28	V_{DDQ}	DQ26					GND	GND	GND	GND					NC	DQ23	DQ25	DQ
DQ24	V _{DD}	DQ20	GND													GND	DQ19	V _{DDQ}	DQ
DQ22	DQ16	DQ14	V _{DDQ}												V _{DDQ}	NC	DQ15	DQ	
V_{DD}	DQ18	V_{DDQ}	DQ6													DQ9	DQ11	DQ13	۷ _D
NC	DQ12	DQ8	DQ0						вот	ТОМ					DQ1	DQ5	DQ7	NO	
DQ10	NC	V_{DDQ}	GND	NC	CMD2	CMD4	GND	WE_L	CLK2X	V _{DD}	SADR 15	GND	V_{DDQ}	SADR 5	V _{DDQ}	GND	NC	NC	V _{DE}
DQ2	DQ4	V _{DD}	SSF	CMD6	CMD3	CMD0	AE_L	OE_L	SADR 21	SADR 18	SADR 16	SADR 12	SADR 9	SADR 7	SADR 6	NC	SADR 0	V _{DD}	DC
NC	NC	NC	SSV	CMD5	CMD1	CMDV	V _{DDQ}	PHS_L	V_{DDQ}	SADR 19	V_{DDQ}	NC	SADR 10	SADR 11	NC	SADR 4	SADR 3	NC	N
NC	NC	CMD8	CMD7	V _{DDQ}	V _{DD}	NC	CE_L	NC	V_{DD}	SADR 20	SADR 17	SADR 14	SADR 13	V _{DD}	SADR 8	V_{DDQ}	SADR 2	SADR 1	N

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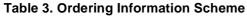
PHS_L ---Comparand Registers[15:0] CLK2X -Global Mask Registers [7:0] Information and Command Register
Burst Read Register RST_L → Burst Write Register Next Free Address Register Search Successful Index Registers [7:0] Compare/PIO Data (All registers are 68-bit-wide) TAP TAP Controller DQ [67:0] Cmd Compare/PIO Data Configurable as SADR [21:0] 32K x 34 16K x 68 CMD [8:0] -OE_L Command 8K x 136 Pipeline Address Decode Priority Encode CMDV 4K x 272 Decode Match Logic and and PIO Access Data Array ACK -SRAM WE_L Control EOT -Configurable as 32K x 34 CE_L 16K x 68 8K x 136 ALE_L ID [4:0] 4K x 272 Mask Array Full Logic FULL [6:0] -FULL LHI [6:0] -LHO [1:0] BHI [2:0] -Arbitration BHO [2:0] Logic SSF FULO [1:0] SSV

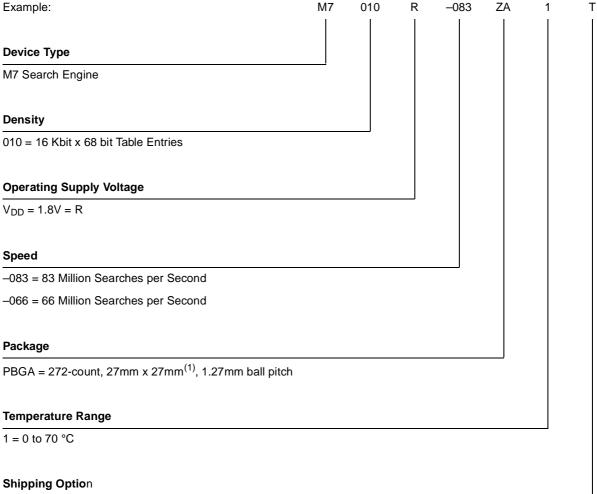
Figure 4. M7010 Block Diagram

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AI04273

PART NUMBERING





Tape & Reel Packing = T

Note: 1. Where "Z" is the symbol for BGA packages and "A" denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

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