ST Microelectronics
GRENOBLE PLANT

Standard Linear ICs, DSG

SHORT QUALIFICATION REPORT

LINE : **185X**

PRODUCT NAME : **TS1851/ TS1852/ TS1854**

LINE DESCRIPTION : **LOW POWER RAIL TO RAIL OPERATIONAL AMPLIFIER**

WAFER CODE : **C1851AAH / C1852AAH / C1854AAH**

PACKAGE : **SOT23-5 / SO8 & 14 / TSSOP8 & 14 / DIP8 & 14**

Qualification plan REFERENCE : **7139741**

CONTENTS

DEVICE DESCRIPTION

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS1851**
Function	(type)	**Single op-amp r/rail low power 1.8V**
Die name	(Part number)	**P1851AAH**
Die size	(mm * mm)	**1.40*0.88**
Shrink	(Level)	**N/A**
Transistor count	(Number)	**181**
Process	(Name)	**HF2CMOS 2µm**
Process qualification	(Date)	**Q4/96**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter)	**6”**
		radius value
	(Tickness)	**375µm**
	(Dopant type)	**P**
	(Epi type)	**N**
Mask set reference	(Name)	**1851A**
Masks	(Number)	**18**

Minimum effective dimension(Nature/Width) **2µm (Metal - Metal)**

Composite defect density (Defects per cm2) **0.17**

Layers(M1,M2,poly1,poly2,etc..) (Nature/Width)

	Nature	**Thickness**	**Width**	**Pitch**
M1:	**AlSiCu**	**0.6µm**	**2µm**	**4.5µm**
M2:	**AlSiCu**	**1.05µm**	**2µm**	**4.5µm**
Poly1:	**Poly**	**0.4µm**	**2µm**	**4.5µm**
Poly2:	**Poly**	**0.4µm**	**2µm**	**4.5µm**

Frontside metallisation layers	(Nature / Tickness)	**AlSiCu 06µm/ AlSiCu 1.05µm**
Backside metallisation layers	(Nature / Tickness)	**RAW SILICON / 50µm**
Passivation layers	(Nature / Thickness)	**PVAPOX 0.5µm+NITRIDE 0.6µm**
	(Method)	**CVD**
Process flow	(Reference)	**HFMS580**
Fault coverage level	(%)	**100%**

DEVICE DESCRIPTION

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS1852**
Function	(type)	**Dual op-amp r/rail low power 1.8V**
Die name	(Part number)	**P1852AAH**
Die size	(mm * mm)	**1.56*1.46**
Shrink	(Level)	**N/A**
Transistor count	(Number)	**362**
Process	(Name)	**HF2CMOS 2µm**
Process qualification	(Date)	**Q4/96**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter)	**6”**
		radius value
	(Tickness)	**375µm**
	(Dopant type)	**P**
	(Epi type)	**N**
Mask set reference	(Name)	**1852A**
Masks	(Number)	**18**
Minimum effective dimension	(Nature/Width)	**2µm (Metal - Metal)**
Composite defect density	(Defects per cm2	**0.17**

Layers(M1,M2,poly1,poly2,etc..) (Nature/Width)

	Nature	**Thickness**	**Width**	**Pitch**
M1:	**AlSiCu**	**0.6µm**	**2µm**	**4.5µm**
M2:	**AlSiCu**	**1.05µm**	**2µm**	**4.5µm**
Poly1:	**Poly**	**0.4µm**	**2µm**	**4.5µm**
Poly2:	**Poly**	**0.4µm**	**2µm**	**4.5µm**

Frontside metallisation layers	(Nature / Tickness)	**AlSiCu 06µm/ AlSiCu 1.05µm**
Backside metallisation layers	(Nature / Tickness)	**RAW SILICON / 50µm**
Passivation layers	(Nature / Thickness)	**PVAPOX 0.5µm+NITRIDE 0.6µm**
	(Method)	**CVD**
Process flow	(Reference)	**HFMS580**
Fault coverage level	(%)	**100%**

DEVICE DESCRIPTION

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS1854**
Function	(type)	**Quad op-amp r/rail low power 1.8V**
Die name	(Part number)	**P1854AAH**
Die size	(mm * mm)	**2.32*1.95**
Shrink	(Level)	**N/A**
Transistor count	(Number)	**724**
Process	(Name)	**HF2CMOS 2µm**
Process qualification	(Date)	**Q4/96**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter)	**6”**
		radius value
	(Tickness)	**375µm**
	(Dopant type)	**P**
	(Epi type)	**N**
Mask set reference	(Name)	**1854A**
Masks	(Number)	**18**
Minimum effective dimension	(Nature/Width)	**2µm (Metal - Metal)**
Composite defect density	(Defects per cm2	**0.17**

Layers(M1,M2,poly1,poly2,etc..) (Nature/Width)

	Nature	**Thickness**	**Width**	**Pitch**
M1:	**AlSiCu**	**0.6µm**	**2µm**	**4.5µm**
M2:	**AlSiCu**	**1.05µm**	**2µm**	**4.5µm**
Poly1:	**Poly**	**0.4µm**	**2µm**	**4.5µm**
Poly2:	**Poly**	**0.4µm**	**2µm**	**4.5µm**

Frontside metallisation layers	(Nature / Tickness)	**AlSiCu 06µm/ AlSiCu 1.05µm**
Backside metallisation layers	(Nature / Tickness)	**RAW SILICON / 50µm**
Passivation layers	(Nature / Thickness)	**PVAPOX 0.5µm+NITRIDE 0.6µm**
	(Method)	**CVD**
Process flow	(Reference)	**HFMS580**
Fault coverage level	(%)	**100%**

ELECTRICAL CHARACTERISATION PRESENTATION

Since the process technology and electrical specifications are identical forthese devices, this report covers the entire family. The characterisation was performed on the**TS1851, TS1852 & TS1854** devices.

ASSURANCE OF THE DEVICE PARAMETERS AT CORNER TEMPERATURES

1st level :

During the Design phase the critical parameters are simulated at temperature min and max.

2nd level :

During the Evaluation phase 50 units are tested at temperature min andmax and the results are compared to the simulations and to the specification.

The CPK must be > 2 for 98% of the parameters and > 1.33 for the others.

3rd level :

The limits of specification at temperature are calculated to include the temperature drift evaluated at the 2nd level compared to the specification at 25°C.

4th level :

The test is made at 25°C with the limits of the specification at 25°C, so with a guard band compared to the limits at temperature.
The test results at 25°C and temperature with the CP/CPK calculation and the specification are available in the qualification report. This report is available for all new products and for redesigned products.

QUALIFICATION RESULTS

a) Electrical results

* Yield analysis on 3 lots : conform to ST standard results
* Electrical parameters distribution on 50 pièces at T°AMB = 25°C results conform to datasheet specification

b) ESD measurement was performed

* ESD resistance is > **2 KV** ***according to MILSTD883C***
* ESD resistance is > **200V** ***according to Machin Model***
* ESD resistance is > **1.5 KV** ***according to Charge Device Model***

c) Latch-up measurement was performed according to ST specification (n°0018695)

* No latch-up was observed

d) Reliability tests were performed according to the qualification plan

Reliability test	Nb of rejects	Package
High temperature bias test (HTB) T° AMB = 125°C - Duration = 1000h	0/78 x2 0/78 0/77 0/77 0/77 0/77	SO8 1851 &1852 SO14 1854 TSSOP8 0922 TSSOP14 0924 SOT23-5 0951 DIP8 0462
Temperature & humidity bias (THB) T°AMB = 85°C humidity = 85% Duration = 1000h	0/78 x2 0/78 0/77 0/77 0/77 0/77	SO8 1851 &1852 SO14 1854 SOT23-5 0951 TSSOP8 0462 TSSOP14 0464 DIP8 0462
Temperature cycling (CT) T°AMB = -65/150°C Nb cycles = 1000	0/50 0/50 0/50 0/50 0/50	SO8 1851 SOT23-5 0951 TSSOP8 0462 TSSOP14 0464 DIP8 0462
Presure pot test (PPT) T°AMB = 121°C Pressure = 2atm - Duration = 240h	0/50 0/50 0/50 0/50 0/50	SO8 1851 SOT23-5 0951 TSSOP8 0462 TSSOP14 0464 DIP8 0462

e) Conclusion

* Electrical and reliability results meet or exceed the requirements set in the ST qualification program. The devices TS1851, TS1852 and TS1854 are qualified for all packages (SOT23-5, S08, DIP8, TSSOP8, SO14, TSSOP14 and DIP14).

NB : Detailed results are available upon request

"WARNING" : Tests results and information contained in this document are for information only. This document does not alter ST Microelectronic's standard warranty or product specification

PRODUCT DESIGN QUALIFICATION FLOW

"Quality is what the customer says it is."
Tom Peters

Manufacturing and reliability must be considered at the design level in order to manufacture reliable products meeting customers' expectations.

New product development plans adopt the Quality Function Deployment **(QFD)** methodology as a basic tool to understand customers' requirements. This formally translates the customers' need into technical requirements as product specifications, process operations and manufacturing process controls, that represent the key points for the product finalization.

In SGS-THOMSON, a corporate procedure defines the product maturity, specifying three maturity levels with rules from one level to the next. They are: design, engineering and production. In addition there are various sub levels. This procedure governs the entire life cycle of a product from new product proposal to its obsolescence. It also determines when and how, engineering samples can be released at sub-maturity levels in a controlled manner by defining "for application study only" or "not yet fully qualified" on the customer documentation.

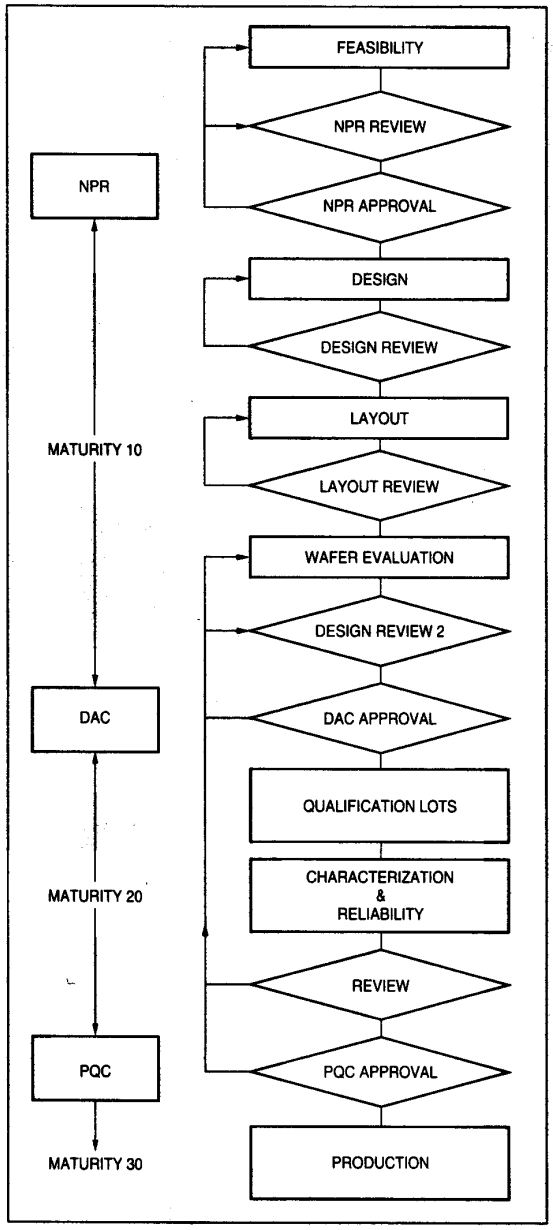
Each new product begins from the preparation of a target specification and a document called a New Product Request **(NPR)**, which contains business and technical details. The purpose of this first control is to evaluate the potential of the product and determine if there is sufficient justification to allocate design resources.

Once the NPR is approved the designers can start work. Designers work to clearly defined design rules which incorporate robust design principles. When the design is complete and the first working samples are available they are evaluated to make sure that the design is acceptable for the next phase, Engineering.

The results of these tests are included in the next key document, the Design Approval Certificate **(DAC)**. The approval of the DAC commits the company to a major investment so it is essential to ensure that the product is ready to proceed.

While a product is in design and characterization (maturity 10 & 20), samples may be given to customers with the documentation indicating "engineering samples for application study only and at the customers' risk" under the responsibility of the Division Manager.

New product is prepared for qualification through product characterization and reliability testing. A Product Qualification Certificate **(PQC)** which permits the new product to proceed to manufacturing must be approved by Group Management.



Product design qualification flow