ST Microelectronics
GRENOBLE PLANT

Standard Linear ICs, DSG

SHORT QUALIFICATION REPORT

LINE : **094X**

PRODUCT NAME : **TS94X**

LINE DESCRIPTION : **OUTPUT RAIL TO RAIL BiCMOS µPOWER OPAMP**

WAFER CODE : **C0941AAH/C0942AAZ/C0944AAH**

PACKAGES : **SOT23/SO8/SO14/TSSOP14/DIP8/DIP14**

NPQP REFERENCE : **7086741**

TEI REFERENCE : **E917093XA**

May 4, 2000

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DEVICE DESCRIPTION: TS944

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS944**
Function	(Type)	**Quad µPower amplifier**
Die name	(Part number)	**C0944AAH**
Die size	(mm*mm)	**2,34*1,95**
Process	(Name)	**HFMS510**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter) (Thickness) (Dopant type) (Epi type)	**6"** **375 µm** **N** **P100**
Mask set reference	(Name)	**X944**
Masks	(Number)	**17**
Minimum effective dimension	(Nature/Width)	**Contact/1µm**
Composite defect density	(Defects per cm2/level for 94%)	**0.01**
FrontSide metallization layers	(Nature/Width)	**AlSiCu/0.6µm** **AlSiCu/1.05µm**
Backside metallisation layers	(Nature / Tickness)	**Silicon**
Passivation layers	(Nature / Thickness)	**PVapox/0.5µm,** **SiNo2/0.6µm**
Fault coverage level	(%)	**100**

DEVICE DESCRIPTION: TS942

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS942**
Function	(Type)	**Dual µPower amplifier**
Die name	(Part number)	**C0942AAZ**
Die size	(mm*mm)	**1,5*1,4**
Process	(Name)	**HFMS610**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter) (Thickness) (Dopant type) (Epi type)	**6"** **375 µm** **N** **P100**
Mask set reference Masks	(Name) (Number)	**PE42A** **16**

Minimum effective dimension	(Nature/Width)	**Contact/1µm**
Composite defect density	(Defects per cm2/level for 94%)	**0.01**
FrontSide metallization layers	(Nature/Width)	**AlSiCu/0.6µm** **AlSiCu/1.05µm**
Backside metallisation layers	(Nature / Tickness)	**Silicon**
Passivation layers	(Nature / Thickness)	**PVapox/0.5µm,** **SiNo2/0.6µm**
Fault coverage level	(%)	**100**

DEVICE DESCRIPTION: TS941

Wafer Fab. Process	**Asked**	**Answer**
Device name	(Part number)	**TS941**
Function	(Type)	**Single µPower amplifier**
Die name	(Part number)	**C0941AAH**
Die size	(mm*mm)	**0,9*1,4**
Process	(Name)	**HFMS510**
Wafer fab.	(Location)	**Carrollton**
Wafer characteristics	(Diameter) (Thickness) (Dopant type) (Epi type)	**6"** **375 µm** **N** **P100**
Mask set reference Masks	(Name) (Number)	**X941** **17**

Minimum effective dimension	(Nature/Width)	**Contact/1µm**
Composite defect density	(Defects per cm2/level for 94%)	**0.01**
FrontSide metallization layers	(Nature/Width)	**AlSiCu/0.6µm** **AlSiCu/1.05µm**
Backside metallisation layers	(Nature / Tickness)	**Silicon**
Passivation layers	(Nature / Thickness)	**PVapox/0.5µm,** **SiNo2/0.6µm**
Fault coverage level	(%)	**100**

ELECTRICAL CHARACTERISATION PRESENTATION

The TS94X family contains ouput Rail to Rail BiCMOS µPower operational amplifier.

Please find enclosed the qualification report for the **TS941, TS942 and TS944** family of **operational amplifiers products**.

Since the processing technology and electrical specifications are identical for these devices, this report covers the entire family. The characterisation was performed on the **TS944, TS941** devices.

The products below are available:

TS944: quad operational amplifier.
TS942: dual operational amplifier.
TS941: single operational amplifier

NOTES :
- The high class versions (TS941B, TS942B and TS944B) are screened at final test. For this reason, it is not possible to calculate Cpk values for parameters selected for high class specifications.

- Others parameters like Cmr or Svr cannot have a Cpk calculated due to a none gaussien law.

ASSURANCE OF THE DEVICE PARAMETERS AT CORNER TEMPERATURES

1st level :

During the Design phase the critical parameters are simulated at temperature min and max.

2nd level :

During the Evaluation phase 50 units are tested at temperature min and max and the results are compared to the simulations and to the specification.

The CPK must be > 2 for 98% of the parameters and > 1.33 for the others.

3rd level :

The limits of specification at temperature are calculated to include the temperature drift evaluated at the 2nd level compared to the specification at 25°C.

4th level :

The test is made at 25°C with the limits of the specification at 25°C, so with a guard band compared to the limits at temperature.
The test results at 25°C and temperature with the CP/CPK calculation and the specification are available in the qualification report. This report is available for all new products and for redesigned products.

QUALIFICATION RESULTS

a) Electrical results

* Yield analysis on 5 lots: conform to ST standard results
* Electrical parameters distribution on 50 pieces at T°AMB = 25°C: results conform to datasheet specification.

b) ESD measurement was performed according to MILSTD883C, Machine Model & Charge device Model

* TS941: HBM > 2 KV, MM > 200V, CDM > 1000 V.
* TS942: HBM > 2 KV.
* TS944: HBM > 2 KV, MM > 200V, CDM > 1500 V.

c) Latch-up measurement was performed according to ST specification (n°0018695)

* No latch-up was observed

d) Reliability tests were performed according to the qualification plan

Reliability test	Device	Nb of rejects	Package
High temperature bias test (HTB) T° AMB = 125°C - Duration = 1000h	TS944 TS942 TS942 TS941 TS951 TS934	0/76 0/76 0/76 0/78 0/76 0/77	SO14 SO8 DIP8 SO8 SOT23-5 TSSOP14
Temperature and Humidity Bias (THB) T=85°C / RH=85% - Duration=1000h	TS942 TS942 TS951 TS925	0/76 0/76 0/76 0/77	SO8 DIP8 SOT23-5 TSSOP16
Pressure Pot (PPT) 121°C / 2atm, 480h (TS942) and 240 h (TS944)	TS944 TS942 TS942 TS951	0/77 0/50 0/50 0/50	SO14 SO8 DIP8 SOT23-5
Temperature Cycling (TC) T=-65°C / +150°C - Duration: 1000 cycles (TS944) and 500 cycles (TS942)	TS944 TS942 TS942 TS951	0/77 0/50 0/50 0/50	SO14 SO8 DIP8 SOT23-5

e) Conclusion

* Electrical and reliability results meet or exceed the requirements set in the ST qualification program. These devices are qualified for all packages (**SO8, SO14, TSSOP14, SOT23-5**, **DIP8 and DIP14**).

We take in account electrical and reliability results got on TS925, and TS951 devices (which are manufactured with the same wafer process) for respectively **TSSOP** and **SOT23-5** packages.

NB : Detailed results are available upon request

"WARNING" : Tests results and information contained in this document are for information only. This document does not alter ST Microelectronic's standard warranty or product specification.

PRODUCT DESIGN QUALIFICATION FLOW

"Quality is what the customer says it is."
Tom Peters

Manufacturing and reliability must be considered at the design level in order to manufacture reliable products meeting customers' expectations.

New product development plans adopt the Quality Function Deployment **(QFD)** methodology as a basic tool to understand customers' requirements. This formally translates the customers' need into technical requirements as product specifications, process operations and manufacturing process controls, that represent the key points for the product finalization.

In SGS-THOMSON, a corporate procedure defines the product maturity, specifying three maturity levels with rules from one level to the next. They are: design, engineering and production. In addition there are various sub levels. This procedure governs the entire life cycle of a product from new product proposal to its obsolescence. It also determines when and how, engineering samples can be released at sub-maturity levels in a controlled manner by defining "for application study only" or "not yet fully qualified" on the customer documentation.

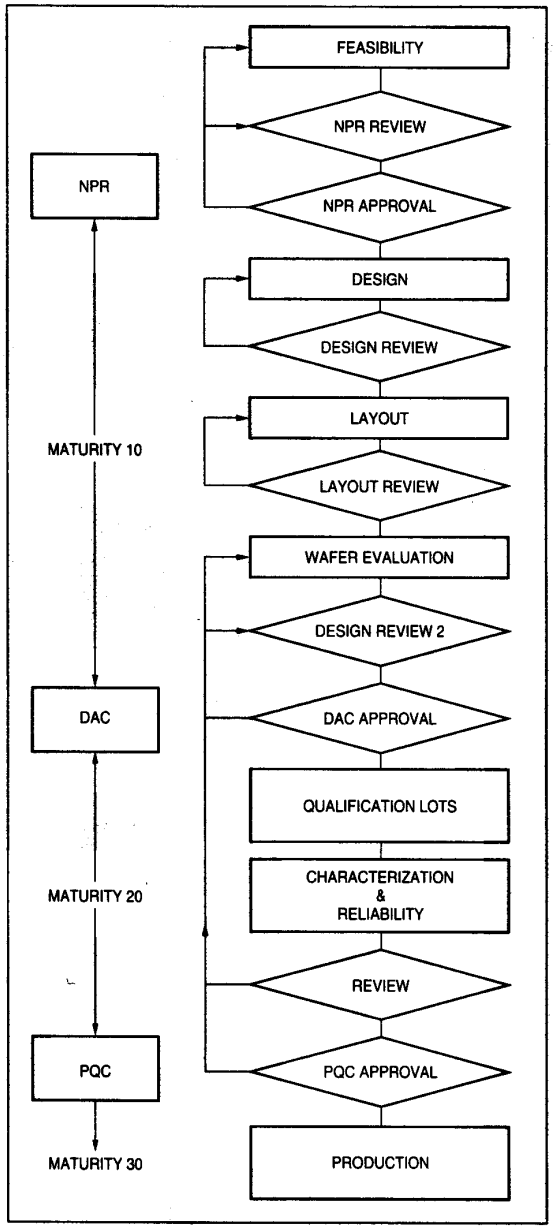
Each new product begins from the preparation of a target specification and a document called a New Product Request **(NPR)**, which contains business and technical details. The purpose of this first control is to evaluate the potential of the product and determine if there is sufficient justification to allocate design resources.

Once the NPR is approved the designers can start work. Designers work to clearly defined design rules which incorporate robust design principles. When the design is complete and the first working samples are available they are evaluated to make sure that the design is acceptable for the next phase, Engineering.

The results of these tests are included in the next key document, the Design Approval Certificate **(DAC)**. The approval of the DAC commits the company to a major investment so it is essential to ensure that the product is ready to proceed.

While a product is in design and characterization (maturity 10 & 20), samples may be given to customers with the documentation indicating "engineering samples for application study only and at the customers' risk" under the responsibility of the Division Manager.

New product is prepared for qualification through product characterization and reliability testing. A Product Qualification Certificate **(PQC)** which permits the new product to proceed to manufacturing must be approved by Group Management.



Product design qualification flow