ST Microelectronics
GRENOBLE PLANT

Standard Linear ICs, DSG

SHORT QUALIFICATION REPORT

LINE : **093X**

PRODUCT NAME : **TS93X**

LINE DESCRIPTION : **MICROPOWER OPERATIONAL AMPLIFIER**

WAFER CODE : **093XAAH**

PACKAGES : **TS931 : SO8 / SOT23-5**
TS932 : SO8 / DIP8
TS934 : SO14 / DIP14 / TSSOP14

NPQP REFERENCE : **7139595**

TEI REFERENCE : **E917093XA**

January 19, 2000

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DEVICE DESCRIPTION

Wafer Fab. Process	Asked	Answer		
		931	932	934
Device name	(Part number)	**TS931**	**TS932**	**TS934**
Function	(type)	**Rail to Rail**	**Voltage Low Output**	**Power**
Die name	(Part number)	**0931AAH**	**0932AAH**	**0934AAH**
Die size (X x Y)	(mm x mm)	**0.9 x 1.4**	**1.7 x 1.4**	**2.35 x 1.95**
Shrink	(Level)	**N/A**		
Transistor count	(Number)	**77**	**152**	**302**
Process	(Name)		**HF2CMOS**	
Process qualification	(Date)		**Q4/1996**	
Wafer fab.	(Location)		**Carroltton**	
Wafer characteristics	(Diameter)		**6”**	
			radius value	
	(Tickness)		**375 µm**	
	(Dopant type)		**P**	
	(Epi type)		**N**	
Mask set reference	(Name)	**X931AA**	**X932AA**	**X934AA**
Masks	(Number)	**16**	**16**	**16**
Minimum effective dimension	(Nature/Width)		**2µm (Metal-Metal)**	
Composite defect density	(Defects per cm2)		**0.17**	
	NATURE	*THICKNESS*	*WIDTH*	*PITCH*
Layers(M1,M2,poly1,poly2,etc..)	M1 : **AlSiCu**	**0.6µm**	**2µm**	**4.5µm**
	M2 : **AlSiCu**	**1.05µm**	**2µm**	**4.5µm**
	POLY1 : **Poly**	**0.4µm**	**2µm**	**4.5µm**
	POLY2 : **Poly**	**0.4µm**	**2µm**	**4.5µm**
Frontside metallisation layers	(Nature /Thickness)		**AlSiCu**	
Backside metallisation layers	(Nature /Thickness)		**Silicon**	
Passivation layers	(Nature /Thickness)		**Pvapox + Silicon Nitride**	
	(Method)		**CVD**	
Process flow	(Reference)		**Hfms510A**	
Fault coverage level	(%)		**100**	

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ELECTRICAL CHARACTERISATION PRESENTATION

Since the processing technology and electrical specifications are identical for the three **TS931**, **TS932** & **TS934** devices, this report covers the entire family. The characterisation was performed on the **TS931** device.

NOTES :

The high class versions (**TS93XA**) are screened at final test. For this reason, it is not possible to calculate Cpk values for parameters selected for high class specifications.

For the production program :
The input offset current (Iio) and input bias current (Iib) parameters (originating from the input protection diodes leakage currents) are tested with Vcc = 5V, even for the 3V specified versions. Please note that Vcc = 5V is the most severe condition.

The AVD parameter cannot be tested due to low accuracy of test system. This parameter value is too high (100000)

ASSURANCE OF THE DEVICE PARAMETERS AT CORNER TEMPERATURES

1st level :

During the Design phase the critical parameters are simulated at temperature min and max.

2nd level :

During the Evaluation phase 50 units are tested at temperature min and max and the results are compared to the simulations and to the specification.

The CPK must be > 2 for 98% of the parameters and > 1.33 for the others.

3rd level :

The limits of specification at temperature are calculated to include the temperature drift evaluated at the 2nd level compared to the specification at 25°C.

4th level :

The test is made at 25°C with the limits of the specification at 25°C, so with a guard band compared to the limits at temperature.
The test results at 25°C and temperature with the CP/CPK calculation and the specification are available in the qualification report. This report is available for all new products and for redesigned products.

QUALIFICATION RESULTS

a) Electrical results

* Yield analysis on 3 lots : conform to ST standard results
* Electrical parameters distribution on 50 pièces at T°AMB (= 25°C) and at cold and hot temperature : results conform to datasheet specification

b) ESD measurement was performed according to MILSTD883C

* ESD resistance is :

HBM > **2 KV**
MM > **200 V**
CDM > **2 KV**

c) Latch-up measurement was performed according to ST specification (n°0018695)

***** No latch-up was observed

d) Reliability tests were performed according to the qualification plan

Reliability test	Nb of rejects	Package
High temperature bias test (HTB) T° AMB = 125°C - Duration = 1000h	0/77 x 3	0931 SOT23-5 / 0932 SO8 0934 TSSOP14
Temperature & humidity bias (THB) T°AMB = 85°C humidity = 85% Duration = 1000h	0/77 x 3	0951 SOT23-5 / 0942 SO8 0925 TSSOP16
Temperature cycling (CT) T°AMB = -65/150°C Nb cycles = 1000	0/77 x 3	0931 SOT23-5 / 0942 SO8 0462 TSSOP8
Presure pot test (PPT) T°AMB = 121°C Pressure = 2atm - Duration = 240h	0/77 x 3	0931 SOT23-5 / 0942 SO8 0462 TSSOP8

e) Conclusion

* Electrical and reliability results meet or exceed the requirements set in the ST qualification program. The devices TS931, TS932 and TS934 are qualified for all packages (**SOT23-5, SO8, DIP8, TSSOP14, SO14** and **DIP14**).

NB : Detailed results are available upon request

"WARNING" : Tests results and information contained in this document are for information only. This document does not alter ST Microelectronic's standard warranty or product specification

S08 / 0931 DAC 1st PAGE

N° : D9110931A

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0931	Sales types : TS931ID & IDT
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0931AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 0931 = 0.9 x 1.4	Die size (mm²) : 1.26
Gross by wafer : 0931=12654	Packages : SO8
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 3.295	Sales (M$) : 1.5
Man. margin (K$) : 580	A.S.P. ($) : 0.15
Development cost (K$) : 78	Unit man. cost ($) : 0.093
Payback time (Y)/compl. Year : 1.2	Man. margin (M$) :

This document states that the product satisfies electrical specification and then preseries can start to characterize it, to optimize testing and to perform reliability test.

SIGNED BY :	NAME	DATE	SIGNATURE
Product responsible	A. JAC	26/11/99	
Product responsible	F. JACQUIN	26/11/99	
Program manager	N. BANCHERI	26/11/99	
Designer	J. BOURGOIN	26/11/99	
Product Engineering	A. CHASSAGNEUX	29/11/99	
Division manager	JC. KAIRE	29/11/99 (p.o.)	A. CHASSAGNEUX
APPROVED BY:			
GROUP GENERAL MANAGER	p.o JC. KAIRE	29/11/99 (p.o.)	A. CHASSAGNEUX

SOT23-5 / 0931 DAC 1st PAGE

N° : D9110931B

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0931	Sales types : TS931ILT
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0931AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 0.9 x 1.4	Die size (mm²) : 1.26
Gross by wafer : 12654	Packages : SOT23-5
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 3.295	Sales (M$) : 1.5
Man. margin (K$) : 580	A.S.P. ($) : 0.15
Development cost (K$) : 78	Unit man. cost ($) : 0.093
Payback time (Y)/compl. Year : 1.2	Man. margin (M$) :

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Program manager	N. BANCHERI	26/11/99	
Designer	J. BOURGOIN	26/11/99	
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Division manager	JC. KAIRE	29/11/99 (p.o)	A. CHASSAGNEUX
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GROUP GENERAL MANAGER	p.o JC. KAIRE	29/11/99 (p.o)	A. CHASSAGNEUX

SO8 / 0932 DAC 1st PAGE

N° : D9110932B

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0932	Sales types : TS932ID & DT
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0932AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 1.7 x 1.4	Die size (mm²) : 2.38
Gross by wafer : 6637	Packages :SO8
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 3.466	Sales (M$) : 1
Man. margin (K$) : 260	A.S.P. ($) : 0.25
Development cost (K$) : 61	Unit man. cost ($) : 0.186
Payback time (Y)/compl. Year : 1	Man. margin (M$) :

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Program manager	N. BANCHERI	26/11/99	
Designer	J. BOURGOIN	26/11/99	
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GROUP GENERAL MANAGER	p.o JC. KAIRE	29/11/99 (p.o.)	A. CHASSAGNEUX

DIP8 / 0932 DAC 1st PAGE

N° : D9110932A

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0932	Sales types : TS932IN
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0932AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 1.7 x 1.4	Die size (mm²) : 2.38
Gross by wafer : 6637	Packages : DIP8
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 3.466	Sales (M$) : 1
Man. margin (K$) : 260	A.S.P. ($) : 0.25
Development cost (K$) : 61	Unit man. cost ($) : 0.186
Payback time (Y)/compl. Year : 1	Man. margin (M$) :

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Division manager	JC. KAIRE	29/11/99 (p.o.)	
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SO14 / 0934 DAC 1st PAGE

N° : D9110934B

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0934	Sales types : TS934ID & IDT
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0934AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 2.35 x 1.95	Die size (mm^2) : 4.5825
Gross by wafer : 3406	Packages : SO14
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 1.58	Sales (M$) : 0.46
Man. margin (K$) : 109	A.S.P. ($) : 0.23
Development cost (K$) : 61	Unit man. cost ($) : 0.144
Payback time (Y)/compl. Year : 1	Man. margin (M$) :

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DIP14 / 0934 DAC 1st PAGE

N° : D9110934A

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0934	Sales types : TS934IN
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0934AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 2.35 x 1.95	Die size (mm²) : 4.5825
Gross by wafer : 3406	Packages : DIP14
ECONOMIC INFORMATION	
Cumulative 5 years :	**Peak sales year :**
Sales (M$) : 1.58	Sales (M$) : 0.46
Man. margin (K$) : 109	A.S.P. ($) : 0.23
Development cost (K$) : 61	Unit man. cost ($) : 0.144
Payback time (Y)/compl. Year : 1	Man. margin (M$) :

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TSSOP14 / 0934 DAC 1st PAGE

N° : D9110934C

DESIGN APPROVAL CERTIFICATE

DESIGN APPROVAL CERTIFICATE (1/4) **Date : 24/11/99**

Line code : 0934	Sales types : TS934IPT
Description : Output rail to rail Micropower Operational Amplifier	PL family: 71 (Std Linear Ics DSG)
Market segment : Telecom Computer Consumer	Design location : Grenoble
MAIN TECHNICAL DATA	
Wafer code : 0934AAH	Process : HF2CMOS
Diffusion plant : CARROLLTON	Wafer size (inches) : 6"
Die size (X Y, mm) : 2.35 x 1.95	Die size (mm²) : 4.5825
Gross by wafer : 3406	Packages : TSSOP14
ECONOMIC INFORMATION	
Cumulative 6 years :	**Peak sales year :**
Sales (M$) : 1.58	Sales (M$) : 0.46
Man. margin (K$) : 109	A.S.P. ($) : 0.23
Development cost (K$) : 61	Unit man. cost ($) : 0.144
Payback time (Y)/compl. Year : 1	Man. margin (M$) :

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PRODUCT DESIGN QUALIFICATION FLOW

"Quality is what the customer says it is."
Tom Peters

Manufacturing and reliability must be considered at the design level in order to manufacture reliable products meeting customers' expectations.

New product development plans adopt the Quality Function Deployment **(QFD)** methodology as a basic tool to understand customers' requirements. This formally translates the customers' need into technical requirements as product specifications, process operations and manufacturing process controls, that represent the key points for the product finalization.

In SGS-THOMSON, a corporate procedure defines the product maturity, specifying three maturity levels with rules from one level to the next. They are: design, engineering and production. In addition there are various sub levels. This procedure governs the entire life cycle of a product from new product proposal to its obsolescence. It also determines when and how, engineering samples can be released at sub-maturity levels in a controlled manner by defining "for application study only" or "not yet fully qualified" on the customer documentation.

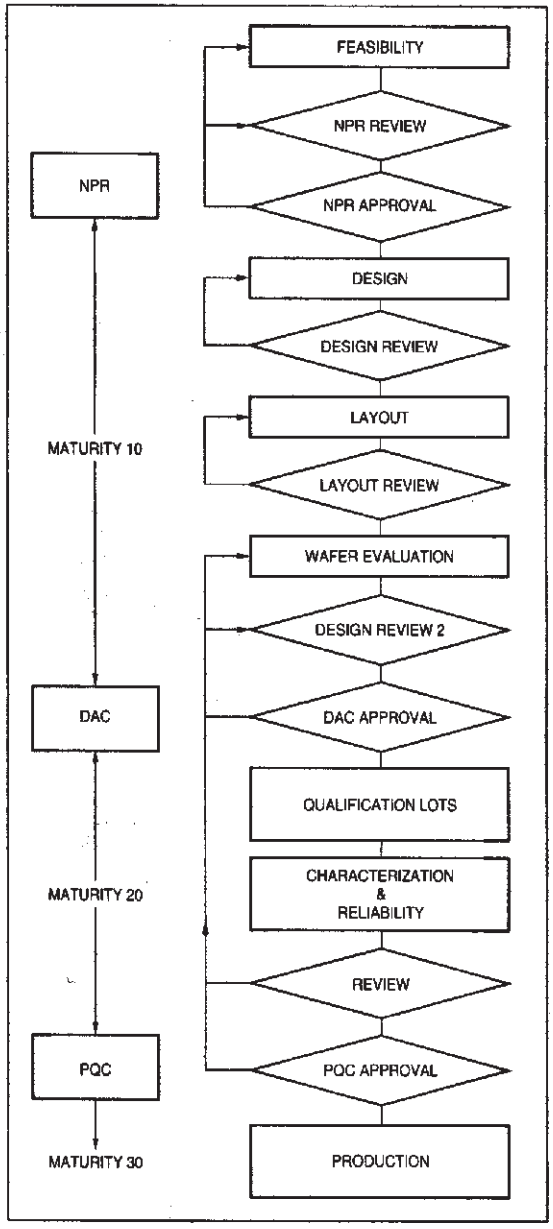
Each new product begins from the preparation of a target specification and a document called a New Product Request **(NPR)**, which contains business and technical details. The purpose of this first control is to evaluate the potential of the product and determine if there is sufficient justification to allocate design resources.

Once the NPR is approved the designers can start work. Designers work to clearly defined design rules which incorporate robust design principles. When the design is complete and the first working samples are available they are evaluated to make sure that the design is acceptable for the next phase, Engineering.

The results of these tests are included in the next key document, the Design Approval Certificate **(DAC)**. The approval of the DAC commits the company to a major investment so it is essential to ensure that the product is ready to proceed.

While a product is in design and characterization (maturity 10 & 20), samples may be given to customers with the documentation indicating "engineering samples for application study only and at the customers' risk" under the responsibility of the Division Manager.

New product is prepared for qualification through product characterization and reliability testing. A Product Qualification Certificate **(PQC)** which permits the new product to proceed to manufacturing must be approved by Group Management.



Product design qualification flow